

# ELECTRONIC MODEL SHOP DORADO MIDAS LISTINGS

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by

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Bravo files stored on: [Indigo]<DoradoSource>GarageMidasManual.Dm

Press files stored on: [Indigo]<DoradoDocs>GarageMidasListings.Press

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## 1. Kernel.Midas

```

L X Reset          ; KERNEL.MIDAS display relevant rm, im values for kernel diagnostics
L X Do-it
L X Ld KERNEL      ; load the microprogram
L B0 Addr RBASE 0
L B1 Addr RBASE 17
L B0 Val 0
L B1 Val 0
L B2 Addr MCR
L B2 Val 1        ; turn off stack overflow/underflow wakeups from memC
L B4 Addr STACKPTOPBITS
L B5 Addr STACKPADDR
L C0 Addr R0      ; display common registers
L C1 Addr R1
L C2 Addr RM1
L C3 Addr R01
L C4 Addr R10
L C5 Addr RHIGH1
L C6 Addr RSCR
L C7 Addr RSCR2
L C8 Addr T 20
L C9 Addr FLAGS  ; control for hold, task simulator
L C10 Addr ITERATIONS ; count of iterations
L C11 Addr NEXTTASK
L C12 Addr HOLDVALUE
L C13 Addr
L C14 Addr
L A19 Addr TASK 20 ; use task 0 as default
L A19 Val 0
L A7 Addr RBASE 20 ; use rbase 17 as default
L A7 Val 0
L X DisplayOn      ; May 18, 1981 11:43 AM
L X TimeOut 10000
L X Call XORTASKCIRC() ; TURN ON TASK CIRCULATE
L X Skip 1
L X ShowError Timed out
L X TimeOut 100000
L X Go BEGIN
L X Skip 1
L X ShowError Timed out

```

## 2. MemA.Midas

```

L X Reset
L X Do-it
L X Ld MEMA        ; load memAll diagnostic
L C0 Addr R0;      This code is stolen from "showS.midas"
L C1 Addr SVA      ; current virtual address for storage
L C2 Addr COL      ; current cache column
L C3 Addr SEXPECTED
L C4 Addr ;        leave it blank
L C5 Addr RSCR
L C6 Addr RSCR2
L C7 Addr T 20;    End code stolen from "showS.midas"

```

```

L C8 Addr ROW 0
L C12 Addr ITERATIONS
L C13 Addr MEMFLAGS
L C14 Addr FLAGS
L C15 Addr ROW 1
L B0 Addr SPATX;           Begin more code stolen from "showS.midas"
L B1 Addr CURSPATTERN
L B2 Addr SVAX
L B3 Addr SVAHIX
L B4 Addr SMAXBRHI
L B5 Addr SNMODULES
L B6 Addr SSUBRSCR
L B7 Addr SVAHIOLD
L B8 Addr SVAXOLD
L B9 Addr SIMSCR0           ; SIM TASK SCRATCH REGISTER
L B10 Addr SIMSCR1        ; SIM TASK SCRATCH REGISTER
L B11 Addr SMCRVICTIM
L B11 Addr HOLD
L B12 Addr PIPE 0
L B15 Addr PIPE 10
L A19 Addr TASK 20        ; use task 0 as default
L A19 Val 0
L A7 Addr RBASE 20        ; use rbase 17 as default
L A7 Val 17
L A17 Addr PROCSRN           ; init procsr to zero
L A17 Val 0
L X DisplayOn              ; memA.midas August 13, 1979 6:44 PM
L X UnBrk SVATRYNEXTPAT
L X TimeOut 4000000; 120 min, for 12 megaword memory systems.
L X Go BEGIN
L X Skip 1
L X ShowError Timed out

```

### 3. MemMisc.Midas

```

; Modified by Frank Vest
; April 9, 1985
L X Reset
L X Do-it                 ; Added by McDaniel June 1, 1981 4:50 PM
L X Ld MEMMISC           ; load memAll diagnostic
;L X DisplayOn
L C0 Addr R0
L C1 Addr ANFAULTSX
L C2 Addr ANFAULTSX2
L C3 Addr ATESTTASKX
L C4 Addr ASUBTASKX
L C5 Addr ASRNX
L C6 Addr AUSESRN
L C7 Addr AMAKINGFAULTS
L C8 Addr RSCR
L C9 Addr RSCR2
L C10 Addr RSCR3
L C11 Addr T 20;         End code stolen from "showS.midas"
L C12 Addr ITERATIONS
L C13 Addr MEMFLAGS

```

```

L C14 Addr FLAGS
L C15 Addr
L C16 Addr
L C17 Addr
L B0 Addr PIPE 0
L B4 Addr PIPE 10
L B8 Addr ROW 0
L B12 Addr HOLD
L B13 Addr
L B14 Addr ARLINK
L B15 Addr TPC 2
L B16 Addr TPC 1;           End code stolen from "showS.midas"
L A19 Addr TASK 20 ; use task 0 as default
L A19 Val 0
L A7 Addr RBASE 20 ; use rbase 17 as default
L A7 Val 17
L A17 Addr PROCSRN           ; init procsr to zero
L A17 Val 0
L A14 Val -1                 ; Set Q to 1777777 to make sure of task switch.
L X DisplayOn                ; memMisc.midas July 10, 1979 2:51 PM
L X TimeOut 400000; increase timeout for 256k memory chips
L X Go BEGIN
L X Skip 1
L X ShowError Timed out

```

#### 4. IfuSimple.Midas

```

L X Reset                    ; IFU midas display June 18, 1981 10:15 AM
L X Do-it
L X Ld ifuSimple             ; load the microprogram
L B0 Addr RBASE 0           ; Rbase values
L B1 Addr RBASE 17
L B0 Val 0
L B1 Val 0
L B2 Addr MEMRQ             ; MIDAS MUFFLERS
L B3 Addr LOADS
L B4 Addr HJ
L B5 Addr MX
L B6 Addr JMPEXC
L B7 Addr PCJ
L B8 Addr FFK
L B9 Addr HOLD;
L B10 Addr ITESTX          ; ifu test number
L B11 Addr ITESTCOUNTX   ; ifujump count
L B12 Addr ICURRENTTESTLOC ;byte (memory) address of beginning of ifu test program.
L B13 Addr KLINK           ;place where return link from ifu jumps is kept
L B14 Addr TPC 1           ;convenient task pc we can clobber w/ KLINK contents to get pretty print
L B15 Addr STKP
L B15 Val 1;               initialize stkp for convenience
L B15 Addr ;               throw it away to avoid cluttered screen
L C0 Addr R0                ; display common registers
L C1 Addr
L C2 Addr EXPECTEDDISPATCH
L C3 Addr PAT16
L C4 Addr IADDRX

```

```

L C5 Addr RHIGH1
L C6 Addr RSCR
L C7 Addr RSCR2
L C8 Addr T 20
L C9 Addr FLAGS ; control for hold, task simulator
L C10 Addr ITERATIONS ; count of iterations
L C11 Addr NEXTTASK
L C12 Addr HOLDVALUE
L C13 Addr
L C14 Addr
L A19 Addr TASK 20 ; use task 0 as default
L A19 Val 0
L A7 Addr RBASE 20 ; use rbase 17 as default
L A7 Val 17
L X DisplayOn ; June 18, 1981 10:14 AM
L X TimeOut 100000
L X Go BEGIN
L X Skip 1
L X ShowError Timed out

```

## 5. IfuComplex.Midas

```

L X Reset ; IFU midas display June 18, 1981 10:15 AM
L X Do-it
L X Ld ifuComplex ; load the microprogram
L B0 Addr RBASE 0 ; Rbase values
L B1 Addr RBASE 17
L B0 Val 0
L B1 Val 0
L B2 Addr MEMRQ ; MIDAS MUFFLERS
L B3 Addr LOADS
L B4 Addr HJ
L B5 Addr MX
L B6 Addr JMPEXC
L B7 Addr PCJ
L B8 Addr FFK
L B9 Addr HOLD;
L B10 Addr ITESTX; ifu test number
L B11 Addr ITESTCOUNTX; ifujump count
L B12 Addr ICURRENTTESTLOC;byte (memory) address of beginning of ifu test program.
L B13 Addr KLINK; place where return link from ifu jumps is kept
L B14 Addr TPC 1; convenient task pc we can clobber w/ KLINK contents to get pretty print
L B15 Addr STKP
L B15 Val 1; initialize stkp for convenience
L B15 Addr ; throw it away to avoid cluttered screen
L C0 Addr R0 ; display common registers
L C1 Addr
L C2 Addr EXPECTEDDISPATCH
L C3 Addr PAT16
L C4 Addr IADDRX
L C5 Addr RHIGH1
L C6 Addr RSCR
L C7 Addr RSCR2
L C8 Addr T 20
L C9 Addr FLAGS ; control for hold, task simulator

```

```

L C10 Addr ITERATIONS          ; count of iterations
L C11 Addr NEXTTASK
L C12 Addr HOLDVALUE
L C13 Addr
L C14 Addr
L A19 Addr TASK 20      ; use task 0 as default
L A19 Val 0
L A7 Addr RBASE 20     ; use rbase 17 as default
L A7 Val 17
L X DisplayOn           ; June 18, 1981 10:14 AM
L X TimeOut 100000
L X Go BEGIN
L X Skip 1
L X ShowError Timed out

```

## 6. EventCounters.Midas

```

;L X DisplayOn           ; October 12, 1979 5:59 PM
L X Reset                ; event counters midas display
L X Do-it
L X Ld eventCounters    ; load the microprogram
L B0 Addr RBASE 0      ; Rbase values
L B1 Addr RBASE 17
L B0 Val 17
L B1 Val 17
;L B2 Addr MEMRQ       ; MIDAS MUFFLERS
L B3 Addr LOADS
L B4 Addr HJ
L B5 Addr MX
L B6 Addr JMPEXC
L B7 Addr PCJ
L B8 Addr FFK
L B9 Addr HOLD;
;L B10 Addr
;L B11 Addr
;L B12 Addr
L B13 Addr KLINK;      place where return link from ifu jumps is kept
L B14 Addr TPC 1;     convenient task pc we can clobber w/ KLINK contents to get pretty print
L B15 Addr STKP
L B15 Val 1;          initialize stkp for convenience
L B15 Addr ;          throw it away to avoid cluttered screen
L B16 Addr CTRL0
L C0 Addr R0           ; display common registers
;L C1 Addr
;L C2 Addr
;L C3 Addr
;L C4 Addr
;L C5 Addr
L C6 Addr RSCR
L C7 Addr RSCR2
L C8 Addr T 20
L C9 Addr FLAGS        ; control for hold, task simulator
L C10 Addr ITERATIONS  ; count of iterations
L C11 Addr NEXTTASK
L C12 Addr HOLDVALUE

```

```

L C13 Addr
L C14 Addr
L C15 Addr
L A19 Addr TASK 20 ; use task 0 as default
L A19 Val 0
L A7 Addr RBASE 20 ; use rbase 17 as default
L A7 Val 17
L X DisplayOn ; May 18, 1981 11:43 AM
L X TimeOut 100000
L X Go BEGIN
L X Skip 1
L X ShowError Timed out
    
```

## 7. TriconD.Midas

```

;L X Displayon ; July 19, 1979 1:55 PM
L X Reset ; KERNEL.MIDAS display relevant rm, im values for TriconD diagnostics
L X Do-it
L X Ld TriconD ; load the microprogram
L B0 Addr RBASE 0
L B1 Addr RBASE 14
L B2 Addr KSTATE
L B3 Addr KSTAT
L B4 Addr KRAM
L B5 Addr KTAG
L B6 Addr KFIFO
L B15 Addr DMUX100
L B16 Addr DMUX101
L B17 Addr DMUX102
L B18 Addr DMUX103
L B19 Addr DMUX104
L C0 Addr ERRORS ; display common registers
L C1 Addr T 14
L C2 Addr KSCR
L C3 Addr KSCR2
L C4 Addr KSCR3
L C5 Addr KSCR4
L C6 Addr COUNT
L C7 Addr COUNTS
L C8 Addr KSCRS
L C9 Addr ; control for hold, task simulator
L C10 Addr ITERATIONS ; count of iterations
L C11 Addr
L C12 Addr
L C13 Addr
L C14 Addr
L C15 Addr
L C16 Addr
L C17 Addr
L A19 Addr TASK 20 ; use task 0 as default
L A19 Val 14
L A7 Addr RBASE 20 ; use rbase 17 as default
L A7 Val 17
L X DisplayOn
L X TimeOut 100000
    
```

L X Go BEGIN  
L X Skip 1  
L X ShowError Timed out

## 8. Triex.Midas

L X Ld TRIMESA  
L X Timeout 7777777777; as close to infinite timeout as we can manage.  
L X Go INITMAP  
L X Skip 1  
L X ShowError Timed out  
L X Abort

## 9. KernelS.Midas

; Written by Frank Vest  
; May 1, 1984  
L X SetClk  
L X 31  
L X RunProg  
L X KERNEL  
L A6 SkipE DONE+1  
L X ShowError KERNEL Failed AT 31 NS  
L X SetClk  
L X 30  
L X Timeout 30000 ; 12 seconds  
L X Go BEGIN  
L X Skip 1  
L X ShowError KERNEL Failed AT 30 NS. Timed out  
L A6 SkipE DONE+1  
L X ShowError KERNEL Failed AT 30 NS  
L X SetClk  
L X 29  
L A2 Val 476 ;Quit checking for RM parity errors at speeds faster than 30 ns.  
;(ProcH board has a known problem).  
L X Timeout 30000  
L X Go BEGIN  
L X Skip 1  
L X ShowError KERNEL Failed AT 29 NS. Timed out  
L A6 SkipE DONE+1  
L X ShowError KERNEL Failed AT 29 NS  
L X SetClk  
L X 28  
L X Timeout 30000  
L X Go BEGIN  
L X Skip 1  
L X ShowError KERNEL Failed AT 28 NS. Timed out  
L A6 SkipE DONE+1  
L X ShowError KERNEL Failed AT 28 NS  
L X SetClk  
L X 27  
L X Timeout 30000  
L X Go BEGIN  
L X Skip 1

L X ShowError KERNEL Failed AT 27 NS. Timed out  
L A6 SkipE DONE+1  
L X ShowError KERNEL Failed AT 27 NS  
L X SetClk  
L X 26  
L X TimeOut 30000  
L X Go BEGIN  
L X Skip 1  
L X ShowError KERNEL Failed AT 26 NS. Timed out  
L A6 SkipE DONE+1  
L X ShowError KERNEL Failed AT 26 NS  
L X SetClk  
L X 25  
L X TimeOut 30000  
L X Go BEGIN  
L X Skip 1  
L X ShowError KERNEL Failed AT 25 NS. Timed out  
L A6 SkipE DONE+1  
L X ShowError KERNEL Failed AT 25 NS  
L X SetClk  
L X 24  
L X TimeOut 30000  
L X Go BEGIN  
L X Skip 1  
L X ShowError KERNEL Failed AT 24 NS. Timed out  
L A6 SkipE DONE+1  
L X ShowError KERNEL Failed AT 24 NS  
L X SetClk  
L X 23  
L X TimeOut 30000  
L X Go BEGIN  
L X Skip 1  
L X ShowError KERNEL Failed AT 23 NS. Timed out  
L A6 SkipE DONE+1  
L X ShowError KERNEL Failed AT 23 NS  
L X SetClk  
L X 22  
L X TimeOut 30000  
L X Go BEGIN  
L X Skip 1  
L X ShowError KERNEL Failed AT 22 NS. Timed out  
L A6 SkipE DONE+1  
L X ShowError KERNEL Failed AT 22 NS

## 10. MemaS.Midas

; Modified by Frank Vest  
; May 7, 1985  
L X SetClk  
L X 31  
L X RunProg  
L X MEMA  
L A6 SkipE DONE+1  
L X ShowError MEMA Failed AT 31 NS  
L X SetClk  
L X 30

L X TimeOut 40000000  
L X Go BEGIN  
L X Skip 1  
L X ShowError MEMA Failed AT 30 NS (Timed out)  
L A6 SkipE DONE+1  
L X ShowError MEMA Failed AT 30 NS  
L X SetClk  
L X 29  
L A2 Val 476 ;Quit checking for RM parity errors at speeds faster than 30 ns.  
;(ProcH board has a known problem).  
L X TimeOut 40000000  
L X Go BEGIN  
L X Skip 1  
L X ShowError MEMA Failed AT 29 NS (Timed out)  
L A6 SkipE DONE+1  
L X ShowError MEMA Failed AT 29 NS  
L X SetClk  
L X 28  
L X TimeOut 40000000  
L X Go BEGIN  
L X Skip 1  
L X ShowError MEMA Failed AT 28 NS (Timed out)  
L A6 SkipE DONE+1  
L X ShowError MEMA Failed AT 28 NS  
L X SetClk  
L X 27  
L X TimeOut 40000000  
L X Go BEGIN  
L X Skip 1  
L X ShowError MEMA Failed AT 27 NS (Timed out)  
L A6 SkipE DONE+1  
L X ShowError MEMA Failed AT 27 NS  
L X SetClk  
L X 26  
L X TimeOut 40000000  
L X Go BEGIN  
L X Skip 1  
L X ShowError MEMA Failed AT 26 NS (Timed out)  
L A6 SkipE DONE+1  
L X ShowError MEMA Failed AT 26 NS  
L X SetClk  
L X 25  
L X TimeOut 40000000  
L X Go BEGIN  
L X Skip 1  
L X ShowError MEMA Failed AT 25 NS (Timed out)  
L A6 SkipE DONE+1  
L X ShowError MEMA Failed AT 25 NS  
L X SetClk  
L X 24  
L X TimeOut 40000000  
L X Go BEGIN  
L X Skip 1  
L X ShowError MEMA Failed AT 24 NS (Timed out)  
L A6 SkipE DONE+1  
L X ShowError MEMA Failed AT 24 NS  
L X SetClk

L X 23  
L X TimeOut 4000000  
L X Go BEGIN  
L X Skip 1  
L X ShowError MEMA Failed AT 23 NS (Timed out)  
L A6 SkipE DONE+1  
L X ShowError MEMA Failed AT 23 NS  
L X SetClk  
L X 22  
L X TimeOut 4000000  
L X Go BEGIN  
L X Skip 1  
L X ShowError MEMA Failed AT 22 NS (Timed out)  
L A6 SkipE DONE+1  
L X ShowError MEMA Failed AT 22 NS

## 11. MemMiscS.Midas

; Modified by Frank Vest  
; May 7, 1985  
L X SetClk  
L X 31  
L X RunProg  
L X MEMMISC  
L A6 SkipE DONE+1  
L X ShowError MEMMISC Failed AT 31 NS  
L X SetClk  
L X 30  
L X TimeOut 400000 ; 12 seconds  
L X Go BEGIN  
L X Skip 1  
L X ShowError MEMMISC Failed AT 30 NS (Timed out)  
L A6 SkipE DONE+1  
L X ShowError MEMMISC Failed AT 30 NS  
L X SetClk  
L X 29  
L A2 Val 476 ;Quit checking for RM parity errors at speeds faster than 30 ns.  
;(ProcH board has a known problem).  
L X TimeOut 400000  
L X Go BEGIN  
L X Skip 1  
L X ShowError MEMMISC Failed AT 29 NS (Timed out)  
L A6 SkipE DONE+1  
L X ShowError MEMMISC Failed AT 29 NS  
L X SetClk  
L X 28  
L X TimeOut 400000  
L X Go BEGIN  
L X Skip 1  
L X ShowError MEMMISC Failed AT 28 NS (Timed out)  
L A6 SkipE DONE+1  
L X ShowError MEMMISC Failed AT 28 NS  
L X SetClk  
L X 27  
L X TimeOut 400000  
L X Go BEGIN

L X Skip 1  
L X ShowError MEMMISC Failed AT 27 NS (Timed out)  
L A6 SkipE DONE+1  
L X ShowError MEMMISC Failed AT 27 NS  
L X SetClk  
L X 26  
L X TimeOut 400000  
L X Go BEGIN  
L X Skip 1  
L X ShowError MEMMISC Failed AT 26 NS (Timed out)  
L A6 SkipE DONE+1  
L X ShowError MEMMISC Failed AT 26 NS  
L X SetClk  
L X 25  
L X TimeOut 400000  
L X Go BEGIN  
L X Skip 1  
L X ShowError MEMMISC Failed AT 25 NS (Timed out)  
L A6 SkipE DONE+1  
L X ShowError MEMMISC Failed AT 25 NS  
L X SetClk  
L X 24  
L X TimeOut 400000  
L X Go BEGIN  
L X Skip 1  
L X ShowError MEMMISC Failed AT 24 NS (Timed out)  
L A6 SkipE DONE+1  
L X ShowError MEMMISC Failed AT 24 NS  
L X SetClk  
L X 23  
L X TimeOut 400000  
L X Go BEGIN  
L X Skip 1  
L X ShowError MEMMISC Failed AT 23 NS (Timed out)  
L A6 SkipE DONE+1  
L X ShowError MEMMISC Failed AT 23 NS  
L X SetClk  
L X 22  
L X TimeOut 400000  
L X Go BEGIN  
L X Skip 1  
L X ShowError MEMMISC Failed AT 22 NS (Timed out)  
L A6 SkipE DONE+1  
L X ShowError MEMMISC Failed AT 22 NS

## 12. IfuSimpleS.Midas

L X SetClk  
L X 31  
L X RunProg  
L X IFUSIMPLE  
L A6 SkipE DONE+1  
L X ShowError IFUSIMPLE Failed AT 31 NS  
L X SetClk  
L X 30

L X TimeOut 100000  
L X Go BEGIN  
L X Skip 1  
L X ShowError IFUSIMPLE Failed AT 30 NS. Timed out  
L A6 SkipE DONE+1  
L X ShowError IFUSIMPLE Failed AT 30 NS  
L X SetClk  
L X 29  
L A2 Val 476 ;Quit checking for RM parity errors at speeds faster than 30 ns.  
;(ProcH board has a known problem).  
L X TimeOut 100000  
L X Go BEGIN  
L X Skip 1  
L X ShowError IFUSIMPLE Failed AT 31 NS. Timed out  
L A6 SkipE DONE+1  
L X ShowError IFUSIMPLE Failed AT 29 NS  
L X SetClk  
L X 28  
L X TimeOut 100000  
L X Go BEGIN  
L X Skip 1  
L X ShowError IFUSIMPLE Failed AT 28 NS. Timed out  
L A6 SkipE DONE+1  
L X ShowError IFUSIMPLE Failed AT 28 NS  
L X SetClk  
L X 27  
L X TimeOut 100000  
L X Go BEGIN  
L X Skip 1  
L X ShowError IFUSIMPLE Failed AT 27 NS. Timed out  
L A6 SkipE DONE+1  
L X ShowError IFUSIMPLE Failed AT 27 NS  
L X SetClk  
L X 26  
L X TimeOut 100000  
L X Go BEGIN  
L X Skip 1  
L X ShowError IFUSIMPLE Failed AT 26 NS. Timed out  
L A6 SkipE DONE+1  
L X ShowError IFUSIMPLE Failed AT 26 NS  
L X SetClk  
L X 25  
L X TimeOut 100000  
L X Go BEGIN  
L X Skip 1  
L X ShowError IFUSIMPLE Failed AT 25 NS. Timed out  
L A6 SkipE DONE+1  
L X ShowError IFUSIMPLE Failed AT 25 NS  
L X SetClk  
L X 24  
L X TimeOut 100000  
L X Go BEGIN  
L X Skip 1  
L X ShowError IFUSIMPLE Failed AT 24 NS. Timed out  
L A6 SkipE DONE+1  
L X ShowError IFUSIMPLE Failed AT 24 NS  
L X SetClk

L X 23  
L X TimeOut 100000  
L X Go BEGIN  
L X Skip 1  
L X ShowError IFUSIMPLE Failed AT 23 NS. Timed out  
L A6 SkipE DONE+1  
L X ShowError IFUSIMPLE Failed AT 23 NS  
L X SetClk  
L X 22  
L X TimeOut 10000  
L X Go BEGIN  
L X Skip 1  
L X ShowError IFUSIMPLE Failed AT 22 NS. Timed out  
L A6 SkipE DONE+1  
L X ShowError IFUSIMPLE Failed AT 22 NS

### 13. IfuComplexS.Midas

L X SetClk  
L X 31  
L X RunProg  
L X IFUCOMPLEX  
L A6 SkipE DONE+1  
L X ShowError IFUCOMPLEX Failed AT 31 NS  
L X SetClk  
L X 30  
L X TimeOut 100000  
L X Go BEGIN  
L X Skip 1  
L X ShowError IFUCOMPLEX Failed AT 30 NS. Timed out  
L A6 SkipE DONE+1  
L X ShowError IFUCOMPLEX Failed AT 30 NS  
L X SetClk  
L X 29  
L A2 Val 476 ;Quit checking for RM parity errors at speeds faster than 30 ns.  
;(ProcH board has a known problem).  
L X TimeOut 100000  
L X Go BEGIN  
L X Skip 1  
L X ShowError IFUCOMPLEX Failed AT 29 NS. Timed out  
L A6 SkipE DONE+1  
L X ShowError IFUCOMPLEX Failed AT 29 NS  
L X SetClk  
L X 28  
L X TimeOut 100000  
L X Go BEGIN  
L X Skip 1  
L X ShowError IFUCOMPLEX Failed AT 28 NS. Timed out  
L A6 SkipE DONE+1  
L X ShowError IFUCOMPLEX Failed AT 28 NS  
L X SetClk  
L X 27  
L X TimeOut 100000  
L X Go BEGIN  
L X Skip 1

```

L X ShowError IFUCOMPLEX Failed AT 27 NS. Timed out
L A6 SkipE DONE+1
L X ShowError IFUCOMPLEX Failed AT 27 NS
L X SetClk
L X 26
L X TimeOut 100000
L X Go BEGIN
L X Skip 1
L X ShowError IFUCOMPLEX Failed AT 26 NS. Timed out
L A6 SkipE DONE+1
L X ShowError IFUCOMPLEX Failed AT 26 NS
L X SetClk
L X 25
L X TimeOut 100000
L X Go BEGIN
L X Skip 1
L X ShowError IFUCOMPLEX Failed AT 25 NS. Timed out
L A6 SkipE DONE+1
L X ShowError IFUCOMPLEX Failed AT 25 NS
L X SetClk
L X 24
L X TimeOut 100000
L X Go BEGIN
L X Skip 1
L X ShowError IFUCOMPLEX Failed AT 24 NS. Timed out
L A6 SkipE DONE+1
L X ShowError IFUCOMPLEX Failed AT 24 NS
L X SetClk
L X 23
L X TimeOut 100000
L X Go BEGIN
L X Skip 1
L X ShowError IFUCOMPLEX Failed AT 23 NS. Timed out
L A6 SkipE DONE+1
L X ShowError IFUCOMPLEX Failed AT 23 NS
L X SetClk
L X 22
L X TimeOut 10000
L X Go BEGIN
L X Skip 1
L X ShowError IFUCOMPLEX Failed AT 22 NS. Timed out
L A6 SkipE DONE+1
L X ShowError IFUCOMPLEX Failed AT 22 NS

```

#### 14. SboardTest.Midas

```

; Written by Frank Vest
; Last modified April 9, 1985
L X Reset
L X Do-it
L X Ld MEMA           ; load memAll diagnostic
L C0 Addr R0;       This code is stolen from "showS.midas"
L C1 Addr SVA       ; current virtual address for storage
L C2 Addr COL       ; current cache column
L C3 Addr SEXPECTED

```

```

L C4 Addr ;          leave it blank
L C5 Addr RSCR
L C6 Addr RSCR2
L C7 Addr T 20;      End code stolen from "showS.midas"
L C8 Addr ROW 0
L C9 Addr
L C10 Addr
L C11 Addr
L C12 Addr ITERATIONS
L C13 Addr MEMFLAGS
L C14 Addr FLAGS
L C15 Addr ROW 1
L C16 Addr
L B0 Addr SPATX;      Begin more code stolen from "showS.midas"
L B1 Addr CURSPATTERN
L B2 Addr SVAX
L B3 Addr SVAHIX
L B4 Addr SMAXBRHI
L B5 Addr SNMODULES
L B6 Addr SSUBRSCR
L B7 Addr SVAHIOLD
L B8 Addr SVAXOLD
L B9 Addr SIMSCR0      ; SIM TASK SCRATCH REGISTER
L B10 Addr SIMSCR1    ; SIM TASK SCRATCH REGISTER
L B11 Addr SMCRVICTIM
L B11 Addr HOLD
L B12 Addr PIPE 0
L B15 Addr PIPE 10
L A19 Addr TASK 20
L A19 Addr TASK 20    ; use task 0 as default
L A19 Val 0
L A7 Addr RBASE 20    ; use rbase 17 as default
L A7 Val 17
L A17 Addr PROCSRN      ; init procsr to zero
L A17 Val 0
L X DisplayOn          ; memA.midas August 13, 1979 6:44 PM
L X TimeOut 10000
L X Call ONLYSBOARDTEST(
L X Skip 1
L X ShowError Timed out
L X UnBrk SVATRYNEXTPAT
L X TimeOut 40000000; 120 min, for 12 megaword memory systems.
L X Go BEGIN
L X Skip 1
L X ShowError Timed out

```

## 15. CboardTest.Midas

```

L X Reset
L X Do-it
L X Ld MEMA           ; load memAll diagnostic
L C0 Addr R0;        This code is stolen from "showS.midas"
L C1 Addr SVA         ; current virtual address for storage
L C2 Addr COL         ; current cache column
L C3 Addr SEXPECTED

```

```

L C4 Addr ;          leave it blank
L C5 Addr RSCR
L C6 Addr RSCR2
L C7 Addr T 20;      End code stolen from "showS.midas"
L C8 Addr
L C9 Addr
L C10 Addr
L C11 Addr
L C12 Addr ITERATIONS
L C13 Addr MEMFLAGS
L C14 Addr FLAGS
L C15 Addr
L C16 Addr
L B0 Addr SPATX;      Begin more code stolen from "showS.midas"
L B1 Addr CURSPATTERN
L B2 Addr SVAX
L B3 Addr SVAHIX
L B4 Addr SMAXBRHI
L B5 Addr SNMODULES
L B6 Addr SSUBRSCR
L B7 Addr SVAHIOLD
L B8 Addr SVAXOLD
L B9 Addr SIMSCR0      ; SIM TASK SCRATCH REGISTER
L B10 Addr SIMSCR1    ; SIM TASK SCRATCH REGISTER
L B11 Addr SMCRVICTIM
L B11 Addr HOLD
L B12 Addr PIPE 0
L A19 Addr TASK 20    ; use task 0 as default
L A19 Val 0
L A7 Addr RBASE 20    ; use rbase 17 as default
L A7 Val 17
L A17 Addr PROCSRN      ; init procsr to zero
L A17 Val 0
L X DisplayOn          ; memA.midas August 13, 1979 6:44 PM
L X TimeOut 10000
L X Call ONLYCBOARDTEST(
L X Skip 1
L X ShowError Timed out
;L X UnBrk SVATRYNEXTPAT
L X TimeOut 10000000
L X Go BEGIN
L X Skip 1
L X ShowError Timed out

```

## 16. XboardTest.Midas

```

L X Reset
L X Do-it
L X Ld MEMA           ; load memAll diagnostic
L C0 Addr R0;         This code is stolen from "showS.midas"
L C1 Addr SVA         ; current virtual address for storage
L C2 Addr COL         ; current cache column
L C3 Addr SEXPECTED
L C4 Addr ;          leave it blank
L C5 Addr RSCR

```

```

L C6 Addr RSCR2
L C7 Addr T 20;           End code stolen from "showS.midas"
L C8 Addr MPATLOW
L C9 Addr MPATHI
L C10 Addr
L C11 Addr
L C12 Addr ITERATIONS
L C13 Addr MEMFLAGS
L C14 Addr FLAGS
L C15 Addr
L C16 Addr
L B0 Addr SPATX;         Begin more code stolen from "showS.midas"
L B1 Addr CURSPATTERN
L B2 Addr SVAX
L B3 Addr SVAHIX
L B4 Addr SMAXBRHI
L B5 Addr SNMODULES
L B6 Addr SSUBRSCR
L B7 Addr SVAHIOLD
L B8 Addr SVAXOLD
L B9 Addr SIMSCR0        ; SIM TASK SCRATCH REGISTER
L B10 Addr SIMSCR1      ; SIM TASK SCRATCH REGISTER
L B11 Addr SMCRVICTIM
L B11 Addr HOLD
L B12 Addr PIPE 0
L A19 Addr TASK 20      ; use task 0 as default
L A19 Val 0
L A7 Addr RBASE 20     ; use rbase 17 as default
L A7 Val 17
L A17 Addr PROCSRN      ; init procsr to zero
L A17 Val 0
L X DisplayOn          ; memA.midas August 13, 1979 6:44 PM
L X TimeOut 10000
L X Call ONLYXBOARDTEST(
L X Skip 1
L X ShowError Timed out
;L X UnBrk SVATRYNEXTPAT
L X TimeOut 10000000
L X Go BEGIN
L X Skip 1
L X ShowError Timed out

```

## 17. DboardTest.Midas

```

L X Reset
L X Do-it
L X Ld MEMA             ; load memAll diagnostic
L C0 Addr R0;          This code is stolen from "showS.midas"
L C1 Addr SVA           ; current virtual address for storage
L C2 Addr COL           ; current cache column
L C3 Addr SEXPECTED
L C4 Addr ;            leave it blank
L C5 Addr RSCR
L C6 Addr RSCR2
L C7 Addr T 20;       End code stolen from "showS.midas"

```

```

L C8 Addr
L C9 Addr
L C10 Addr
L C11 Addr
L C12 Addr ITERATIONS
L C13 Addr MEMFLAGS
L C14 Addr FLAGS
L C15 Addr
L C16 Addr
L B0 Addr SPATX;           Begin more code stolen from "showS.midas"
L B1 Addr CURSPATTERN
L B2 Addr SVAX
L B3 Addr SVAHIX
L B4 Addr SMAXBRHI
L B5 Addr SNMODULES
L B6 Addr SSUBRSCR
L B7 Addr SVAHIOLD
L B8 Addr SVAXOLD
L B9 Addr SIMSCR0           ; SIM TASK SCRATCH REGISTER
L B10 Addr SIMSCR1         ; SIM TASK SCRATCH REGISTER
L B11 Addr SMCRVICTIM
L B11 Addr HOLD
L B12 Addr PIPE 0
L A19 Addr TASK 20        ; use task 0 as default
L A19 Val 0
L A7 Addr RBASE 20        ; use rbase 17 as default
L A7 Val 17
L A17 Addr PROCSRN         ; init procsr to zero
L A17 Val 0
L X DisplayOn              ; memA.midas August 13, 1979 6:44 PM
L X Timeout 10000
L X Call ONLYDBOARDTEST(
L X Skip 1
L X ShowError Timed out
;L X UnBrk SVATRYNEXTPAT
L X Timeout 10000000
L X Go BEGIN
L X Skip 1
L X ShowError Timed out

```

## 18. FIO.Midas

```

; This test the MEMMISC test with the FIO option turned on
; Be sure that the memory system is ok before running the FIO Command file
; Last modified April 9, 1985
L X Reset
L X Do-it                   ; Added by McDaniel June 1, 1981 4:50 PM
L X Ld MEMMISC              ; load memAll diagnostic
;L X DisplayOn
L C0 Addr R0
L C1 Addr ANFAULTSX
L C2 Addr ANFAULTSX2
L C3 Addr ATESTTASKX
L C4 Addr ASUBTASKX

```

```

L C5 Addr ASRNX
L C6 Addr AUSESRN
L C7 Addr AMAKINGFAULTS
L C8 Addr RSCR
L C9 Addr RSCR2
L C10 Addr RSCR3
L C11 Addr T 20;           End code stolen from "showS.midas"
L C12 Addr ITERATIONS
L C13 Addr MEMFLAGS
L C14 Addr FLAGS
L C15 Addr
L C16 Addr
L C17 Addr
L B0 Addr
L B1 Addr
L B2 Addr
L B3 Addr
L B4 Addr
L B5 Addr
L B6 Addr
L B7 Addr
L B8 Addr
L B9 Addr
L B10 Addr
L B11 Addr HOLD
L B12 Addr
L B13 Addr
L B14 Addr ARLINK
L B15 Addr TPC 2
L B16 Addr TPC 1;           End code stolen from "showS.midas"
L A19 Addr TASK 20 ; use task 0 as default
L A19 Val 0
L A7 Addr RBASE 20 ; use rbase 17 as default
L A7 Val 17
L A17 Addr PROCSRN ; init procsr to zero
L A17 Val 0
L X DisplayOn ; memMisc.midas July 10, 1979 2:51 PM
L X TimeOut 40000; increase timeout for 256k memory chips
L X Call FIOTESTON() ; TURN ON FIO TEST
L X Skip 1
L X ShowError Timed out
L X TimeOut 100000
L X Go BEGIN
L X Skip 1
L X ShowError Timed out

```

## 19. LAG.Midas

```

.Begin    L X RunProg
          L X KERNEL
          L A6 SkipE DONE+1
          L X ShowError KERNEL Failed
          L X RunProg
          L X MEMMISC
          L A6 SkipE DONE+1
          L X ShowError MEMMISC Failed

```

```

L X RunProg
L X IFUSIMPLE
L A6 SkipE DONE+1
L X ShowError IFUSIMPLE Failed
L X RunProg
L X IFUCOMPLEX
L A6 SkipE DONE+1
L X ShowError IFUCOMPLEX Failed
L X RunProg
L X EVENTCOUNTERS
L A6 SkipE DONE+1
L X ShowError EVENTCOUNTERS Failed
L X RunProg
L X MEMA
L A6 SkipE DONE+1
L X ShowError MEMA Failed
L X BackSkip .Begin

```

## 20. LAG1.Midas

```

.Begin      L X SetClk
            L X 30
            L X RunProg
            L X KERNEL
            L A6 SkipE DONE+1
            L X ShowError KERNEL Failed at 30 Nanoseconds
            L X RunProg
            L X MEMMISC
            L A6 SkipE DONE+1
            L X ShowError MEMMISC Failed 30 Nanoseconds
            L X RunProg
            L X IFUSIMPLE
            L A6 SkipE DONE+1
            L X ShowError IFUSIMPLE Failed 30 Nanoseconds
            L X RunProg
            L X IFUCOMPLEX
            L A6 SkipE DONE+1
            L X ShowError IFUCOMPLEX Failed 30 Nanoseconds
            L X RunProg
            L X EVENTCOUNTERS
            L A6 SkipE DONE+1
            L X ShowError EVENTCOUNTERS Failed 30 Nanoseconds
            L X RunProg
            L X MEMA
            L A6 SkipE DONE+1
            L X ShowError MEMA Failed
            L X ShowError Kernel MemMisc IfuSimple IfuComplex EventCounters and Mema ran at 30 ns

```

## 21. LAGSpeedtest.Midas

```

; Written by Frank Vest
; December 9, 1983 5:49 PM
; Last modified by Frank Vest May 7, 1985
L X SetClk

```

```

L X 31
L X RunProg
L X KERNEL
L A6 SkipE DONE+1
L X ShowError KERNEL Failed AT 31 NS
L X RunProg
L X MEMMISC
L A6 SkipE DONE+1
L X ShowError MEMMISC Failed AT 31 NS
L X RunProg
L X IFUSIMPLE
L A6 SkipE DONE+1
L X ShowError IFUSIMPLE Failed AT 31 NS
L X RunProg
L X IFUCOMPLEX
L A6 SkipE DONE+1
L X ShowError IFUCOMPLEX Failed AT 31 NS
L X RunProg
L X MEMA
L A6 SkipE DONE+1
L X ShowError MEMA Failed AT 31 NS
L X SetClk
L X 30
L X RunProg
L X KERNEL
L A6 SkipE DONE+1
L X ShowError KERNEL Failed AT 30 NS
L X RunProg
L X MEMMISC
L A6 SkipE DONE+1
L X ShowError MEMMISC Failed AT 30 NS
L X RunProg
L X IFUSIMPLE
L A6 SkipE DONE+1
L X ShowError IFUSIMPLE Failed AT 30 NS
L X RunProg
L X IFUCOMPLEX
L A6 SkipE DONE+1
L X ShowError IFUCOMPLEX Failed AT 30 NS
L X RunProg
L X MEMA
L A6 SkipE DONE+1
L X ShowError MEMA Failed AT 30 NS
L X SetClk
L X 29
;If we have RM parity errors at speeds faster than 30 ns. Turn checking off
;(ProcH board has a known problem).
L X RunProg
L X KERNEL
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.
L X Skip +5
L A2 Val 476
L X TimeOut 30000; 12 sec
L X Go
L X Skip 1
L X ShowError KERNEL Timed out at 29 ns.
L A6 SkipE DONE+1

```

L X ShowError KERNEL Failed AT 29 NS  
L X RunProg  
L X MEMMISC  
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.  
L X Skip +5  
L A2 Val 476  
L X TimeOut 400000; 40 sec  
L X Go  
L X Skip 1  
L X ShowError MEMMISC Timed out at 29 ns.  
L A6 SkipE DONE+1  
L X ShowError MEMMISC Failed AT 29 NS  
L X RunProg  
L X IFUSIMPLE  
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.  
L X Skip +5  
L A2 Val 476  
L X TimeOut 30000; 12 sec  
L X Go  
L X Skip 1  
L X ShowError IFUSIMPLE Timed out at 29 ns.  
L A6 SkipE DONE+1  
L X ShowError IFUSIMPLE Failed AT 29 NS  
L X RunProg  
L X IFUCOMPLEX  
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.  
L X Skip +5  
L A2 Val 476  
L X TimeOut 30000; 12 sec  
L X Go  
L X Skip 1  
L X ShowError IFUCOMPLEX Timed out at 29 ns.  
L A6 SkipE DONE+1  
L X ShowError IFUCOMPLEX Failed AT 29 NS  
L X RunProg  
L X MEMA  
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.  
L X Skip +5  
L A2 Val 476  
L X TimeOut 40000000; 80 minutes  
L X Go  
L X Skip 1  
L X ShowError MEMA Timed out at 29 ns.  
L A6 SkipE DONE+1  
L X ShowError MEMA Failed AT 29 NS  
L X SetClk  
L X 28  
L X RunProg  
L X KERNEL  
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.  
L X Skip +5; Skip 5 places if no RM parity error.  
L A2 Val 476 ; Turn off RM parity errors ; 12-9-83  
L X TimeOut 30000; 12 sec ; 12-9-83  
L X Go ; Continue running diagnostic from RM parity errors. ; 12-9-83  
L X Skip 1 ; 12-9-83  
L X ShowError Kernel Timed out at 28 ns. ; 12-9-83  
L A6 SkipE DONE+1

L X ShowError KERNEL Failed AT 28 NS  
L X RunProg  
L X MEMMISC  
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.  
L X Skip +5  
L A2 Val 476  
L X TimeOut 400000; 40 sec  
L X Go  
L X Skip 1  
L X ShowError MEMMISC Timed out at 28 ns.  
L A6 SkipE DONE+1  
L X ShowError MEMMISC Failed AT 28 NS  
L X RunProg  
L X IFUSIMPLE  
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.  
L X Skip +5  
L A2 Val 476  
L X TimeOut 30000; 12 sec  
L X Go  
L X Skip 1  
L X ShowError IFUSIMPLE Timed out at 28 ns.  
L A6 SkipE DONE+1  
L X ShowError IFUSIMPLE Failed AT 28 NS  
L X RunProg  
L X IFUCOMPLEX  
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.  
L X Skip +5  
L A2 Val 476  
L X TimeOut 30000; 12 sec  
L X Go  
L X Skip 1  
L X ShowError IFUCOMPLEX Timed out at 28 ns.  
L A6 SkipE DONE+1  
L X ShowError IFUCOMPLEX Failed AT 28 NS  
L X RunProg  
L X MEMA  
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.  
L X Skip +5  
L A2 Val 476  
L X TimeOut 40000000; 80 minutes  
L X Go  
L X Skip 1  
L X ShowError MEMA Timed out at 28 ns.  
L A6 SkipE DONE+1  
L X ShowError MEMA Failed AT 28 NS  
L X SetClk  
L X 27  
L X RunProg  
L X KERNEL  
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.  
L X Skip +5  
L A2 Val 476  
L X TimeOut 30000; 12 sec  
L X Go  
L X Skip 1  
L X ShowError KERNEL Timed out at 27 ns.  
L A6 SkipE DONE+1

L X ShowError KERNEL Failed AT 27 NS  
L X RunProg  
L X MEMMISC  
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.  
L X Skip +5  
L A2 Val 476  
L X TimeOut 400000; 40 sec  
L X Go  
L X Skip 1  
L X ShowError MEMMISC Timed out at 27 ns.  
L A6 SkipE DONE+1  
L X ShowError MEMMISC Failed AT 27 NS  
L X RunProg  
L X IFUSIMPLE  
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.  
L X Skip +5  
L A2 Val 476  
L X TimeOut 30000; 12 sec  
L X Go  
L X Skip 1  
L X ShowError IFUSIMPLE Timed out at 27 ns.  
L A6 SkipE DONE+1  
L X ShowError IFUSIMPLE Failed AT 27 NS  
L X RunProg  
L X IFUCOMPLEX  
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.  
L X Skip +5  
L A2 Val 476  
L X TimeOut 30000; 12 sec  
L X Go  
L X Skip 1  
L X ShowError IFUCOMPLEX Timed out at 27 ns.  
L A6 SkipE DONE+1  
L X ShowError IFUCOMPLEX Failed AT 27 NS  
L X RunProg  
L X MEMA  
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.  
L X Skip +5  
L A2 Val 476  
L X TimeOut 40000000; 80 minutes  
L X Go  
L X Skip 1  
L X ShowError MEMA Timed out at 27 ns.  
L A6 SkipE DONE+1  
L X ShowError MEMA Failed AT 27 NS  
L X SetClk  
L X 26  
L X RunProg  
L X KERNEL  
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.  
L X Skip +5  
L A2 Val 476  
L X TimeOut 30000; 12 sec  
L X Go  
L X Skip 1  
L X ShowError KERNEL Timed out at 26 ns.  
L A6 SkipE DONE+1

L X ShowError KERNEL Failed AT 26 NS  
L X RunProg  
L X MEMMISC  
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.  
L X Skip +5  
L A2 Val 476  
L X TimeOut 400000; 40 sec  
L X Go  
L X Skip 1  
L X ShowError MEMMISC Timed out at 26 ns.  
L A6 SkipE DONE+1  
L X ShowError MEMMISC Failed AT 26 NS  
L X RunProg  
L X IFUSIMPLE  
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.  
L X Skip +5  
L A2 Val 476  
L X TimeOut 30000; 12 sec  
L X Go  
L X Skip 1  
L X ShowError IFUSIMPLE Timed out at 26 ns.  
L A6 SkipE DONE+1  
L X ShowError IFUSIMPLE Failed AT 26 NS  
L X RunProg  
L X IFUCOMPLEX  
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.  
L X Skip +5  
L A2 Val 476  
L X TimeOut 30000; 12 sec  
L X Go  
L X Skip 1  
L X ShowError IFUCOMPLEX Timed out at 26 ns.  
L A6 SkipE DONE+1  
L X ShowError IFUCOMPLEX Failed AT 26 NS  
L X RunProg  
L X MEMA  
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.  
L X Skip +5  
L A2 Val 476  
L X TimeOut 40000000; 80 minutes  
L X Go  
L X Skip 1  
L X ShowError MEMA Timed out at 26 ns.  
L A6 SkipE DONE+1  
L X ShowError MEMA Failed AT 26 NS  
L X SetClk  
L X 25  
L X RunProg  
L X KERNEL  
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.  
L X Skip +5  
L A2 Val 476  
L X TimeOut 30000; 12 sec  
L X Go  
L X Skip 1  
L X ShowError KERNEL Timed out at 25 ns.  
L A6 SkipE DONE+1

L X ShowError KERNEL Failed AT 25 NS  
L X RunProg  
L X MEMMISC  
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.  
L X Skip +5  
L A2 Val 476  
L X TimeOut 400000; 40 sec  
L X Go  
L X Skip 1  
L X ShowError MEMMISC Timed out at 25 ns.  
L A6 SkipE DONE+1  
L X ShowError MEMMISC Failed AT 25 NS  
L X RunProg  
L X IFUSIMPLE  
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.  
L X Skip +5  
L A2 Val 476  
L X TimeOut 30000; 12 sec  
L X Go  
L X Skip 1  
L X ShowError IFUSIMPLE Timed out at 25 ns.  
L A6 SkipE DONE+1  
L X ShowError IFUSIMPLE Failed AT 25 NS  
L X RunProg  
L X IFUCOMPLEX  
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.  
L X Skip +5  
L A2 Val 476  
L X TimeOut 30000; 12 sec  
L X Go  
L X Skip 1  
L X ShowError IFUCOMPLEX Timed out at 25 ns.  
L A6 SkipE DONE+1  
L X ShowError IFUCOMPLEX Failed AT 25 NS  
L X RunProg  
L X MEMA  
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.  
L X Skip +5  
L A2 Val 476  
L X TimeOut 40000000; 80 minutes  
L X Go  
L X Skip 1  
L X ShowError MEMA Timed out at 25 ns.  
L A6 SkipE DONE+1  
L X ShowError MEMA Failed AT 25 NS  
L X SetClk  
L X 24  
L X RunProg  
L X KERNEL  
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.  
L X Skip +5  
L A2 Val 476  
L X TimeOut 30000; 12 sec  
L X Go  
L X Skip 1  
L X ShowError KERNEL Timed out at 24 ns.  
L A6 SkipE DONE+1

```

L X ShowError KERNEL Failed AT 24 NS
L X RunProg
L X MEMMISC
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.
L X Skip +5
L A2 Val 476
L X TimeOut 400000; 40 sec
L X Go
L X Skip 1
L X ShowError MEMMISC Timed out at 24 ns.
L A6 SkipE DONE+1
L X ShowError MEMMISC Failed AT 24 NS
L X RunProg
L X IFUSIMPLE
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.
L X Skip +5
L A2 Val 476
L X TimeOut 30000; 12 sec
L X Go
L X Skip 1
L X ShowError IFUSIMPLE Timed out at 24 ns.
L A6 SkipE DONE+1
L X ShowError IFUSIMPLE Failed AT 24 NS
L X RunProg
L X IFUCOMPLEX
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.
L X Skip +5
L A2 Val 476
L X TimeOut 30000; 12 sec
L X Go
L X Skip 1
L X ShowError IFUCOMPLEX Timed out at 24 ns.
L A6 SkipE DONE+1
L X ShowError IFUCOMPLEX Failed AT 24 NS
L X RunProg
L X MEMA
L A2 SkipE 12476 ; 12-9-83; Skip the next instruction if RM parity error.
L X Skip +5
L A2 Val 476
L X TimeOut 40000000; 80 minutes
L X Go
L X Skip 1
L X ShowError MEMA Timed out at 24 ns.
L A6 SkipE DONE+1
L X ShowError MEMA Failed AT 24 NS
L X ShowError Kernel MemMisc IfuSimple IfuComplex EventCounters and Mema ran error free at 24 ns.

```

## 22. KernelTask.Midas

```

; Kernel task circulate test
; By Frank Vest
; July 6, 1983 2:24 PM
L X DisplayOff
L A19 SkipE 0 ; Task 0
L X ShowError Kernel Failed. TASK problem, should be at TASK 0
L X TimeOut 30000; 12 sec

```

L X Proceed ; ;P  
L X Skip 1  
L X ShowError Timed out  
; For the next task  
L X DisplayOff  
L A19 SkipE 1 ; Task 1  
L X ShowError Kernel Failed. TASK problem, should be at TASK 1  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P  
L X Skip 1  
L X ShowError Timed out  
; For the next task  
L X DisplayOff  
L A19 SkipE 2 ; Task 2  
L X ShowError Kernel Failed. TASK problem, should be at TASK 2  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P  
L X Skip 1  
L X ShowError Timed out  
; For the next task  
L X DisplayOff  
L A19 SkipE 3 ; Task 3  
L X ShowError Kernel Failed. TASK problem, should be at TASK 3  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P  
L X Skip 1  
L X ShowError Timed out  
; For the next task  
L X DisplayOff  
L A19 SkipE 4 ; Task 4  
L X ShowError Kernel Failed. TASK problem, should be at TASK 4  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P  
L X Skip 1  
L X ShowError Timed out  
; For the next task  
L X DisplayOff  
L A19 SkipE 5 ; Task 5  
L X ShowError Kernel Failed. TASK problem, should be at TASK 5  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P  
L X Skip 1  
L X ShowError Timed out  
; For the next task  
L X DisplayOff  
L A19 SkipE 6 ; Task 6  
L X ShowError Kernel Failed. TASK problem, should be at TASK 6  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P  
L X Skip 1  
L X ShowError Timed out  
; For the next task  
L X DisplayOff  
L A19 SkipE 7 ; Task 7  
L X ShowError Kernel Failed. TASK problem, should be at TASK 7  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P

L X Skip 1  
L X ShowError Timed out  
; For the next task  
L X DisplayOff  
L A19 SkipE 10 ; Task 10  
L X ShowError Kernel Failed. TASK problem, should be at TASK 10  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P  
L X Skip 1  
L X ShowError Timed out  
; For the next task  
L A19 SkipE 11 ; Task 11  
L X ShowError Kernel Failed. TASK problem, should be at TASK 11  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P  
L X Skip 1  
L X ShowError Timed out  
; For the next task  
L A19 SkipE 13 ; Task 13  
L X ShowError Kernel Failed. TASK problem, should be at TASK 13  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P  
L X Skip 1  
L X ShowError Timed out  
; For the next task  
L A19 SkipE 14 ; Task 14  
L X ShowError Kernel Failed. TASK problem, should be at TASK 14  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P  
L X Skip 1  
L X ShowError Timed out  
; For the next task  
L A19 SkipE 15 ; Task 15  
L X ShowError Kernel Failed. TASK problem, should be at TASK 15  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P  
L X Skip 1  
L X ShowError Timed out  
; For the next task  
L A19 SkipE 16 ; Task 16  
L X ShowError Kernel Failed. TASK problem, should be at TASK 16  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P  
L X Skip 1  
L X ShowError Timed out  
; For the next task  
L A19 SkipE 17 ; Task 17  
L X ShowError Kernel Failed. TASK problem, should be at TASK 17  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P  
L X Skip 1  
L X ShowError Timed out  
; For the next task  
L A19 SkipE 0 ; Task 0  
L X ShowError Kernel Failed. TASK problem, should be at TASK 0  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P

L X Skip 1  
L X ShowError Timed out  
; For the next task  
L A19 SkipE 1 ; Task 1  
L X ShowError Kernel Failed. TASK problem, should be at TASK 1  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P  
L X Skip 1  
L X ShowError Timed out  
; For the next task  
L A19 SkipE 2 ; Task 2  
L X ShowError Kernel Failed. TASK problem, should be at TASK 2  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P  
L X Skip 1  
L X ShowError Timed out  
; For the next task  
L A19 SkipE 2 ; Task 2  
L X ShowError Kernel Failed. TASK problem, should be at TASK 2  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P  
L X Skip 1  
L X ShowError Timed out  
; For the next task  
L A19 SkipE 3 ; Task 3  
L X ShowError Kernel Failed. TASK problem, should be at TASK 3  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P  
L X Skip 1  
L X ShowError Timed out  
; For the next task  
L A19 SkipE 3 ; Task 3  
L X ShowError Kernel Failed. TASK problem, should be at TASK 3  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P  
L X Skip 1  
L X ShowError Timed out  
; For the next task  
L A19 SkipE 4 ; Task 4  
L X ShowError Kernel Failed. TASK problem, should be at TASK 4  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P  
L X Skip 1  
L X ShowError Timed out  
; For the next task  
L A19 SkipE 4 ; Task 4  
L X ShowError Kernel Failed. TASK problem, should be at TASK 4  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P  
L X Skip 1  
L X ShowError Timed out  
; For the next task  
L A19 SkipE 5 ; Task 5  
L X ShowError Kernel Failed. TASK problem, should be at TASK 5  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P  
L X Skip 1

L X ShowError Timed out  
; For the next task  
L A19 SkipE 5 ; Task 5  
L X ShowError Kernel Failed. TASK problem, should be at TASK 5  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P  
L X Skip 1  
L X ShowError Timed out  
; For the next task  
L A19 SkipE 6 ; Task 6  
L X ShowError Kernel Failed. TASK problem, should be at TASK 6  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P  
L X Skip 1  
L X ShowError Timed out  
; For the next task  
L A19 SkipE 7 ; Task 7  
L X ShowError Kernel Failed. TASK problem, should be at TASK 7  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P  
L X Skip 1  
L X ShowError Timed out  
; For the next task  
L A19 SkipE 7 ; Task 7  
L X ShowError Kernel Failed. TASK problem, should be at TASK 7  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P  
L X Skip 1  
L X ShowError Timed out  
; For the next task  
L A19 SkipE 10 ; Task 10  
L X ShowError Kernel Failed. TASK problem, should be at TASK 10  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P  
L X Skip 1  
L X ShowError Timed out  
; For the next task  
L A19 SkipE 10 ; Task 10  
L X ShowError Kernel Failed. TASK problem, should be at TASK 10  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P  
L X Skip 1  
L X ShowError Timed out  
; For the next task  
L A19 SkipE 11 ; Task 11  
L X ShowError Kernel Failed. TASK problem, should be at TASK 11  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P  
L X Skip 1  
L X ShowError Timed out  
; For the next task  
L A19 SkipE 13 ; Task 13  
L X ShowError Kernel Failed. TASK problem, should be at TASK 13  
L X TimeOut 30000; 12 sec  
L X Proceed ; ;P  
L X Skip 1  
L X ShowError Timed out

```

; For the next task
L A19 SkipE 14 ; Task 14
L X ShowError Kernel Failed. TASK problem, should be at TASK 14
L X TimeOut 30000; 12 sec
L X Proceed ; ;P
L X Skip 1
L X ShowError Timed out
; For the next task
L A19 SkipE 15 ; Task 15
L X ShowError Kernel Failed. TASK problem, should be at TASK 15
L X TimeOut 30000; 12 sec
L X Proceed ; ;P
L X Skip 1
L X ShowError Timed out
; For the next task
L A19 SkipE 16 ; Task 16
L X ShowError Kernel Failed. TASK problem, should be at TASK 16
L X TimeOut 30000; 12 sec
L X Proceed ; ;P
L X Skip 1
L X ShowError Timed out
; For the next task
L A19 SkipE 17 ; Task 17
L X ShowError Kernel Failed. TASK problem, should be at TASK 17
L X TimeOut 30000; 12 sec
L X Proceed ; ;P
L X Skip 1
L X ShowError Timed out
; For the next task
L A19 SkipE 0 ; Task 0
L X ShowError Kernel Failed. TASK problem, should be at TASK 0

```

### 23. VoltageTest.Midas

```

;Voltage test
;By Frank Vest
;February 28, 1984 10:00 AM

```

```

;+12 VOLTS MIN AND MAX (Normal voltage)

```

```

L B0 Addr $ABSOLUTE 2
L B0 SkipGE BA; 11.51
L X ShowError +12 Volts too low (11.51 min.)
L B0 SkipLE CA ; 12.50
L X ShowError +12 Volts too high (12.50 max.)

```

```

;+5 VOLTS MIN AND MAX

```

```

L B0 Addr $ABSOLUTE 3
L B0 SkipGE B8 ; 4.82
L X ShowError +5 Volts too low (4.82 min.)
L B0 SkipLE C6 ; 5.19
L X ShowError +5 Volts too high (5.19 max.)

```

```

;-2 VOLTS MIN AND MAX

```

```

L B0 Addr $ABSOLUTE 4

```

L B0 SkipGE BB ; 1.89  
 L X ShowError -2 Volts too low (1.89 min.)  
 L B0 SkipLE D0 ; 2.10  
 L X ShowError -2 Volts too high (2.10 max.)

## ;-5.2 VOLTS MIN AND MAX

L B0 Addr \$ABSOLUTE 5  
 L B0 SkipGE C3 ; 5.05  
 L X ShowError -5.2 Volts too low (5.05 min.)  
 L B0 SkipLE CF ; 5.36  
 L X ShowError -5.2 Volts too high (5.36 max.)

## ;+12 VOLTS MIN AND MAX (Maximum voltages read)

L B0 Addr \$ABSOLUTE 3E  
 L B0 SkipGE BA; 11.51  
 L X ShowError MAXVOLTS +12 Volts too low (11.51 min.)  
 L B0 SkipLE CA ; 12.50  
 L X ShowError MAXVOLTS +12 Volts too high (12.50 max.)

## ;+5 VOLTS MIN AND MAX

L B0 Addr \$ABSOLUTE 3F  
 L B0 SkipGE B8 ; 4.82  
 L X ShowError MAXVOLTS +5 Volts too low (4.82 min.)  
 L B0 SkipLE C6 ; 5.19  
 L X ShowError MAXVOLTS +5 Volts too high (5.19 max.)

## ;-2 VOLTS MIN AND MAX

L B0 Addr \$ABSOLUTE 40  
 L B0 SkipGE BB ; 1.89  
 L X ShowError MAXVOLTS -2 Volts too low (1.89 min.)  
 L B0 SkipLE D0 ; 2.10  
 L X ShowError MAXVOLTS -2 Volts too high (2.10 max.)

## ;-5.2 VOLTS MIN AND MAX

L B0 Addr \$ABSOLUTE 41  
 L B0 SkipGE C3 ; 5.05  
 L X ShowError MAXVOLTS -5.2 Volts too low (5.05 min.)  
 L B0 SkipLE CF ; 5.36  
 L X ShowError MAXVOLTS -5.2 Volts too high (5.36 max.)

## ;+12 VOLTS MIN AND MAX ( Min. voltages read)

L B0 Addr \$ABSOLUTE 2A  
 L B0 SkipGE BA; 11.51  
 L X ShowError MINVOLTS +12 Volts too low (11.51 min.)  
 L B0 SkipLE CA ; 12.50  
 L X ShowError MINVOLTS +12 Volts too high (12.50 max.)

## ;+5 VOLTS MIN AND MAX

L B0 Addr \$ABSOLUTE 2B  
 L B0 SkipGE B8 ; 4.82  
 L X ShowError MINVOLTS +5 Volts too low (4.82 min.)  
 L B0 SkipLE C6 ; 5.19  
 L X ShowError MINVOLTS +5 Volts too high (5.19 max.)  
 ; L X ShowError MINVOLTS +5 Volts ok.; For debugging

## ;-2 VOLTS MIN AND MAX

L B0 Addr \$ABSOLUTE 2C  
 L B0 SkipGE BB ; 1.89  
 L X ShowError MINVOLTS -2 Volts too low (1.89 min.)  
 L B0 SkipLE D0 ; 2.10  
 L X ShowError MINVOLTS -2 Volts too high (2.10 max.)

## ;-5.2 VOLTS MIN AND MAX

L B0 Addr \$ABSOLUTE 2D  
 L B0 SkipGE C3 ; 5.05  
 L X ShowError MINVOLTS -5.2 Volts too low (5.05 min.)  
 L B0 SkipLE CF ; 5.36  
 L X ShowError MINVOLTS -5.2 Volts too high (5.36 max.)

**24. CurrentTest.Midas**

;Current test  
 ;By Frank Vest  
 ;February 28, 1984 10:01 AM

## ;+12 VOLTS MIN AND MAX (Normal Current)

L B0 Addr \$ABSOLUTE 6  
 L B0 SkipGE 0; 0 amps  
 L X ShowError +12 Current too low (AMPS "0" Amps min.)  
 L B0 SkipLE 10 ; 3 amps  
 L X ShowError +12 Current too high (AMPS "3" Amps max.)

## ;+5 VOLTS MIN AND MAX CURRENT CHECK

L B0 Addr \$ABSOLUTE 7  
 L B0 SkipGE 1 ; 3 amps  
 L X ShowError +5 Current too low (AMPS "3" Amps min.)  
 L B0 SkipLE 17 ; 61 amps  
 L X ShowError +5 Current too high (AMPS "61" Amps max.)

## ;-2 VOLTS MIN AND MAX CURRENT CHECK

L B0 Addr \$ABSOLUTE 8  
 L B0 SkipGE 10 ; 41 amps  
 L X ShowError -2 Current too low (AMPS "41" Amps min.)  
 L B0 SkipLE 1B ; 69 amps  
 L X ShowError -2 Current too high (AMPS "69" Amps max.)

## ;-5.2 VOLTS MIN AND MAX CURRENT CHECK

L B0 Addr \$ABSOLUTE 9  
 L B0 SkipGE 28 ; 151 amps  
 L X ShowError -5.2 Current too low (AMPS "151" Amps min.)  
 L B0 SkipLE 3B ; 222 amps  
 L X ShowError -5.2 Current too high (AMPS "222" Amps max.)

## ;+12 VOLTS CURRENT CHECK (MINAMPS)

L B0 Addr \$ABSOLUTE 2E  
 L B0 SkipGE 0; 0 amps  
 L X ShowError +12 Current too low (MINAMPS "0" Amps min.)  
 L B0 SkipLE 10 ; 3 amps  
 L X ShowError +12 Current too high (MINAMPS)

## ;+5 VOLTS CURRENT CHECK (MINAMPS)

```

L B0 Addr $ABSOLUTE 2F
L B0 SkipGE 0 ; 0 amps
L X ShowError +5 Current too low (MINAMPS "0" Amps min.)
L B0 SkipLE 17 ; 61 amps
L X ShowError +5 Current too high (MINAMPS)

```

## ;-2 VOLTS CURRENT CHECK (MINAMPS)

```

L B0 Addr $ABSOLUTE 30
L B0 SkipGE 10 ; 41 amps
L X ShowError -2 Current too low (MINAMPS "41" Amps min.)
L B0 SkipLE 1B ; 69 amps
L X ShowError -2 Current too high (MINAMPS)

```

## ;-5.2 VOLTS CURRENT CHECK (MINAMPS)

```

L B0 Addr $ABSOLUTE 31
L B0 SkipGE 28 ; 151 amps
L X ShowError -5.2 Current too low (MINAMPS "151" Amps min.)
L B0 SkipLE 3B ; 222 amps
L X ShowError -5.2 Current too high (MINAMPS)

```

## ;+12 VOLTS CURRENT CHECK (MAXAMPS)

```

L B0 Addr $ABSOLUTE 42
L B0 SkipGE 0; 0 amps
L X ShowError +12 Current too low (MAXAMPS)
L B0 SkipLE 10 ; 3 amps
L X ShowError +12 Current too high (MAXAMPS "3" Amps max.)

```

## ;+5 VOLTS CURRENT CHECK (MAXAMPS)

```

L B0 Addr $ABSOLUTE 43
L B0 SkipGE 1 ; 3 amps
L X ShowError +5 Current too low (MAXAMPS)
L B0 SkipLE 17 ; 61 amps
L X ShowError +5 Current too high (MAXAMPS "61" Amps max.)

```

## ;-2 VOLTS CURRENT CHECK (MAXAMPS)

```

L B0 Addr $ABSOLUTE 44
L B0 SkipGE 10 ; 41 amps
L X ShowError -2 Current too low (MAXAMPS)
L B0 SkipLE 1B ; 69 amps
L X ShowError -2 Current too high (MAXAMPS "69" Amps max.)

```

## ;-5.2 VOLTS CURRENT CHECK (MAXAMPS)

```

L B0 Addr $ABSOLUTE 45
L B0 SkipGE 28 ; 151 amps
L X ShowError -5.2 Current too low (MAXAMPS)
L B0 SkipLE 3B ; 222 amps
L X ShowError -5.2 Current too high (MAXAMPS "222" Amps max.)

```

**25. TemperatureTest.Midas**

;Temperature test

;By Frank Vest

;February 24, 1984 10:05 AM

;Temperature test

;Baseboard

L B0 Addr \$ABSOLUTE A  
L B0 SkipGE 94; 17 Degrees C  
L X ShowError BaseBoard temperature too low (17 Degrees C min.)  
L B0 SkipLE A0 ; 41  
L X ShowError BaseBoard temperature high (41 Degrees C max.)

;ContB board

L B0 Addr \$ABSOLUTE B  
L B0 SkipGE 94; 17 Degrees C  
L X ShowError ContB Board temperature too low (17 Degrees C min.)  
L B0 SkipLE A0 ; 41  
L X ShowError ContB Board temperature high (41 Degrees C max.)

;ProcL board

L B0 Addr \$ABSOLUTE D  
L B0 SkipGE 94; 17 Degrees C  
L X ShowError ProcL board temperature too low (17 Degrees C min.)  
L B0 SkipLE A0 ; 41  
L X ShowError ProcL board temperature high (41 Degrees C max.)

;ProcH board

L B0 Addr \$ABSOLUTE E  
L B0 SkipGE 94; 17 Degrees C  
L X ShowError ProcH board temperature too low (17 Degrees C min.)  
L B0 SkipLE A0 ; 41  
L X ShowError ProcH board temperature high (41 Degrees C max.)

;IFU board

L B0 Addr \$ABSOLUTE F  
L B0 SkipGE 94; 17 Degrees C  
L X ShowError IFU board temperature too low (17 Degrees C min.)  
L B0 SkipLE A0 ; 41  
L X ShowError IFU board temperature high (41 Degrees C max.)

;MemD board

L B0 Addr \$ABSOLUTE 12  
L B0 SkipGE 94; 17 Degrees C  
L X ShowError MemD board temperature too low (17 Degrees C min.)  
L B0 SkipLE A0 ; 41  
L X ShowError MemD board temperature high (41 Degrees C max.)

;DSK/ETH board

L B0 Addr \$ABSOLUTE 13  
L B0 SkipGE 94; 17 Degrees C  
L X ShowError DSK/ETH board temperature too low (17 Degrees C min.)  
L B0 SkipLE A0 ; 41  
L X ShowError DSK/ETH board temperature high (41 Degrees C max.)

;Temperature test for "Max" temperature ever logged.

;Baseboard

L B0 Addr \$ABSOLUTE 46  
L B0 SkipGE 94; 17 Degrees C

```

L X ShowError BaseBoard "MAXTEMP" too low (17 Degrees C min.)
L B0 SkipLE A0 ; 41
L X ShowError BaseBoard "MAXTEMP" high (41 Degrees C max.)

```

## ;ContB board

```

L B0 Addr $ABSOLUTE 47
L B0 SkipGE 94; 17 Degrees C
L X ShowError ContB Board "MAXTEMP" too low (17 Degrees C min.)
L B0 SkipLE A0 ; 41
L X ShowError ContB Board "MAXTEMP" high (41 Degrees C max.)

```

## ;ProcL board

```

L B0 Addr $ABSOLUTE 49
L B0 SkipGE 94; 17 Degrees C
L X ShowError ProcL board "MAXTEMP" too low (17 Degrees C min.)
L B0 SkipLE A0 ; 41
L X ShowError ProcL board "MAXTEMP" high (41 Degrees C max.)

```

## ;ProcH board

```

L B0 Addr $ABSOLUTE 4A
L B0 SkipGE 94; 17 Degrees C
L X ShowError ProcH board "MAXTEMP" too low (17 Degrees C min.)
L B0 SkipLE A0 ; 41
L X ShowError ProcH board "MAXTEMP" high (41 Degrees C max.)

```

## ;IFU board

```

L B0 Addr $ABSOLUTE 4B
L B0 SkipGE 94; 17 Degrees C
L X ShowError IFU board "MAXTEMP" too low (17 Degrees C min.)
L B0 SkipLE A0 ; 41
L X ShowError IFU board "MAXTEMP" high (41 Degrees C max.)

```

## ;MemD board

```

L B0 Addr $ABSOLUTE 4E
L B0 SkipGE 94; 17 Degrees C
L X ShowError MemD board "MAXTEMP" too low (17 Degrees C min.)
L B0 SkipLE A0 ; 41
L X ShowError MemD board "MAXTEMP" high (41 Degrees C max.)

```

## ;DSK/ETH board

```

L B0 Addr $ABSOLUTE 4F
L B0 SkipGE 94; 17 Degrees C
L X ShowError DSK/ETH board "MAXTEMP" too low (17 Degrees C min.)
L B0 SkipLE A0 ; 41
L X ShowError DSK/ETH board "MAXTEMP" high (41 Degrees C max.)

```

**26. VIT.Midas**

```

L X RdCmds VOLTAGETEST
L X RdCmds CURRENTTEST
L X RdCmds TEMPERATURETEST

```

## 27. TestAllGarage.Midas

L X RdCmds  
L X TESTS

L C9 Val 10000  
L X Test  
L X RANDOM  
L X TimeOut 60000; 24 sec  
L X VM  
L X ShowError "VM" FAILED (VIRTUAL MEMORY) MEMORY SYSTEM BROKEN. RUN "MEMA" AND "MEMMISC".  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 10000  
L X CPREG  
L X ShowError "CP" REG FAILED (Control Processor) PG. 6 thru 19 ContA Board (Baseboard?)  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 10000  
L X MIR  
L X ShowError "MIR" FAILED (MIRCROINSTRUCTION REGISTER) PG. 1 CONTA, PG.1-2-3 CONTB BOARD  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 10000  
L X Q  
L X ShowError "Q" REG FAILED. BITS 0-7 PG.17 PROCH BOARD, BITS 8-15 PG.17 PROCL BOARD  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 10000  
L X CNT  
L X ShowError "CNT"REG FAILED(COUNT REGISTER)BITS 0-7 PG.17 PROCH, BITS 8-15 PG.17 PROCL  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 10000  
L X SHC  
L X ShowError "SHC" FAILED (SHIFT CONTROL) BITS 0-7 PG.18 PROCH, BITS 8-15 PG.18 PROCL  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 10000  
L X MEMBX  
L X ShowError "MEMBX" FAILED. (MEM BASE INDEX) PG.24 PROCH BOARD  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 10000  
L X STKP  
L X ShowError "STKP" FAILED. (STACK POINTER) PG.25 PROCL BOARD  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 10000  
L X TASK  
L X ShowError "TASK" REG FAILED. PG. 26 CONTA BOARD  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 10000  
L X PROCSRN  
L X ShowError "PROCSRN" FAILED. (PROCESSOR STORAGE REFERENCE NUMBER) PG. 3 MEMX BOARD  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 10000  
L X MCR  
L X ShowError "MCR" REG FAILED (MEMORY CONTROL REGISTER) PG. 4, 5 MEMC BOARD  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 10000  
L X INSSET  
L X ShowError "INSSET" FAILED (INSTRUCTION SET) PG. 4 IFU BOARD  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 10000  
L X EVCNTB  
L X ShowError "EVENTB" FAILED (EVENT COUNTER B) PG. 14 IFU BOARD  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 10000  
L X ESTAT  
L X ShowError "ESTAT" FAILED. (ERROR STATUS) PG.9 CONTB BOARD  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 20000  
L X TPC  
L X ShowError "TPC" FAILED. (TASK PROGRAM COUNTER) PG.6 THRU 19 CONTA BOARD  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 20000  
L X TLINK  
L X ShowError "TLINK" FAILED (TEMPORARY LINK REGISTER) PG.6 THRU 19 CONTA BOARD  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 100000  
L X IMX  
L X ShowError "IMX" FAILED. (INSTRUCTION MEMORY) CONTB BOARD  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 100000  
L X IMBD  
L X ShowError "IMBD" FAILED. (INSTRUCTION MEMORY BDUMX) PG. 12 CONTB BOARD  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 10000  
L X ALUFM  
L X ShowError "ALUFM" FAILED.(ARITHMETIC LOGIC UNIT FUNTION MEMORY)PG.11  
PROCL(ALUFDEC)  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 10000  
L X T  
L X ShowError "T" FAILED(TEMPORARY STORAGE)BITS 0-7 PG.2-9 PROCH, BITS 8-16 PG.2-9 PROCL  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 10000  
L X RBASE  
L X ShowError "RBASE" FAILED (REGISTER MEMORY BASE) PG. 23 PROCL BOARD  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 10000  
L X TIOA  
L X ShowError "TIOA" FAILED (TASK INPUT/OUTPUT ADDRESS) PG. 23 PROCH BOARD  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 10000  
L X MEMBASE  
L X ShowError "MEMBASE" FAILED (MEMORY BASE) PG. 25 PROCH BOARD  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 20000  
L X RM  
L X ShowError "RM" FAILED(REGISTER MEMORY)BITS 0-7 PG.2-9 PROCH, BITS 8-16 PG.2-9 PROCL  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 70000  
L X CACHEA  
L X ShowError "CACHEA" FAILED (CACHE ADDRESS) PG. 11 AND 12 OF THE MEMC BOARD  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 200000  
L X CACHED  
L X ShowError "CACHED" FAILED (CACHE DATA) MEMD BOARD  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 1000000  
L X MAP  
L X ShowError "MAP" FAILED (MEMORY MAP) PG. 12 AND 13 OF THE MEMX BOARD  
L X Skip 1  
L X Abort

L X Test

L X RANDOM  
L X TimeOut 70000  
L X IFUM  
L X ShowError "IFUM" FAILED (INSTRUCTION FETCH UNIT MEMORY) PG.6 IFU BOARD  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 10000  
L X Shmv  
L X ShowError "SHMV" FAILED (SHIFTER MASK VECTOR) BITS 0-7 PG.16 PROCH, BITS 8-15 PG 16 PROCL  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 10000  
L X WF  
L X ShowError "WF" FAILED (MESA WRITE FIELD) PG. 18 PROCH, PG. 18 PROCL BOARDS  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 10000  
L X RF  
L X ShowError "RF" FAILED (MESA READ FIELD) PG. 18 PROCH, PG. 18 PROCL BOARDS  
L X Skip 1  
L X Abort

L X Test  
L X RANDOM  
L X TimeOut 10000  
L X ProcVA  
L X ShowError "ProcVA" FAILED (PROCESSOR VIRTUAL ADDRESS) PG. 1,7,8,9, AND 10 MEMC BOARD  
L X Skip 1  
L X Abort

## 28. Acceptance Tests. Midas

; Written by Frank Vest  
; December 9, 1983 2:52 PM  
; L X DisplayOff  
L X Reset  
L X Do-it  
L X DisplayOff  
L X RdCmds VOLTAGETEST  
L X RdCmds CURRENTTEST  
L X RdCmds TEMPERATURETEST  
L X Reset  
L X Do-it  
L X RdCmds TESTALLGARAGE

; Run all of the microdiagnostics at 30  
L X SetClk

```

L X 30
L X RdCmds KERNELTASK
L A6 SkipE DONE+1
L X ShowError KERNEL "Task test" Failed at 30 Nanoseconds
L X RunProg
L X MEMMISC
L A6 SkipE DONE+1
L X ShowError MEMMISC Failed at 30 Nanoseconds
L X RunProg
L X IFUSIMPLE
L A6 SkipE DONE+1
L X ShowError IFUSIMPLE Failed at 30 Nanoseconds
L X RunProg
L X IFUCOMPLEX
L A6 SkipE DONE+1
L X ShowError IFUCOMPLEX Failed at 30 Nanoseconds
L X RunProg
L X EVENTCOUNTERS
L A6 SkipE DONE+1
L X ShowError EVENTCOUNTERS Failed at 30 Nanoseconds
L X RunProg
L X MEMA
L A6 SkipE DONE+1
L X ShowError MEMA Failed at 30 Nanoseconds
L X RunProg
L X TRICOND
L A6 SkipE DONE+1
L X ShowError TRICOND Failed at 30 Nanoseconds

```

```

; Now run a 2 minute simtest. We will log up to 5 errors
; Remove the known simtest bugs

```

```

L X DisplayOff
L B19 Addr CJNK3
LR X DMux
L B19 Val 177774 ; get rid of bSwitch'a/A failures
L X RdCmds
L X ifud
M B7 Val
LR X DMux ; Get rid of the DSel0 and the DSel1 errors
L B7 Val 177477; Get rid of the DSel0 and the DSel1 errors
L B10 Addr HIT
LR X DMux
L B10 Val 177477 ; get rid of ColVic.0 and ColVic.1
L X RdCmds
L X mmx
LR X DMux
L B6 Val 167777 ; get rid of STWait-Mem'X errors

```

```

;Now run the simtest for 2 minutes

```

```

L X TimeOut 400000
L X SimTest
L X Skip .Error
L X Skip .Complete
L X OpenOutput SIMERROR

```

```

L X WriteMessage ~Simulator dump on\
L X WriteDT
M X DMux ; Put failures on comment line
L X DumpDisplay ; Print 1st 5 simulation failures

L X TimeOut 400000 ; Start over must run for 2 minutes
L X SimTest
L X Skip .Error1
L X Skip .Complete1
.Error1 M X DMux ; Put failures on comment line
L X DumpDisplay ; Print 1st 5 simulation failures

L X TimeOut 400000 ; Start over must run for 2 minutes
L X SimTest
L X Skip .Error2
L X Skip .Complete2
.Error2 M X DMux ; Put failures on comment line
L X DumpDisplay ; Print 1st 5 simulation failures

L X TimeOut 400000 ; Start over must run for 2 minutes
L X SimTest
L X Skip .Error3
L X Skip .Complete3
.Error3 M X DMux ; Put failures on comment line
L X DumpDisplay ; Print 1st 5 simulation failures

L X TimeOut 400000 ; Start over must run for 2 minutes
L X SimTest
L X Skip .Error4
L X Skip .Complete4
.Error4 M X DMux ; Put failures on comment line
L X DumpDisplay ; Print 1st 5 simulation failures

L X TimeOut 400000 ; Start over must run for 2 minutes
L X SimTest
L X Skip .Error5
L X Skip .Complete5
.Error5 M X DMux ; Put failures on comment line
L X DumpDisplay ; Print 1st 5 simulation failures

.Complete L X CloseOutput
L X ShowError Acceptance tests complete with no errors. Clocks were set to 30 ns.

.Complete1 L X CloseOutput
L X ShowError Acceptance tests complete, 1 Simtest error. Clk. set to 30 ns.

.Complete2 L X CloseOutput
L X ShowError Acceptance tests complete, 2 Simtest errors. Clk. set to 30 ns.

.Complete3 L X CloseOutput
L X ShowError Acceptance tests complete, 3 Simtest errors. Clk. set to 30 ns.

.Complete4 L X CloseOutput
L X ShowError Acceptance tests complete, 4 Simtest errors. Clk. set to 30 ns.

```

.Complete5 L X CloseOutput  
 L X ShowError Acceptance tests complete, 5 Simtest errors. Clk. set to 30 ns.

## 29. MapAddr.Midas

```
; Written by Frank Vest
; December 9, 1983 1:04 PM
L B0 Addr MAP 0
L B1 Addr MAP 1
L B2 Addr MAP 2
L B3 Addr MAP 4
L B4 Addr MAP 10
L B5 Addr MAP 20
L B6 Addr MAP 40
L B7 Addr MAP 100
L B8 Addr MAP 200
L B9 Addr MAP 400
L B10 Addr MAP 1000
L B11 Addr MAP 2000
L B12 Addr MAP 4000
L B13 Addr MAP 10000
L B14 Addr MAP 20000
L B15 Addr MAP 40000
L B16 Addr MAP 100000
L B0 Val 0
L B1 Val 1
L B2 Val 2
L B3 Val 4
L B4 Val 10
L B5 Val 20
L B6 Val 40
L B7 Val 100
L B8 Val 200
L B9 Val 400
L B10 Val 1000
L B11 Val 2000
L B12 Val 4000
L B13 Val 10000
L B14 Val 20000
L B15 Val 40000
L B16 Val 100000
;Now check for correct values.
L B0 SkipE 2 0 0 ; Value for MAP 0
L X ShowError Value for MAP 0 wrong should be "2 0 000000".
L B1 SkipE 1 ; Value for MAP 1
L X ShowError Value for MAP 1 wrong should be "1".
L B2 SkipE 2 ; Value for MAP 2
L X ShowError Value for MAP 2 wrong should be "2".
L B3 SkipE 4 ; Value for MAP 4
L X ShowError Value for MAP 4 wrong should be "4".
L B4 SkipE 10 ; Value for MAP 10
L X ShowError Value for MAP 10 wrong should be "10".
L B5 SkipE 20 ; Value for MAP 20
L X ShowError Value for MAP 20 wrong should be "20".
L B6 SkipE 40 ; Value for MAP 40
```

L X ShowError Value for MAP 40 wrong should be "40".  
 L B7 SkipE 100 ; Value for MAP 100  
 L X ShowError Value for MAP 100 wrong should be "100".  
 L B8 SkipE 200 ; Value for MAP 200  
 L X ShowError Value for MAP 200 wrong should be "200".  
 L B9 SkipE 400 ; Value for MAP 400  
 L X ShowError Value for MAP 400 wrong should be "400".  
 L B10 SkipE 1000 ; Value for MAP 1000  
 L X ShowError Value for MAP 1000 wrong should be "1000".  
 L B11 SkipE 2000 ; Value for MAP 2000  
 L X ShowError Value for MAP 2000 wrong should be "2000".  
 L B12 SkipE 4000 ; Value for MAP 4000  
 L X ShowError Value for MAP 4000 wrong should be "4000".  
 L B13 SkipE 10000 ; Value for MAP 10000  
 L X ShowError Value for MAP 10000 wrong should be "10000".  
 L B14 SkipE 20000 ; Value for MAP 20000  
 L X ShowError Value for MAP 20000 wrong should be "20000".  
 L B15 SkipE 40000 ; Value for MAP 40000  
 L X ShowError Value for MAP 40000 wrong should be "40000".  
 L B16 SkipE 100000 ; Value for MAP 100000  
 L X ShowError Value for MAP 100000 wrong should be "100000".

### 30. CacheDAddr.Midas

; Written by Frank Vest  
 ; December 9, 1983December 9, 1983 1:12 PM 1:12 PM  
 L B0 Addr CACHED 0  
 L B1 Addr CACHED 1  
 L B2 Addr CACHED 2  
 L B3 Addr CACHED 4  
 L B4 Addr CACHED 10  
 L B5 Addr CACHED 20  
 L B6 Addr CACHED 40  
 L B7 Addr CACHED 100  
 L B8 Addr CACHED 200  
 L B9 Addr CACHED 400  
 L B10 Addr CACHED 1000  
 L B11 Addr CACHED 2000  
 L B12 Addr CACHED 4000  
 L B13 Addr CACHED 6000  
 L B0 Val 0  
 L B1 Val 1  
 L B2 Val 2  
 L B3 Val 4  
 L B4 Val 10  
 L B5 Val 20  
 L B6 Val 40  
 L B7 Val 100  
 L B8 Val 200  
 L B9 Val 400  
 L B10 Val 1000  
 L B11 Val 2000  
 L B12 Val 4000  
 L B13 Val 6000  
 L C0 Addr CACHED 0

L C1 Addr CACHED 1  
 L C2 Addr CACHED 3  
 L C3 Addr CACHED 5  
 L C4 Addr CACHED 11  
 L C5 Addr CACHED 21  
 L C6 Addr CACHED 41  
 L C7 Addr CACHED 101  
 L C8 Addr CACHED 201  
 L C9 Addr CACHED 401  
 L C10 Addr CACHED 1001  
 L C11 Addr CACHED 2001  
 L C12 Addr CACHED 4001  
 L C13 Addr CACHED 6001  
 L C13 Val 6001  
 L C12 Val 4001  
 L C11 Val 2001  
 L C10 Val 1001  
 L C9 Val 401  
 L C8 Val 201  
 L C7 Val 101  
 L C6 Val 41  
 L C5 Val 21  
 L C4 Val 11  
 L C3 Val 5  
 L C2 Val 3  
 L C1 Val 1  
 L C0 Val 0

;Now check for correct values.

L B0 SkipE 0 ; Value for CacheD 0  
 L X ShowError Value for CacheD 0 wrong should be "0".  
 L B1 SkipE 1 ; Value for CacheD 1  
 L X ShowError Value for CacheD 1 wrong should be "1".  
 L B2 SkipE 2 ; Value for CacheD 2  
 L X ShowError Value for CacheD 2 wrong should be "2".  
 L B3 SkipE 4 ; Value for CacheD 4  
 L X ShowError Value for CacheD 4 wrong should be "4".  
 L B4 SkipE 10 ; Value for CacheD 10  
 L X ShowError Value for CacheD 10 wrong should be "10".  
 L B5 SkipE 20 ; Value for CacheD 20  
 L X ShowError Value for CacheD 20 wrong should be "20".  
 L B6 SkipE 40 ; Value for CacheD 40  
 L X ShowError Value for CacheD 40 wrong should be "40".  
 L B7 SkipE 100 ; Value for CacheD 100  
 L X ShowError Value for CacheD 100 wrong should be "100".  
 L B8 SkipE 200 ; Value for CacheD 200  
 L X ShowError Value for CacheD 200 wrong should be "200".  
 L B9 SkipE 400 ; Value for CacheD 400  
 L X ShowError Value for CacheD 400 wrong should be "400".  
 L B10 SkipE 1000 ; Value for CacheD 1000  
 L X ShowError Value for CacheD 1000 wrong should be "1000".  
 L B11 SkipE 2000 ; Value for CacheD 2000  
 L X ShowError Value for CacheD 2000 wrong should be "2000".  
 L B12 SkipE 4000 ; Value for CacheD 4000  
 L X ShowError Value for CacheD 4000 wrong should be "4000".  
 L B13 SkipE 6000 ; Value for CacheD 60000  
 L X ShowError Value for CacheD 60000 wrong should be "60000".

;Now check for the rest of the CacheD values.

L C0 SkipE 0 ; Value for CacheD 0  
 L X ShowError Value for CacheD 0 wrong should be "0".  
 L C1 SkipE 1 ; Value for CacheD 1  
 L X ShowError Value for CacheD 1 wrong should be "1".  
 L C2 SkipE 3 ; Value for CacheD 3  
 L X ShowError Value for CacheD 3 wrong should be "3".  
 L C3 SkipE 5 ; Value for CacheD 5  
 L X ShowError Value for CacheD 5 wrong should be "5".  
 L C4 SkipE 11 ; Value for CacheD 11  
 L X ShowError Value for CacheD 11 wrong should be "11".  
 L C5 SkipE 21 ; Value for CacheD 21  
 L X ShowError Value for CacheD 21 wrong should be "21".  
 L C6 SkipE 41 ; Value for CacheD 41  
 L X ShowError Value for CacheD 41 wrong should be "41".  
 L C7 SkipE 101 ; Value for CacheD 101  
 L X ShowError Value for CacheD 101 wrong should be "101".  
 L C8 SkipE 201 ; Value for CacheD 201  
 L X ShowError Value for CacheD 201 wrong should be "201".  
 L C9 SkipE 401 ; Value for CacheD 401  
 L X ShowError Value for CacheD 401 wrong should be "401".  
 L C10 SkipE 1001 ; Value for CacheD 1001  
 L X ShowError Value for CacheD 1001 wrong should be "1001".  
 L C11 SkipE 2001 ; Value for CacheD 2001  
 L X ShowError Value for CacheD 2001 wrong should be "2001".  
 L C12 SkipE 4001 ; Value for CacheD 4001  
 L X ShowError Value for CacheD 4001 wrong should be "4001".  
 L C13 SkipE 6001 ; Value for CacheD 60001  
 L X ShowError Value for CacheD 60001 wrong should be "60001".

### 31. CacheAAddr.Midas

; Written by Frank VEst  
 ; December 5, 1983 1:06 PM

L B0 Addr CACHEA 0  
 L B1 Addr CACHEA 1  
 L B2 Addr CACHEA 2  
 L B3 Addr CACHEA 4  
 L B4 Addr CACHEA 10  
 L B5 Addr CACHEA 20  
 L B6 Addr CACHEA 40  
 L B7 Addr CACHEA 100  
 L B8 Addr CACHEA 200  
 L B0 Val 0  
 L B1 Val 1  
 L B2 Val 2  
 L B3 Val 4  
 L B4 Val 10  
 L B5 Val 20  
 L B6 Val 40  
 L B7 Val 100  
 L B8 Val 200

;Now check for correct values.

L B0 SkipE 0 ; Value for CacheA 0  
 L X ShowError Value for CacheA 0 wrong should be "0".  
 L B1 SkipE 1 ; Value for CacheA 1  
 L X ShowError Value for CacheA 1 wrong should be "1".

L B2 SkipE 2 ; Value for CacheA 2  
 L X ShowError Value for CacheA 2 wrong should be "2".  
 L B3 SkipE 4 ; Value for CacheA 4  
 L X ShowError Value for CacheA 4 wrong should be "4".  
 L B4 SkipE 10 ; Value for CacheA 10  
 L X ShowError Value for CacheA 10 wrong should be "10".  
 L B5 SkipE 20 ; Value for CacheA 20  
 L X ShowError Value for CacheA 20 wrong should be "20".  
 L B6 SkipE 40 ; Value for CacheA 40  
 L X ShowError Value for CacheA 40 wrong should be "40".  
 L B7 SkipE 100 ; Value for CacheA 100  
 L X ShowError Value for CacheA 100 wrong should be "100".  
 L B8 SkipE 200 ; Value for CacheA 200  
 L X ShowError Value for CacheA 200 wrong should be "200".

### 32. StkAddr.Midas

; Written by Frank Vest  
 ; December 9, 1983 12:37 PM  
 L B0 Addr STK 0  
 L B1 Addr STK 1  
 L B2 Addr STK 2  
 L B3 Addr STK 4  
 L B4 Addr STK 10  
 L B5 Addr STK 20  
 L B6 Addr STK 40  
 L B7 Addr STK 100  
 L B8 Addr STK 200  
 L B0 Val 0  
 L B1 Val 401  
 L B2 Val 1002  
 L B3 Val 2004  
 L B4 Val 4010  
 L B5 Val 10020  
 L B6 Val 20040  
 L B7 Val 40100  
 L B8 Val 100200  
 ;Now check for correct values.  
 L B0 SkipE 0 ; Value for STK 0  
 L X ShowError Value for STK 0 wrong should be "0".  
 L B1 SkipE 401 ; Value for STK 1  
 L X ShowError Value for STK 1 wrong should be "401".  
 L B2 SkipE 1002 ; Value for STK 2  
 L X ShowError Value for STK 2 wrong should be "1002".  
 L B3 SkipE 2004 ; Value for STK 4  
 L X ShowError Value for STK 4 wrong should be "2004".  
 L B4 SkipE 4010 ; Value for STK 10  
 L X ShowError Value for STK 10 wrong should be "4010".  
 L B5 SkipE 10020 ; Value for STK 20  
 L X ShowError Value for STK 20 wrong should be "10020".  
 L B6 SkipE 20040 ; Value for STK 40  
 L X ShowError Value for STK 40 wrong should be "20040".  
 L B7 SkipE 40100 ; Value for STK 100  
 L X ShowError Value for STK 100 wrong should be "40100".  
 L B8 SkipE 100200 ; Value for STK 200  
 L X ShowError Value for STK 200 wrong should be "100200".

### 33. RMAddr.Midas

```
; Written by Frank Vest
; December 9, 1983 12:35 PM
L B0 Addr RM 0
L B1 Addr RM 1
L B2 Addr RM 2
L B3 Addr RM 4
L B4 Addr RM 10
L B5 Addr RM 20
L B6 Addr RM 40
L B7 Addr RM 100
L B8 Addr RM 200
L B0 Val 0
L B1 Val 401
L B2 Val 1002
L B3 Val 2004
L B4 Val 4010
L B5 Val 10020
L B6 Val 20040
L B7 Val 40100
L B8 Val 100200
;Now check for correct values.
L B0 SkipE 0 ; Value for RM 0
L X ShowError Value for RM 0 wrong should be "0".
L B1 SkipE 401 ; Value for RM 1
L X ShowError Value for RM 1 wrong should be "401".
L B2 SkipE 1002 ; Value for RM 2
L X ShowError Value for RM 2 wrong should be "1002".
L B3 SkipE 2004 ; Value for RM 4
L X ShowError Value for RM 4 wrong should be "2004".
L B4 SkipE 4010 ; Value for RM 10
L X ShowError Value for RM 10 wrong should be "4010".
L B5 SkipE 10020 ; Value for RM 20
L X ShowError Value for RM 20 wrong should be "10020".
L B6 SkipE 20040 ; Value for RM 40
L X ShowError Value for RM 40 wrong should be "20040".
L B7 SkipE 40100 ; Value for RM 100
L X ShowError Value for RM 100 wrong should be "40100".
L B8 SkipE 100200 ; Value for RM 200
L X ShowError Value for RM 200 wrong should be "100200".
```

### 34. IMXAddr.Midas

```
; Written by Frank Vest
; February 28, 1984 12:47 PM
L C0 Addr IMX 0
L C1 Addr IMX 1
L C2 Addr IMX 2
L C3 Addr IMX 4
L C4 Addr IMX 10
L C5 Addr IMX 20
L C6 Addr IMX 40
L C7 Addr IMX 100
```

```

L C8 Addr IMX 200
L C9 Addr IMX 400
L C10 Addr IMX 1000
L C11 Addr IMX 2000
L C12 Addr IMX 4000
L C0 Val 0
L C1 Val 1
L C2 Val 2
L C3 Val 4
L C4 Val 10
L C5 Val 20
L C6 Val 40
L C7 Val 100
L C8 Val 200
L C9 Val 400
L C10 Val 1000
L C11 Val 2000
L C12 Val 4000
;Now check for correct values.
L C0 SkipE 0 ; Value for IMX 0
L X ShowError Value for IMX 0 wrong should be "0" ContB board.
L C1 SkipE 1 ; Value for IMX 1
L X ShowError Value for IMX 1 wrong should be "1" ContB board.
L C2 SkipE 2 ; Value for IMX 2
L X ShowError Value for IMX 2 wrong should be "2" ContB board.
L C3 SkipE 4 ; Value for IMX 4
L X ShowError Value for IMX 4 wrong should be "4" ContB board.
L C4 SkipE 10 ; Value for IMX 10
L X ShowError Value for IMX 10 wrong should be "10" ContB board.
L C5 SkipE 20 ; Value for IMX 20
L X ShowError Value for IMX 20 wrong should be "20" ContB board.
L C6 SkipE 40 ; Value for IMX 40
L X ShowError Value for IMX 40 wrong should be "40" ContB board.
L C7 SkipE 100 ; Value for IMX 100
L X ShowError Value for IMX 100 wrong should be "100" ContB board.
L C8 SkipE 200 ; Value for IMX 200
L X ShowError Value for IMX 200 wrong should be "200" ContB board.
L C9 SkipE 400 ; Value for IMX 400
L X ShowError Value for IMX 400 wrong should be "400" ContB board.
L C10 SkipE 1000 ; Value for IMX 1000
L X ShowError Value for IMX 1000 wrong should be "1000" ContB board.
L C11 SkipE 2000 ; Value for IMX 2000
L X ShowError Value for IMX 2000 wrong should be "2000" ContB board.
L C12 SkipE 4000 ; Value for IMX 4000
L X ShowError Value for IMX 4000 wrong should be "4000" ContB board.

```

### 35. IFUMAddr.Midas

```

; Written by Frank Vest
; December 9, 1983 2:42 PM
L B0 Addr IFUM 0
L B1 Addr IFUM 1
L B2 Addr IFUM 2
L B3 Addr IFUM 4
L B4 Addr IFUM 10

```

```

L B5 Addr IFUM 20
L B6 Addr IFUM 40
L B7 Addr IFUM 100
L B8 Addr IFUM 200
L B9 Addr IFUM 400
L B10 Addr IFUM 1000
L B0 Val 0
L B1 Val 1
L B2 Val 2
L B3 Val 4
L B4 Val 10
L B5 Val 20
L B6 Val 40
L B7 Val 100
L B8 Val 200
L B9 Val 400
L B10 Val 1000
;Now check for correct values.
L B0 SkipE 0 ; Value for IFUM 0
L X ShowError Value for IFUM 0 wrong should be "0".
L B1 SkipE 1 ; Value for IFUM 1
L X ShowError Value for IFUM 1 wrong should be "1".
L B2 SkipE 2 ; Value for IFUM 2
L X ShowError Value for IFUM 2 wrong should be "2".
L B3 SkipE 4 ; Value for IFUM 4
L X ShowError Value for IFUM 4 wrong should be "4".
L B4 SkipE 10 ; Value for IFUM 10
L X ShowError Value for IFUM 10 wrong should be "10".
L B5 SkipE 20 ; Value for IFUM 20
L X ShowError Value for IFUM 20 wrong should be "20".
L B6 SkipE 40 ; Value for IFUM 40
L X ShowError Value for IFUM 40 wrong should be "40".
L B7 SkipE 100 ; Value for IFUM 100
L X ShowError Value for IFUM 100 wrong should be "100".
L B8 SkipE 200 ; Value for IFUM 200
L X ShowError Value for IFUM 200 wrong should be "200".
L B9 SkipE 400 ; Value for IFUM 400
L X ShowError Value for IFUM 400 wrong should be "400".
L B10 SkipE 1000 ; Value for IFUM 1000
L X ShowError Value for IFUM 1000 wrong should be "1000".

```

### 36. BRAddr.Midas

```

; Written By Frank Vest
; December 9, 1983 2:40 PM
L B0 Addr BR 0
L B1 Addr BR 1
L B2 Addr BR 2
L B3 Addr BR 4
L B4 Addr BR 10
L B5 Addr BR 20
L B0 Val
L B1 Val 1
L B2 Val 2
L B3 Val 4

```

```

L B4 Val 10
L B5 Val 20
;Now check for correct values.
L B0 SkipE 0 ; Value for BR 0
L X ShowError Value for BR 0 wrong should be "0".
L B1 SkipE 1 ; Value for BR 1
L X ShowError Value for BR 1 wrong should be "1".
L B2 SkipE 2 ; Value for BR 2
L X ShowError Value for BR 2 wrong should be "2".
L B3 SkipE 4 ; Value for BR 4
L X ShowError Value for BR 4 wrong should be "4".
L B4 SkipE 10 ; Value for BR 10
L X ShowError Value for BR 10 wrong should be "10".
L B5 SkipE 20 ; Value for BR 20
L X ShowError Value for BR 20 wrong should be "20".

```

### 37. Klink.Midas

```

; Klink.midas is a special routine for use in diagnosing IFUComplex
; microdiagnostic failures.
; Written by Frank Vest
; November 17, 1984 5:48 PM
L X Abs
L B14 Val
R B13 Val
L B14 Val
L X Virt
M B14 Val

```

### 38. BadChip.Midas

```

; December 3, 1983 3:25 PM
; Last modified by Frank Vest
L X DisplayOff
L X TimeOut 30000; 12 sec
L X Call XGETPIPE4(; Get the syndrome from pipe 4 and put it in "T"
L X Skip 1
L X ShowError Timed out
L X DisplayOff
;Now check for the bad chip.
;Start row "A"
L C7 SkipNE 113440
L X ShowError A-4 chip, odd or top MSA board.
L C7 SkipNE 113316
L X ShowError A-5 chip, odd or top MSA board.
L C7 SkipNE 112713
L X ShowError A-6 chip, odd or top MSA board.
L C7 SkipNE 113117
L X ShowError A-7 chip, odd or top MSA board.
L C7 SkipNE 112512
L X ShowError A-8 chip, odd or top MSA board.
L C7 SkipNE 113016
L X ShowError A-9 chip, odd or top MSA board.
L C7 SkipNE 112413
L X ShowError A-10 chip, odd or top MSA board.

```

L C7 SkipNE 113217  
L X ShowError A-11 chip, odd or top MSA board.  
L C7 SkipNE 112612  
L X ShowError A-12 chip, odd or top MSA board.  
L C7 SkipNE 113357  
L X ShowError A-15 chip, odd or top MSA board.  
L C7 SkipNE 112752  
L X ShowError A-16 chip, odd or top MSA board.  
L C7 SkipNE 113057  
L X ShowError A-17 chip, odd or top MSA board.  
L C7 SkipNE 112452  
L X ShowError A-18 chip, odd or top MSA board.  
L C7 SkipNE 113156  
L X ShowError A-19 chip, odd or top MSA board.  
L C7 SkipNE 112553  
L X ShowError A-20 chip, odd or top MSA board.  
L C7 SkipNE 113256  
L X ShowError A-21 chip, odd or top MSA board.  
L C7 SkipNE 112653  
L X ShowError A-22 chip, odd or top MSA board.  
L C7 SkipNE 112020  
L X ShowError A-23 chip, odd or top MSA board.  
; Start row "B".  
L C7 SkipNE 113040  
L X ShowError B-4 chip, odd or top MSA board.  
L C7 SkipNE 113313  
L X ShowError B-5 chip, odd or top MSA board.  
L C7 SkipNE 112716  
L X ShowError B-6 chip, odd or top MSA board.  
L C7 SkipNE 113112  
L X ShowError B-7 chip, odd or top MSA board.  
L C7 SkipNE 112517  
L X ShowError B-8 chip, odd or top MSA board.  
L C7 SkipNE 113013  
L X ShowError B-9 chip, odd or top MSA board.  
L C7 SkipNE 112416  
L X ShowError B-10 chip, odd or top MSA board.  
L C7 SkipNE 113212  
L X ShowError B-11 chip, odd or top MSA board.  
L C7 SkipNE 112617  
L X ShowError B-12 chip, odd or top MSA board.  
L C7 SkipNE 113352  
L X ShowError B-15 chip, odd or top MSA board.  
L C7 SkipNE 112757  
L X ShowError B-16 chip, odd or top MSA board.  
L C7 SkipNE 113052  
L X ShowError B-17 chip, odd or top MSA board.  
L C7 SkipNE 112457  
L X ShowError B-18 chip, odd or top MSA board.  
L C7 SkipNE 113153  
L X ShowError B-19 chip, odd or top MSA board.  
L C7 SkipNE 112556  
L X ShowError B-20 chip, odd or top MSA board.  
L C7 SkipNE 113253  
L X ShowError B-21 chip, odd or top MSA board.  
L C7 SkipNE 112656  
L X ShowError B-22 chip, odd or top MSA board.

L C7 SkipNE 112420  
L X ShowError B-23 chip, odd or top MSA board.  
; Start row "C".  
L C7 SkipNE 112440  
L X ShowError C-4 chip, odd or top MSA board.  
L C7 SkipNE 113716  
L X ShowError C-5 chip, odd or top MSA board.  
L C7 SkipNE 112313  
L X ShowError C-6 chip, odd or top MSA board.  
L C7 SkipNE 113517  
L X ShowError C-7 chip, odd or top MSA board.  
L C7 SkipNE 112112  
L X ShowError C-8 chip, odd or top MSA board.  
L C7 SkipNE 113416  
L X ShowError C-9 chip, odd or top MSA board.  
L C7 SkipNE 112013  
L X ShowError C-10 chip, odd or top MSA board.  
L C7 SkipNE 113617  
L X ShowError C-11 chip, odd or top MSA board.  
L C7 SkipNE 112212  
L X ShowError C-12 chip, odd or top MSA board.  
L C7 SkipNE 113357  
L X ShowError C-15 chip, odd or top MSA board.  
L C7 SkipNE 112352  
L X ShowError C-16 chip, odd or top MSA board.  
L C7 SkipNE 113457  
L X ShowError C-17 chip, odd or top MSA board.  
L C7 SkipNE 112052  
L X ShowError C-18 chip, odd or top MSA board.  
L C7 SkipNE 113556  
L X ShowError C-19 chip, odd or top MSA board.  
L C7 SkipNE 112153  
L X ShowError C-20 chip, odd or top MSA board.  
L C7 SkipNE 113656  
L X ShowError C-21 chip, odd or top MSA board.  
L C7 SkipNE 112253  
L X ShowError C-22 chip, odd or top MSA board.  
L C7 SkipNE 113020  
L X ShowError C-23 chip, odd or top MSA board.  
; Start row "D".  
L C7 SkipNE 112040  
L X ShowError D-4 chip, odd or top MSA board.  
L C7 SkipNE 113713  
L X ShowError D-5 chip, odd or top MSA board.  
L C7 SkipNE 112316  
L X ShowError D-6 chip, odd or top MSA board.  
L C7 SkipNE 113512  
L X ShowError D-7 chip, odd or top MSA board.  
L C7 SkipNE 112117  
L X ShowError D-8 chip, odd or top MSA board.  
L C7 SkipNE 113413  
L X ShowError D-9 chip, odd or top MSA board.  
L C7 SkipNE 112016  
L X ShowError D-10 chip, odd or top MSA board.  
L C7 SkipNE 113612  
L X ShowError D-11 chip, odd or top MSA board.  
L C7 SkipNE 112217

L X ShowError D-12 chip, odd or top MSA board.  
L C7 SkipNE 113752  
L X ShowError D-15 chip, odd or top MSA board.  
L C7 SkipNE 112357  
L X ShowError D-16 chip, odd or top MSA board.  
L C7 SkipNE 113452  
L X ShowError D-17 chip, odd or top MSA board.  
L C7 SkipNE 112057  
L X ShowError D-18 chip, odd or top MSA board.  
L C7 SkipNE 113553  
L X ShowError D-19 chip, odd or top MSA board.  
L C7 SkipNE 112156  
L X ShowError D-20 chip, odd or top MSA board.  
L C7 SkipNE 113653  
L X ShowError D-21 chip, odd or top MSA board.  
L C7 SkipNE 112256  
L X ShowError D-22 chip, odd or top MSA board.  
L C7 SkipNE 113420  
L X ShowError D-23 chip, odd or top MSA board.  
; Start row "G".  
L C7 SkipNE 113442  
L X ShowError G-4 chip, odd or top MSA board.  
L C7 SkipNE 112136  
L X ShowError G-5 chip, odd or top MSA board.  
L C7 SkipNE 113533  
L X ShowError G-6 chip, odd or top MSA board.  
L C7 SkipNE 112037  
L X ShowError G-7 chip, odd or top MSA board.  
L C7 SkipNE 113432  
L X ShowError G-8 chip, odd or top MSA board.  
L C7 SkipNE 112337  
L X ShowError G-9 chip, odd or top MSA board.  
L C7 SkipNE 113732  
L X ShowError G-10 chip, odd or top MSA board.  
L C7 SkipNE 112236  
L X ShowError G-11 chip, odd or top MSA board.  
L C7 SkipNE 113633  
L X ShowError G-12 chip, odd or top MSA board.  
L C7 SkipNE 112277  
L X ShowError G-15 chip, odd or top MSA board.  
L C7 SkipNE 113672  
L X ShowError G-16 chip, odd or top MSA board.  
L C7 SkipNE 112076  
L X ShowError G-17 chip, odd or top MSA board.  
L C7 SkipNE 113473  
L X ShowError G-18 chip, odd or top MSA board.  
L C7 SkipNE 112376  
L X ShowError G-19 chip, odd or top MSA board.  
L C7 SkipNE 113773  
L X ShowError G-20 chip, odd or top MSA board.  
L C7 SkipNE 112177  
L X ShowError G-21 chip, odd or top MSA board.  
L C7 SkipNE 113572  
L X ShowError G-22 chip, odd or top MSA board.  
L C7 SkipNE 112001  
L X ShowError G-23 chip, odd or top MSA board.  
; Start row "H".

L C7 SkipNE 113002  
L X ShowError H-4 chip, odd or top MSA board.  
L C7 SkipNE 112133  
L X ShowError H-5 chip, odd or top MSA board.  
L C7 SkipNE 113536  
L X ShowError H-6 chip, odd or top MSA board.  
L C7 SkipNE 112032  
L X ShowError H-7 chip, odd or top MSA board.  
L C7 SkipNE 113437  
L X ShowError H-8 chip, odd or top MSA board.  
L C7 SkipNE 112332  
L X ShowError H-9 chip, odd or top MSA board.  
L C7 SkipNE 113737  
L X ShowError H-10 chip, odd or top MSA board.  
L C7 SkipNE 112233  
L X ShowError H-11 chip, odd or top MSA board.  
L C7 SkipNE 113636  
L X ShowError H-12 chip, odd or top MSA board.  
L C7 SkipNE 112272  
L X ShowError H-15 chip, odd or top MSA board.  
L C7 SkipNE 113677  
L X ShowError H-16 chip, odd or top MSA board.  
L C7 SkipNE 112073  
L X ShowError H-17 chip, odd or top MSA board.  
L C7 SkipNE 113476  
L X ShowError H-18 chip, odd or top MSA board.  
L C7 SkipNE 112373  
L X ShowError H-19 chip, odd or top MSA board.  
L C7 SkipNE 113776  
L X ShowError H-20 chip, odd or top MSA board.  
L C7 SkipNE 112172  
L X ShowError H-21 chip, odd or top MSA board.  
L C7 SkipNE 113577  
L X ShowError H-22 chip, odd or top MSA board.  
L C7 SkipNE 112401  
L X ShowError H-23 chip, odd or top MSA board.  
; Start row "I".  
L C7 SkipNE 112402  
L X ShowError I-4 chip, odd or top MSA board.  
L C7 SkipNE 112536  
L X ShowError I-5 chip, odd or top MSA board.  
L C7 SkipNE 113133  
L X ShowError I-6 chip, odd or top MSA board.  
L C7 SkipNE 112437  
L X ShowError I-7 chip, odd or top MSA board.  
L C7 SkipNE 113032  
L X ShowError I-8 chip, odd or top MSA board.  
L C7 SkipNE 112737  
L X ShowError I-9 chip, odd or top MSA board.  
L C7 SkipNE 113332  
L X ShowError I-10 chip, odd or top MSA board.  
L C7 SkipNE 112636  
L X ShowError I-11 chip, odd or top MSA board.  
L C7 SkipNE 113233  
L X ShowError I-12 chip, odd or top MSA board.  
L C7 SkipNE 112677  
L X ShowError I-15 chip, odd or top MSA board.

L C7 SkipNE 113272  
L X ShowError I-16 chip, odd or top MSA board.  
L C7 SkipNE 112476  
L X ShowError I-17 chip, odd or top MSA board.  
L C7 SkipNE 113073  
L X ShowError I-18 chip, odd or top MSA board.  
L C7 SkipNE 112776  
L X ShowError I-19 chip, odd or top MSA board.  
L C7 SkipNE 113373  
L X ShowError I-20 chip, odd or top MSA board.  
L C7 SkipNE 112577  
L X ShowError I-21 chip, odd or top MSA board.  
L C7 SkipNE 113172  
L X ShowError I-22 chip, odd or top MSA board.  
L C7 SkipNE 113001  
L X ShowError I-23 chip, odd or top MSA board.  
; Start row "J".  
L C7 SkipNE 112002  
L X ShowError J-4 chip, odd or top MSA board.  
L C7 SkipNE 112533  
L X ShowError J-5 chip, odd or top MSA board.  
L C7 SkipNE 113136  
L X ShowError J-6 chip, odd or top MSA board.  
L C7 SkipNE 112432  
L X ShowError J-7 chip, odd or top MSA board.  
L C7 SkipNE 113037  
L X ShowError J-8 chip, odd or top MSA board.  
L C7 SkipNE 112732  
L X ShowError J-9 chip, odd or top MSA board.  
L C7 SkipNE 113337  
L X ShowError J-10 chip, odd or top MSA board.  
L C7 SkipNE 112633  
L X ShowError J-11 chip, odd or top MSA board.  
L C7 SkipNE 113236  
L X ShowError J-12 chip, odd or top MSA board.  
L C7 SkipNE 112672  
L X ShowError J-15 chip, odd or top MSA board.  
L C7 SkipNE 113277  
L X ShowError J-16 chip, odd or top MSA board.  
L C7 SkipNE 112473  
L X ShowError J-17 chip, odd or top MSA board.  
L C7 SkipNE 113076  
L X ShowError J-18 chip, odd or top MSA board.  
L C7 SkipNE 112773  
L X ShowError J-19 chip, odd or top MSA board.  
L C7 SkipNE 113376  
L X ShowError J-20 chip, odd or top MSA board.  
L C7 SkipNE 112572  
L X ShowError J-21 chip, odd or top MSA board.  
L C7 SkipNE 113177  
L X ShowError J-22 chip, odd or top MSA board.  
L C7 SkipNE 113401  
L X ShowError J-23 chip, odd or top MSA board.  
; Start row "A" Bottom board  
L C7 SkipNE 113600  
L X ShowError A-4 chip, even or bottom MSA board.  
L C7 SkipNE 113315

L X ShowError A-5 chip, even or bottom MSA board.  
L C7 SkipNE 112707  
L X ShowError A-6 chip, even or bottom MSA board.  
L C7 SkipNE 113114  
L X ShowError A-7 chip, even or bottom MSA board.  
L C7 SkipNE 112506  
L X ShowError A-8 chip, even or bottom MSA board.  
L C7 SkipNE 113015  
L X ShowError A-9 chip, even or bottom MSA board.  
L C7 SkipNE 112407  
L X ShowError A-10 chip, even or bottom MSA board.  
L C7 SkipNE 113214  
L X ShowError A-11 chip, even or bottom MSA board.  
L C7 SkipNE 112606  
L X ShowError A-12 chip, even or bottom MSA board.  
L C7 SkipNE 113354  
L X ShowError A-15 chip, even or bottom MSA board.  
L C7 SkipNE 112746  
L X ShowError A-16 chip, even or bottom MSA board.  
L C7 SkipNE 113054  
L X ShowError A-17 chip, even or bottom MSA board.  
L C7 SkipNE 112446  
L X ShowError A-18 chip, even or bottom MSA board.  
L C7 SkipNE 113155  
L X ShowError A-19 chip, even or bottom MSA board.  
L C7 SkipNE 112547  
L X ShowError A-20 chip, even or bottom MSA board.  
L C7 SkipNE 113255  
L X ShowError A-21 chip, even or bottom MSA board.  
L C7 SkipNE 112647  
L X ShowError A-22 chip, even or bottom MSA board.  
L C7 SkipNE 112100  
L X ShowError A-23 chip, even or bottom MSA board.  
; Start row "B".  
L C7 SkipNE 113200  
L X ShowError B-4 chip, even or bottom MSA board.  
L C7 SkipNE 113307  
L X ShowError B-5 chip, even or bottom MSA board.  
L C7 SkipNE 112715  
L X ShowError B-6 chip, even or bottom MSA board.  
L C7 SkipNE 113106  
L X ShowError B-7 chip, even or bottom MSA board.  
L C7 SkipNE 112514  
L X ShowError B-8 chip, even or bottom MSA board.  
L C7 SkipNE 113007  
L X ShowError B-9 chip, even or bottom MSA board.  
L C7 SkipNE 112415  
L X ShowError B-10 chip, even or bottom MSA board.  
L C7 SkipNE 113206  
L X ShowError B-11 chip, even or bottom MSA board.  
L C7 SkipNE 112614  
L X ShowError B-12 chip, even or bottom MSA board.  
L C7 SkipNE 113346  
L X ShowError B-15 chip, even or bottom MSA board.  
L C7 SkipNE 112754  
L X ShowError B-16 chip, even or bottom MSA board.  
L C7 SkipNE 113046

L X ShowError B-17 chip, even or bottom MSA board.  
L C7 SkipNE 112454  
L X ShowError B-18 chip, even or bottom MSA board.  
L C7 SkipNE 113147  
L X ShowError B-19 chip, even or bottom MSA board.  
L C7 SkipNE 112555  
L X ShowError B-20 chip, even or bottom MSA board.  
L C7 SkipNE 113247  
L X ShowError B-21 chip, even or bottom MSA board.  
L C7 SkipNE 112655  
L X ShowError B-22 chip, even or bottom MSA board.  
L C7 SkipNE 112500  
L X ShowError B-23 chip, even or bottom MSA board.  
; Start row "C". December 2, 1983 1:41 PM  
L C7 SkipNE 112600  
L X ShowError C-4 chip, even or bottom MSA board.  
L C7 SkipNE 113715  
L X ShowError C-5 chip, even or bottom MSA board.  
L C7 SkipNE 112307  
L X ShowError C-6 chip, even or bottom MSA board.  
L C7 SkipNE 113514  
L X ShowError C-7 chip, even or bottom MSA board.  
L C7 SkipNE 112106  
L X ShowError C-8 chip, even or bottom MSA board.  
L C7 SkipNE 113415  
L X ShowError C-9 chip, even or bottom MSA board.  
L C7 SkipNE 112007  
L X ShowError C-10 chip, even or bottom MSA board.  
L C7 SkipNE 113614  
L X ShowError C-11 chip, even or bottom MSA board.  
L C7 SkipNE 112206  
L X ShowError C-12 chip, even or bottom MSA board.  
L C7 SkipNE 113754  
L X ShowError C-15 chip, even or bottom MSA board.  
L C7 SkipNE 112346  
L X ShowError C-16 chip, even or bottom MSA board.  
L C7 SkipNE 113454  
L X ShowError C-17 chip, even or bottom MSA board.  
L C7 SkipNE 112046  
L X ShowError C-18 chip, even or bottom MSA board.  
L C7 SkipNE 113555  
L X ShowError C-19 chip, even or bottom MSA board.  
L C7 SkipNE 112147  
L X ShowError C-20 chip, even or bottom MSA board.  
L C7 SkipNE 113655  
L X ShowError C-21 chip, even or bottom MSA board.  
L C7 SkipNE 112247  
L X ShowError C-22 chip, even or bottom MSA board.  
L C7 SkipNE 113100  
L X ShowError C-23 chip, even or bottom MSA board.  
; Start row "D".  
L C7 SkipNE 112200  
L X ShowError D-4 chip, even or bottom MSA board.  
L C7 SkipNE 113707  
L X ShowError D-5 chip, even or bottom MSA board.  
L C7 SkipNE 112315  
L X ShowError D-6 chip, even or bottom MSA board.

L C7 SkipNE 113506  
L X ShowError D-7 chip, even or bottom MSA board.  
L C7 SkipNE 112114  
L X ShowError D-8 chip, even or bottom MSA board.  
L C7 SkipNE 113407  
L X ShowError D-9 chip, even or bottom MSA board.  
L C7 SkipNE 112015  
L X ShowError D-10 chip, even or bottom MSA board.  
L C7 SkipNE 113606  
L X ShowError D-11 chip, even or bottom MSA board.  
L C7 SkipNE 112214  
L X ShowError D-12 chip, even or bottom MSA board.  
L C7 SkipNE 113746  
L X ShowError D-15 chip, even or bottom MSA board.  
L C7 SkipNE 112354  
L X ShowError D-16 chip, even or bottom MSA board.  
L C7 SkipNE 113446  
L X ShowError D-17 chip, even or bottom MSA board.  
L C7 SkipNE 112054  
L X ShowError D-18 chip, even or bottom MSA board.  
L C7 SkipNE 113547  
L X ShowError D-19 chip, even or bottom MSA board.  
L C7 SkipNE 112155  
L X ShowError D-20 chip, even or bottom MSA board.  
L C7 SkipNE 113647  
L X ShowError D-21 chip, even or bottom MSA board.  
L C7 SkipNE 112255  
L X ShowError D-22 chip, even or bottom MSA board.  
L C7 SkipNE 113500  
L X ShowError D-23 chip, even or bottom MSA board.  
; Start row "G".  
L C7 SkipNE 113410  
L X ShowError G-4 chip, even or bottom MSA board.  
L C7 SkipNE 112135  
L X ShowError G-5 chip, even or bottom MSA board.  
L C7 SkipNE 113527  
L X ShowError G-6 chip, even or bottom MSA board.  
L C7 SkipNE 112034  
L X ShowError G-7 chip, even or bottom MSA board.  
L C7 SkipNE 113426  
L X ShowError G-8 chip, even or bottom MSA board.  
L C7 SkipNE 112334  
L X ShowError G-9 chip, even or bottom MSA board.  
L C7 SkipNE 113726  
L X ShowError G-10 chip, even or bottom MSA board.  
L C7 SkipNE 112235  
L X ShowError G-11 chip, even or bottom MSA board.  
L C7 SkipNE 113627  
L X ShowError G-12 chip, even or bottom MSA board.  
L C7 SkipNE 112247  
L X ShowError G-15 chip, even or bottom MSA board.  
L C7 SkipNE 113666  
L X ShowError G-16 chip, even or bottom MSA board.  
L C7 SkipNE 112075  
L X ShowError G-17 chip, even or bottom MSA board.  
L C7 SkipNE 113467  
L X ShowError G-18 chip, even or bottom MSA board.

L C7 SkipNE 112375  
L X ShowError G-19 chip, even or bottom MSA board.  
L C7 SkipNE 113767  
L X ShowError G-20 chip, even or bottom MSA board.  
L C7 SkipNE 112174  
L X ShowError G-21 chip, even or bottom MSA board.  
L C7 SkipNE 113566  
L X ShowError G-22 chip, even or bottom MSA board.  
L C7 SkipNE 112004  
L X ShowError G-23 chip, even or bottom MSA board.  
; Start row "H".  
L C7 SkipNE 113010  
L X ShowError H-4 chip, even or bottom MSA board.  
L C7 SkipNE 112127  
L X ShowError H-5 chip, even or bottom MSA board.  
L C7 SkipNE 113535  
L X ShowError H-6 chip, even or bottom MSA board.  
L C7 SkipNE 112026  
L X ShowError H-7 chip, even or bottom MSA board.  
L C7 SkipNE 113434  
L X ShowError H-8 chip, even or bottom MSA board.  
L C7 SkipNE 112326  
L X ShowError H-9 chip, even or bottom MSA board.  
L C7 SkipNE 113734  
L X ShowError H-10 chip, even or bottom MSA board.  
L C7 SkipNE 112227  
L X ShowError H-11 chip, even or bottom MSA board.  
L C7 SkipNE 113635  
L X ShowError H-12 chip, even or bottom MSA board.  
L C7 SkipNE 112266  
L X ShowError H-15 chip, even or bottom MSA board.  
L C7 SkipNE 113674  
L X ShowError H-16 chip, even or bottom MSA board.  
L C7 SkipNE 112067  
L X ShowError H-17 chip, even or bottom MSA board.  
L C7 SkipNE 113475  
L X ShowError H-18 chip, even or bottom MSA board.  
L C7 SkipNE 112367  
L X ShowError H-19 chip, even or bottom MSA board.  
L C7 SkipNE 113775  
L X ShowError H-20 chip, even or bottom MSA board.  
L C7 SkipNE 112166  
L X ShowError H-21 chip, even or bottom MSA board.  
L C7 SkipNE 113574  
L X ShowError H-22 chip, even or bottom MSA board.  
L C7 SkipNE 112404  
L X ShowError H-23 chip, even or bottom MSA board.  
; Start row "I".  
L C7 SkipNE 112410  
L X ShowError I-4 chip, even or bottom MSA board.  
L C7 SkipNE 112535  
L X ShowError I-5 chip, even or bottom MSA board.  
L C7 SkipNE 113127  
L X ShowError I-6 chip, even or bottom MSA board.  
L C7 SkipNE 112434  
L X ShowError I-7 chip, even or bottom MSA board.  
L C7 SkipNE 113026

L X ShowError I-8 chip, even or bottom MSA board.  
L C7 SkipNE 112734  
L X ShowError I-9 chip, even or bottom MSA board.  
L C7 SkipNE 113326  
L X ShowError I-10 chip, even or bottom MSA board.  
L C7 SkipNE 112635  
L X ShowError I-11 chip, even or bottom MSA board.  
L C7 SkipNE 113227  
L X ShowError I-12 chip, even or bottom MSA board.  
L C7 SkipNE 112674  
L X ShowError I-15 chip, even or bottom MSA board.  
L C7 SkipNE 113266  
L X ShowError I-16 chip, even or bottom MSA board.  
L C7 SkipNE 112475  
L X ShowError I-17 chip, even or bottom MSA board.  
L C7 SkipNE 113067  
L X ShowError I-18 chip, even or bottom MSA board.  
L C7 SkipNE 112775  
L X ShowError I-19 chip, even or bottom MSA board.  
L C7 SkipNE 113367  
L X ShowError I-20 chip, even or bottom MSA board.  
L C7 SkipNE 112574  
L X ShowError I-21 chip, even or bottom MSA board.  
L C7 SkipNE 113166  
L X ShowError I-22 chip, even or bottom MSA board.  
L C7 SkipNE 113004  
L X ShowError I-23 chip, even or bottom MSA board.  
; Start row "J".December 2, 1983 6:01 PM  
L C7 SkipNE 112010  
L X ShowError J-4 chip, even or bottom MSA board.  
L C7 SkipNE 112527  
L X ShowError J-5 chip, even or bottom MSA board.  
L C7 SkipNE 113135  
L X ShowError J-6 chip, even or bottom MSA board.  
L C7 SkipNE 112426  
L X ShowError J-7 chip, even or bottom MSA board.  
L C7 SkipNE 113034  
L X ShowError J-8 chip, even or bottom MSA board.  
L C7 SkipNE 112726  
L X ShowError J-9 chip, even or bottom MSA board.  
L C7 SkipNE 113334  
L X ShowError J-10 chip, even or bottom MSA board.  
L C7 SkipNE 112627  
L X ShowError J-11 chip, even or bottom MSA board.  
L C7 SkipNE 113235  
L X ShowError J-12 chip, even or bottom MSA board.  
L C7 SkipNE 112666  
L X ShowError J-15 chip, even or bottom MSA board.  
L C7 SkipNE 113274  
L X ShowError J-16 chip, even or bottom MSA board.  
L C7 SkipNE 112467  
L X ShowError J-17 chip, even or bottom MSA board.  
L C7 SkipNE 113075  
L X ShowError J-18 chip, even or bottom MSA board.  
L C7 SkipNE 112767  
L X ShowError J-19 chip, even or bottom MSA board.  
L C7 SkipNE 113375

L X ShowError J-20 chip, even or bottom MSA board.  
L C7 SkipNE 112566  
L X ShowError J-21 chip, even or bottom MSA board.  
L C7 SkipNE 113174  
L X ShowError J-22 chip, even or bottom MSA board.  
L C7 SkipNE 113404  
L X ShowError J-23 chip, even or bottom MSA board.  
L X ShowError I couldn't figure out which memory chip is bad.  
; end of Bottom board

### 39. MsaPair.Midas

; December 3, 1983 3:25 PM  
; Last modified by Frank Vest May 6, 1985 12:06 PM  
L B3 SkipGE 20  
L X ShowError Module 0  
L B3 SkipGE 20  
L X Skip .Done  
L B3 SkipGE 40  
L X ShowError Module 1 if 64k chips, Module 0 if 256k chips.  
L B3 SkipGE 40  
L X Skip .Done  
L B3 SkipGE 60  
L X ShowError Module 2 if 64k chips, Module 0 if 256k chips.  
L B3 SkipGE 60  
L X Skip .Done  
L B3 SkipGE 100  
L X ShowError Module 3 if 64k chips, Module 0 if 256k chips.  
L B3 SkipGE 100  
L X Skip .Done  
L B3 SkipGE 200  
L X ShowError Module 1, 256k chips are installed.  
L B3 SkipGE 200  
L X Skip .Done  
L B3 SkipGE 300  
L X ShowError Module 2, 256k chips are installed.  
L B3 SkipGE 300  
L X Skip .Done  
L B3 SkipGE 400  
L X ShowError Module 3, 256k chips are installed.  
L X Skip .Done  
.Done L X DisplayOn

### 40. IMRH.Midas

L A2 Val 10466

### 41. IMLH.Midas

L A2 Val 10472

### 42. RAMPE.Midas

L A2 Val 477

### 43. IOBPE.Midas

L A2 Val 10474

### 44. MDPE.Midas

L A2 Val 10456

### 45. MemoryPE.Midas

L A2 Val 10076

### 46. SaveDisplay.Midas

- L X OpenOutput CRASH
- L X WriteMessage ~Crash dump on\  
L X WriteDT
- L X WriteMessage ~
- L X DumpDisplay
- L X CloseOutput
- L X ShowError Abort and print the file CRASH.REPORT with Empress

### 47. SaveIfuCrash.Midas

- L X OpenOutput IFUCRASH
- L X WriteMessage ~Crash dump on\  
L X WriteDT
- L X WriteMessage ~
- L X DumpDisplay
- L X DMux
- L X PrettyPrint CJNK0
- L X PrettyPrint CJNK1
- L X PrettyPrint FFEQ
- L X PrettyPrint CJNK3
- L X PrettyPrint BNT
- L X PrettyPrint PENC
- L X PrettyPrint CTD
- L X PrettyPrint NEXT
- L X PrettyPrint CIA
- L X PrettyPrint TNIA
- L X PrettyPrint BNPC
- L X PrettyPrint CIAINC
- L X PrettyPrint CTASK
- L X PrettyPrint RA
- L X PrettyPrint TOPE
- L X PrettyPrint READY
- L X PrettyPrint BMUX
- L X PrettyPrint ALUB
- L X PrettyPrint ALUA
- L X PrettyPrint MAR
- L X PrettyPrint ABCON
- L X PrettyPrint PERR
- L X PrettyPrint SHMV
- L X PrettyPrint PRFA

L X PrettyPrint SCCON  
L X PrettyPrint QPDCON  
L X PrettyPrint ALUCON  
L X PrettyPrint NEXTCL  
L X PrettyPrint RADDR  
L X PrettyPrint STKRB  
L X PrettyPrint RTSB  
L X PrettyPrint PJUNK  
L X PrettyPrint PVAH  
L X PrettyPrint PVAL  
L X PrettyPrint MAPAD  
L X PrettyPrint HIT  
L X PrettyPrint HOLD  
L X PrettyPrint PAIR  
L X PrettyPrint PIPEAD  
L X PrettyPrint AAD  
L X PrettyPrint MEMB  
L X PrettyPrint MEMDO  
L X PrettyPrint DAD  
L X PrettyPrint FD  
L X PrettyPrint EC  
L X PrettyPrint TSYN  
L X PrettyPrint MDMAD  
L X PrettyPrint DADE  
L X PrettyPrint MAPBUF  
L X PrettyPrint P34INEC  
L X PrettyPrint MCDTSK  
L X PrettyPrint STA  
L X PrettyPrint APESRN  
L X PrettyPrint STOUT  
L X PrettyPrint TAGAT  
L X PrettyPrint MEMST  
L X PrettyPrint FLTMEM  
L X PrettyPrint RFSSRN  
L X PrettyPrint EC1MAKE  
L X PrettyPrint MAPCTRL  
L X PrettyPrint PEEC  
L X PrettyPrint INMAP  
L X PrettyPrint MEMRQ  
L X PrettyPrint LOADS  
L X PrettyPrint HJ  
L X PrettyPrint MX  
L X PrettyPrint JMPEXC  
L X PrettyPrint PCJ  
L X PrettyPrint FFK  
L X PrettyPrint IDLY  
L X PrettyPrint IFUM 0  
L X PrettyPrint IFUM 1  
L X PrettyPrint IFUM 2  
L X PrettyPrint IFUM 3  
L X PrettyPrint IFUM 4  
L X PrettyPrint IFUM 5  
L X PrettyPrint IFUM 6  
L X PrettyPrint IFUM 7  
L X PrettyPrint IFUM 10  
L X PrettyPrint IFUM 11  
L X PrettyPrint IFUM 12

L X PrettyPrint IFUM 13  
L X PrettyPrint IFUM 14  
L X PrettyPrint IFUM 15  
L X PrettyPrint IFUM 16  
L X PrettyPrint IFUM 17  
L X PrettyPrint IFUM 20  
L X PrettyPrint IFUM 400  
L X PrettyPrint IFUM 401  
L X PrettyPrint IFUM 402  
L X PrettyPrint IFUM 403  
L X PrettyPrint IFUM 404  
L X PrettyPrint IFUM 405  
L X PrettyPrint IFUM 406  
L X PrettyPrint IFUM 407  
L X PrettyPrint IFUM 410  
L X PrettyPrint IFUM 411  
L X PrettyPrint IFUM 412  
L X PrettyPrint IFUM 413  
L X PrettyPrint IFUM 414  
L X PrettyPrint IFUM 415  
L X PrettyPrint IFUM 416  
L X PrettyPrint IFUM 417  
L X PrettyPrint IFUM 420  
L X PrettyPrint IFUM 1000  
L X PrettyPrint IFUM 1001  
L X PrettyPrint IFUM 1002  
L X PrettyPrint IFUM 1003  
L X PrettyPrint IFUM 1004  
L X PrettyPrint IFUM 1005  
L X PrettyPrint IFUM 1006  
L X PrettyPrint IFUM 1007  
L X PrettyPrint IFUM 1010  
L X PrettyPrint IFUM 1011  
L X PrettyPrint IFUM 1012  
L X PrettyPrint IFUM 1013  
L X PrettyPrint IFUM 1014  
L X PrettyPrint IFUM 1015  
L X PrettyPrint IFUM 1016  
L X PrettyPrint IFUM 1017  
L X PrettyPrint IFUM 1020  
L X PrettyPrint IFUM 1400  
L X PrettyPrint IFUM 1401  
L X PrettyPrint IFUM 1402  
L X PrettyPrint IFUM 1403  
L X PrettyPrint IFUM 1404  
L X PrettyPrint IFUM 1405  
L X PrettyPrint IFUM 1406  
L X PrettyPrint IFUM 1407  
L X PrettyPrint IFUM 1410  
L X PrettyPrint IFUM 1411  
L X PrettyPrint IFUM 1412  
L X PrettyPrint IFUM 1413  
L X PrettyPrint IFUM 1414  
L X PrettyPrint IFUM 1415  
L X PrettyPrint IFUM 1416  
L X PrettyPrint IFUM 1417  
L X PrettyPrint IFUM 1420

X CloseOutput  
 L X ShowError Abort and print the file IFUCRASH.REPORT with Empress

#### 48. SimTestNoErrors.Midas

L B19 Addr CJNK3  
 LR X DMux  
 L B19 Val 177774 ; get rid of bSwitch'a/A failures  
 L X RdCmds  
 L X ifud  
 M B7 Val  
 LR X DMux ; Get rid of the DSel0 and the DSel1 errors  
 L B7 Val 177477; Get rid of the DSel0 and the DSel1 errors  
 L B10 Addr HIT  
 LR X DMux  
 L B10 Val 177477 ; get rid of ColVic.0 and ColVic.1  
 L X RdCmds  
 L X mmx  
 LR X DMux  
 L B6 Val 167777 ; get rid of STWait-Mem'/X errors  
 L X TimeOut 777777777; as close to infinite timeout as we can manage.  
 L X SimTest  
 M X DMux ; TO DISPLAY THE ERROR(S).

#### 49. SimTest20.Midas

; By Frank Vest  
 ; May 5, 1984 10:51 AM

L B19 Addr CJNK3  
 LR X DMux  
 L B19 Val 177774 ; get rid of bSwitch'a/A failures  
 L X RdCmds  
 L X ifud  
 M B7 Val  
 LR X DMux ; Get rid of the DSel0 and the DSel1 errors  
 L B7 Val 177477; Get rid of the DSel0 and the DSel1 errors  
 L B10 Addr HIT  
 LR X DMux  
 L B10 Val 177477 ;get rid of ColVic.0 and ColVic.1  
 L X RdCmds  
 L X mmx  
 LR X DMux  
 L B6 Val 167777 ; get rid of STWait-Mem'/X errors  
 ;Now run the simtest  
 L X TimeOut 77777777  
 L X SimTest  
 L X Skip .Error  
 L X Skip .Complete  
 L X OpenOutput SIMERROR  
 L X WriteMessage ~Simulator dump on\  
 L X WriteDT  
 L X WriteMessage ~  
 M X DMux ; Put failures on comment line  
 L X DumpDisplay ; Print 1st 20 simulation failures

Error

```

      L X TimeOut 77777777 ; Start over delay set forever
      L X SimTest
      L X Skip .Error1
      L X Skip .Complete
      L X WriteMessage ~Simulator dump on\
      L X WriteDT
.Error1 M X DMux ; Put failures on comment line
      L X DumpDisplay ; Print 1st 20 simulation failures

      L X TimeOut 77777777 ; Start over delay set forever
      L X SimTest
      L X Skip .Error2
      L X Skip .Complete
      L X WriteMessage ~Simulator dump on\
      L X WriteDT
.Error2 M X DMux ; Put failures on comment line
      L X DumpDisplay ; Print 1st 20 simulation failures

      L X TimeOut 77777777 ; Start over delay set forever
      L X SimTest
      L X Skip .Error3
      L X Skip .Complete
      L X WriteMessage ~Simulator dump on\
      L X WriteDT
.Error3 M X DMux ; Put failures on comment line
      L X DumpDisplay ; Print 1st 20 simulation failures

      L X TimeOut 77777777 ; Start over delay set forever
      L X SimTest
      L X Skip .Error4
      L X Skip .Complete
      L X WriteMessage ~Simulator dump on\
      L X WriteDT
.Error4 M X DMux ; Put failures on comment line
      L X DumpDisplay ; Print 1st 20 simulation failures

      L X TimeOut 77777777 ; Start over delay set forever
      L X SimTest
      L X Skip .Error5
      L X Skip .Complete
      L X WriteMessage ~Simulator dump on\
      L X WriteDT
.Error5 M X DMux ; Put failures on comment line
      L X DumpDisplay ; Print 1st 20 simulation failures

      L X TimeOut 77777777 ; Start over delay set forever
      L X SimTest
      L X Skip .Error6
      L X Skip .Complete
      L X WriteMessage ~Simulator dump on\
      L X WriteDT
.Error6 M X DMux ; Put failures on comment line
      L X DumpDisplay ; Print 1st 20 simulation failures

      L X TimeOut 77777777 ; Start over delay set forever
      L X SimTest
      L X Skip .Error7

```

```

      L X Skip .Complete
      L X WriteMessage ~Simulator dump on\
      L X WriteDT
.Error7      M X DMux ; Put failures on comment line
             L X DumpDisplay ; Print 1st 20 simulation failures

      L X TimeOut 77777777 ; Start over delay set forever
      L X SimTest
      L X Skip .Error8
      L X Skip .Complete
      L X WriteMessage ~Simulator dump on\
      L X WriteDT
.Error8      M X DMux ; Put failures on comment line
             L X DumpDisplay ; Print 1st 20 simulation failures

      L X TimeOut 77777777 ; Start over delay set forever
      L X SimTest
      L X Skip .Error9
      L X Skip .Complete
      L X WriteMessage ~Simulator dump on\
      L X WriteDT
.Error9      M X DMux ; Put failures on comment line
             L X DumpDisplay ; Print 1st 20 simulation failures

      L X TimeOut 77777777 ; Start over delay set forever
      L X SimTest
      L X Skip .Error10
      L X Skip .Complete
      L X WriteMessage ~Simulator dump on\
      L X WriteDT
.Error10     M X DMux ; Put failures on comment line
             L X DumpDisplay ; Print 1st 20 simulation failures

      L X TimeOut 77777777 ; Start over delay set forever
      L X SimTest
      L X Skip .Error11
      L X Skip .Complete
      L X WriteMessage ~Simulator dump on\
      L X WriteDT
.Error11     M X DMux ; Put failures on comment line
             L X DumpDisplay ; Print 1st 20 simulation failures

      L X TimeOut 77777777 ; Start over delay set forever
      L X SimTest
      L X Skip .Error12
      L X Skip .Complete
      L X WriteMessage ~Simulator dump on\
      L X WriteDT
.Error12     M X DMux ; Put failures on comment line
             L X DumpDisplay ; Print 1st 20 simulation failures

      L X TimeOut 77777777 ; Start over delay set forever
      L X SimTest
      L X Skip .Error13
      L X Skip .Complete
      L X WriteMessage ~Simulator dump on\
      L X WriteDT

```

```
.Error13  M X DMux ; Put failures on comment line
           L X DumpDisplay ; Print 1st 20 simulation failures

           L X TimeOut 77777777 ; Start over delay set forever
           L X SimTest
           L X Skip .Error14
           L X Skip .Complete
           L X WriteMessage ~Simulator dump on\
           L X WriteDT

.Error14  M X DMux ; Put failures on comment line
           L X DumpDisplay ; Print 1st 20 simulation failures

           L X TimeOut 77777777 ; Start over delay set forever
           L X SimTest
           L X Skip .Error15
           L X Skip .Complete
           L X WriteMessage ~Simulator dump on\
           L X WriteDT

.Error15  M X DMux ; Put failures on comment line
           L X DumpDisplay ; Print 1st 20 simulation failures

           L X TimeOut 77777777 ; Start over delay set forever
           L X SimTest
           L X Skip .Error16
           L X Skip .Complete
           L X WriteMessage ~Simulator dump on\
           L X WriteDT

.Error16  M X DMux ; Put failures on comment line
           L X DumpDisplay ; Print 1st 20 simulation failures

           L X TimeOut 77777777 ; Start over delay set forever
           L X SimTest
           L X Skip .Error17
           L X Skip .Complete
           L X WriteMessage ~Simulator dump on\
           L X WriteDT

.Error17  M X DMux ; Put failures on comment line
           L X DumpDisplay ; Print 1st 20 simulation failures

           L X TimeOut 77777777 ; Start over delay set forever
           L X SimTest
           L X Skip .Error18
           L X Skip .Complete
           L X WriteMessage ~Simulator dump on\
           L X WriteDT

.Error18  M X DMux ; Put failures on comment line
           L X DumpDisplay ; Print 1st 20 simulation failures

           L X TimeOut 77777777 ; Start over delay set forever
           L X SimTest
           L X Skip .Error19
           L X Skip .Complete
           L X WriteMessage ~Simulator dump on\
           L X WriteDT

.Error19  M X DMux ; Put failures on comment line
           L X DumpDisplay ; Print 1st 20 simulation failures
```

```

L X TimeOut 77777777 ; Start over delay set forever
L X SimTest
L X Skip .Error20
L X Skip .Complete
L X WriteMessage ~Simulator dump on\
L X WriteDT
.Error20 M X DMux ; Put failures on comment line
L X DumpDisplay ; Print 1st 20 simulation failures
L X CloseOutput
L X ShowError Abort (20 SimTest errors) print the file SIMERROR.REPORT with Empress

.Complete L X CloseOutput

```

## 50. StartMap.Midas

```

L B19 Addr HOLD
LR X DMux
L B19 Val 165454

```

## 51. MirDebug.Midas

```

L A2 Val 10476

```

## 52. IMBDAAddr.Midas

```

; Written by Frank Vest
; April 5, 1984 4:53 PM
L C0 Addr IMBD 0
L C1 Addr IMBD 1
L C2 Addr IMBD 2
L C3 Addr IMBD 4
L C4 Addr IMBD 10
L C5 Addr IMBD 20
L C6 Addr IMBD 40
L C7 Addr IMBD 100
L C8 Addr IMBD 200
L C9 Addr IMBD 400
L C10 Addr IMBD 1000
L C11 Addr IMBD 2000
L C12 Addr IMBD 4000
L C0 Val 0
L C1 Val 1
L C2 Val 2
L C3 Val 4
L C4 Val 10
L C5 Val 20
L C6 Val 40
L C7 Val 100
L C8 Val 200
L C9 Val 400
L C10 Val 1000
L C11 Val 2000
L C12 Val 4000

```

;Now check for correct values.

L C0 SkipE 0 ; Value for IMBD 0  
L X ShowError Value for IMBD 0 wrong should be "0" ContB board.  
L C1 SkipE 1 ; Value for IMBD 1  
L X ShowError Value for IMBD 1 wrong should be "1" ContB board.  
L C2 SkipE 2 ; Value for IMBD 2  
L X ShowError Value for IMBD 2 wrong should be "2" ContB board.  
L C3 SkipE 4 ; Value for IMBD 4  
L X ShowError Value for IMBD 4 wrong should be "4" ContB board.  
L C4 SkipE 10 ; Value for IMBD 10  
L X ShowError Value for IMBD 10 wrong should be "10" ContB board.  
L C5 SkipE 20 ; Value for IMBD 20  
L X ShowError Value for IMBD 20 wrong should be "20" ContB board.  
L C6 SkipE 40 ; Value for IMBD 40  
L X ShowError Value for IMBD 40 wrong should be "40" ContB board.  
L C7 SkipE 100 ; Value for IMBD 100  
L X ShowError Value for IMBD 100 wrong should be "100" ContB board.  
L C8 SkipE 200 ; Value for IMBD 200  
L X ShowError Value for IMBD 200 wrong should be "200" ContB board.  
L C9 SkipE 400 ; Value for IMBD 400  
L X ShowError Value for IMBD 400 wrong should be "400" ContB board.  
L C10 SkipE 1000 ; Value for IMBD 1000  
L X ShowError Value for IMBD 1000 wrong should be "1000" ContB board.  
L C11 SkipE 2000 ; Value for IMBD 2000  
L X ShowError Value for IMBD 2000 wrong should be "2000" ContB board.  
L C12 SkipE 4000 ; Value for IMBD 4000  
L X ShowError Value for IMBD 4000 wrong should be "4000" ContB board.

**53. MakeColorLISP.Cm**

```
// Written by Frank Vest
// October 18, 1984 10:24 AM
// Install LISP COLORDemo << PARTITION 18 >>

delete dmt.boot dumper.boot // garbage on disk
//install swat
ftp Indigo ^
directory/c Alto retrieve/>A InstallSwat.run Sys.Errors
InstallSwat
Delete dumper.boot

FTP IO RET/S <VEST>LISPCOLORUSER.CM USER.CM

//Now create Lisp.virtualmem
ftp Indigo directory/c Alto retrieve/>A CreateFile.run
CREATEFILE.run LISP.VIRTUALMEM 12000D

// Install Lisp Systems files

FTP ERIS dir/c <Lisp>Current> Ret/>A ^
LISP.run LISP.syms ^
DORADOLispMC.eb ^
AltoD1MC.eb ^
Init.Sample ^
Init.NoNet ^

FTP IO ret <EMS>Lisp.Sysout <EMS>InstallFonts.cm <EMS>LISP.RUN

// Install Lisp fonts

@InstallFonts.cm@

// Install Burn-in test

//FTP IO Ret <Ems>Test

FTP Io Dir/C Alto Ret/C ^
Scavenger.run KeyTest.run CopyDisk.run Neptune.run Empress.run ^
Peek.run PeekPup.run EtherWatch.run EDP.run PUPTest.run ^

FTP Io dir/c EMS load LISPColorFiles.dm

FTP IO RET <EMS>TEST

//Scavenge the disk
Scavenger.run
```

**54. MakeDemoLISP.Cm**

```
// Install LISP DEMO << PARTITION 17 >>
// Written by Frank Vest
// October 18, 1984 10:23 AM
```

```

delete dmt.boot dumper.boot // garbage on disk
//install swat
ftp Indigo ^
directory/c Alto retrieve/>A InstallSwat.run Sys.Errors
InstallSwat
Delete dumper.boot

FTP IO RET/S <VEST>LISPDEMOUSER.CM USER.CM

//Now create Lisp.virtualmem
ftp Indigo directory/c Alto retrieve/>A CreateFile.run
CREATEFILE.run LISP.VIRTUALMEM 12000D

// Install Lisp Systems files
FTP IO RET <EMS>DEMO.SYSOUT <EMS>LISP.RUN <EMS>InstallFonts.cm

FTP ERIS dir/c <Lisp>Current> Ret/>A ^
LISP.syms ^
DORADOLispMC.eb ^
AltoDIMC.eb ^
Init.Sample ^
Init.NoNet ^

// Install Lisp fonts

@InstallFonts.cm@

// Install Burn-in test

FTP IO Ret <EMS>Test
FTP IO Ret <Alto>Scavenger.run

//Scavenge the disk
Scavenger.run

```

## 55. NewDoradoDisk.Cm

```

FTP IO DIRECTORY/C VEST RETRIEVE/C USER.CM STAMP.SIL LAUREL.PROFILE FONTS.WIDTHS
KINETIC4.RUN Grid.sil
FTP IVY DIRECTORY/C LAUREL RETRIEVE/S LAUREL.RUN LAUREL.RUN
FTP IO LOAD <VEST>FONTS.DM
FTP IO DIRECTORY/C ALTO RETRIEVE/C BRAVO.ERROR BRAVO.MESSAGES BRAVO.RUN
EMPRESS.RUN INSTALLSWAT.RUN NEPTUNE.RUN TYPE.RUN
DEL DMT.BOOT
INSTALLSWAT.RUN
FTP IVY RET <GAMES>BATTLESHIP.RUN <GAMES>polyGONS.RUN <GAMES>PACMAN7.RUN
<GAMES>BREAKOUT.RUN

FTP IO RETRIEVE <ALTO>EDP.RUN

FTP IO RETRIEVE <EMS>LISPANDSMALLTALK.CM
@LISPANDSMALLTALK.CM

FTP IO LOAD <EMS>SIL.DM

FTP IO LOAD <EMS>sillibraries.dm

```

FTP IO LOAD <EMS>Smalltalkcolortest.dm

BRAVO/I

SIL/I

## **56. MakeGarageMidasManual.Cm**

Pressedit.run GarageMidasManual.Press \_ GarageMidas1.Press GARageMidas1a.Press Grid.press

Ftp indigo conn/c DoradoDocs store/c GarageMidasManual.Press

## **57. MakeGarageMidasListings.Cm**

Pressedit.run GarageMidasListings.Press \_ GarageMidas2.Press GarageMidas3.Press GarageMidas4.Press

Ftp indigo conn/c DoradoDocs store/c GarageMidasListings.Press

## **58. DumpGarageMidasManual.Cm**

Ftp Indigo conn/c Doradosource dump/c GarageMidasManual.dm Garagemidas1.bravo garagemidas1a.bravo garagemidas2.bravo garagemidas3.bravo garagemidas4.bravo dumpgarageMidasManual.cm Grid.sil grid0.sil grid25.sil Grid.press MakeGarageMidasManual.cm MakeGarageMidasListings.cm

## **59. Midas.UserPrograms**

FMEMA  
MEMMISC  
IFUSIMPLE  
IFUCOMPLEX  
EVENTCOUNTERS  
TRICOND  
EDP  
;DIEX  
SBOARDTEST  
XBOARDTEST  
DBOARDTEST  
CBOARDTEST  
SBOARDTEST  
LAG1  
LAG  
LAGSPEEDTEST  
SADDRTEST  
FIO  
;SAVEDISPLAY\*  
ACCEPTANCETESTS\*  
VIT\*  
MAPADDR\*  
KLINK\*  
MSAPAIR\*  
BADCHIP\*

## **60. CiaMap.Midas**

```
; Written by Frank Vest
; May 13, 1985
      L X CloseOutput
      L X OpenOutput CIAmap.report
.Begin L X WriteMessage ~
      L X PrettyPrint CIA
      L X SS
      L X BackSkip .Begin
```

## **61. MirMap.Midas**

```
; Written by Frank Vest
; May 13, 1985
      L X CloseOutput
      L X OpenOutput MIRmap.report
.Begin L X WriteMessage ~
      L X PrettyPrint MIR
      L X SS
      L X BackSkip .Begin
```