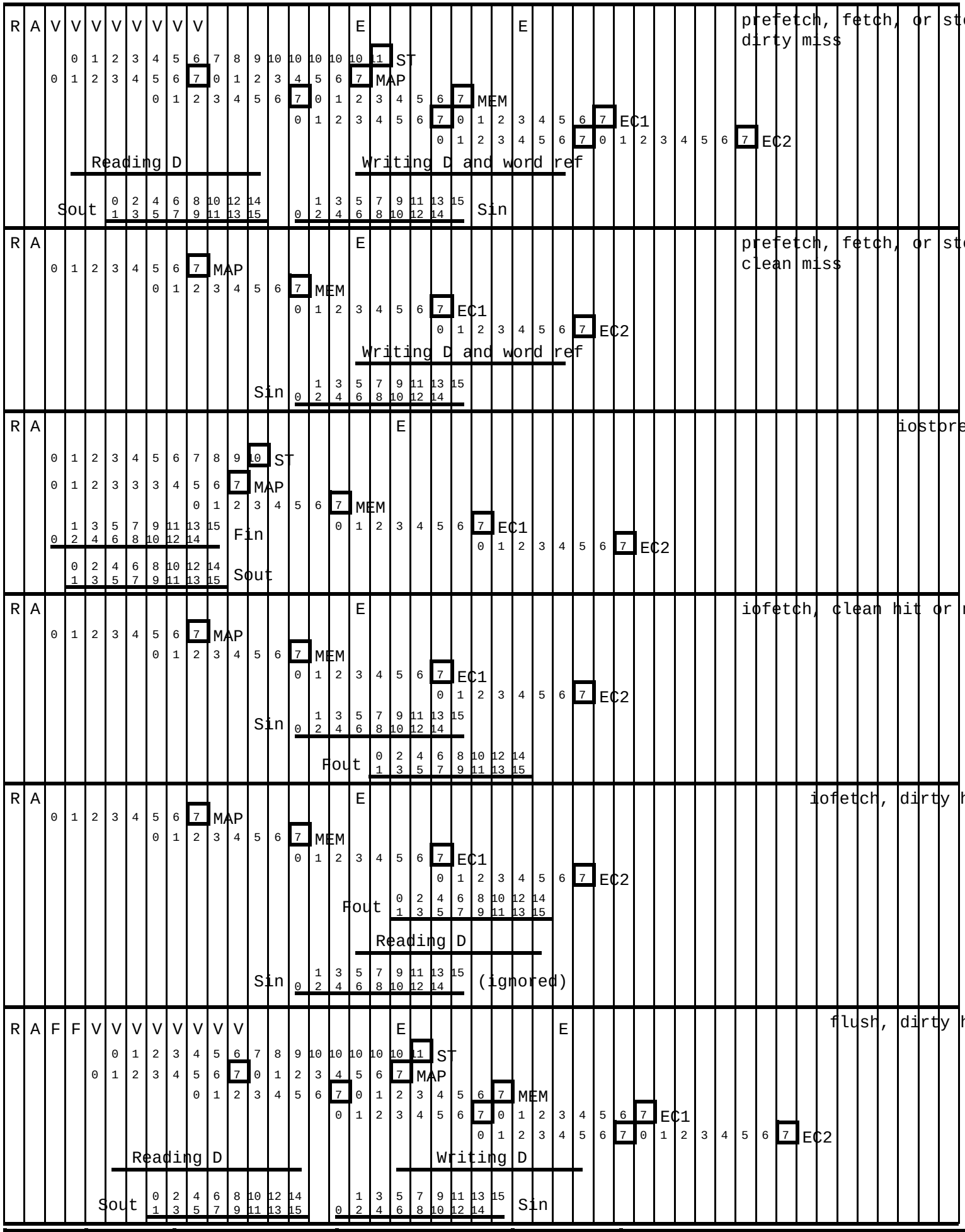
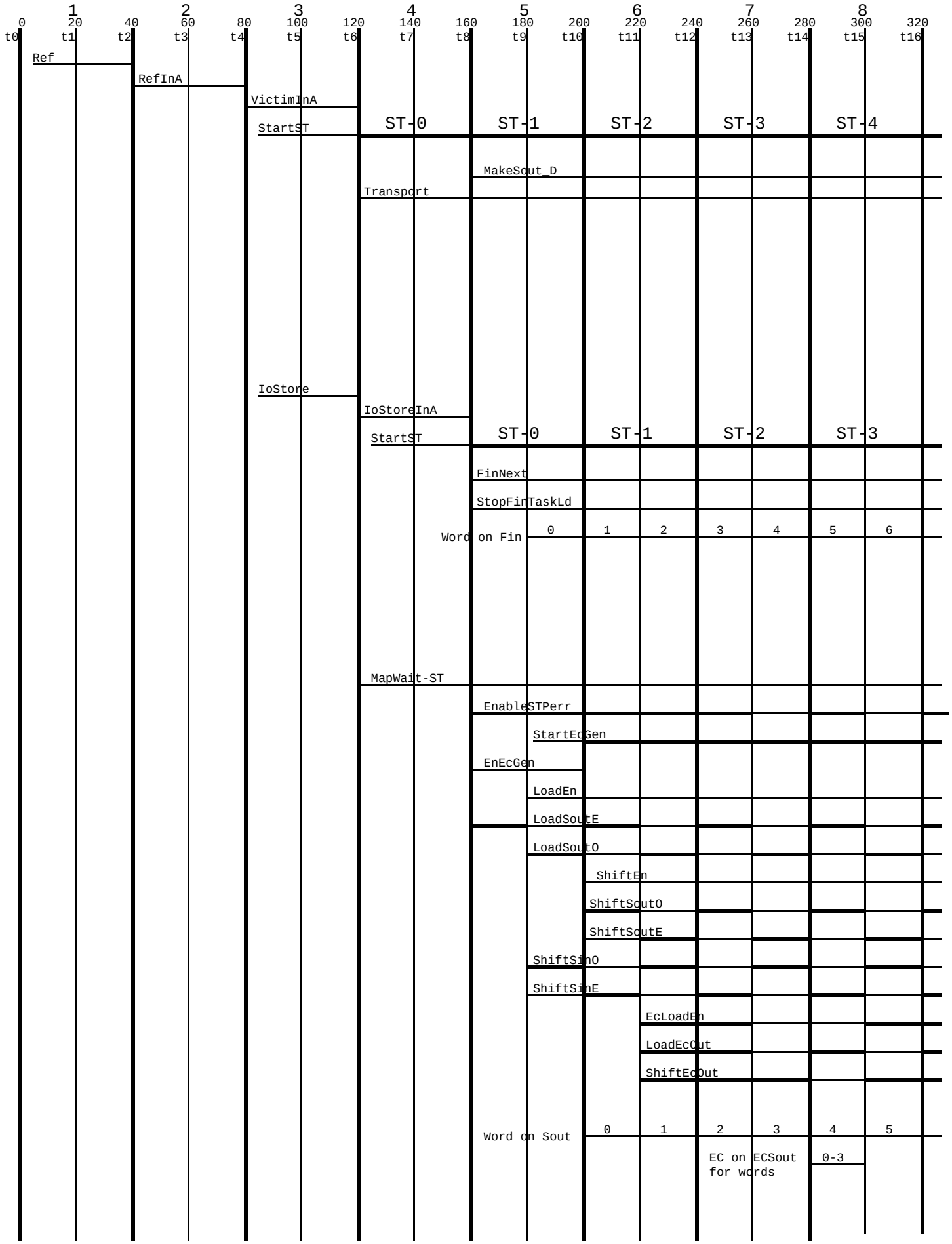


XEROX PARC/CSL	Project Dorado	Memory automata timing--16K chips	File <Clark>BigTime3.sil	Date 12/18/78	Key R=Ref, A=RefInA, V=VicInA, F=FlushStore Font 1=Read, Font 2=Write [7]=Idle state



XEROX PARC/CSL	Project	Memory timing diagram ST 1	File	Directory	Rev	Date	Page
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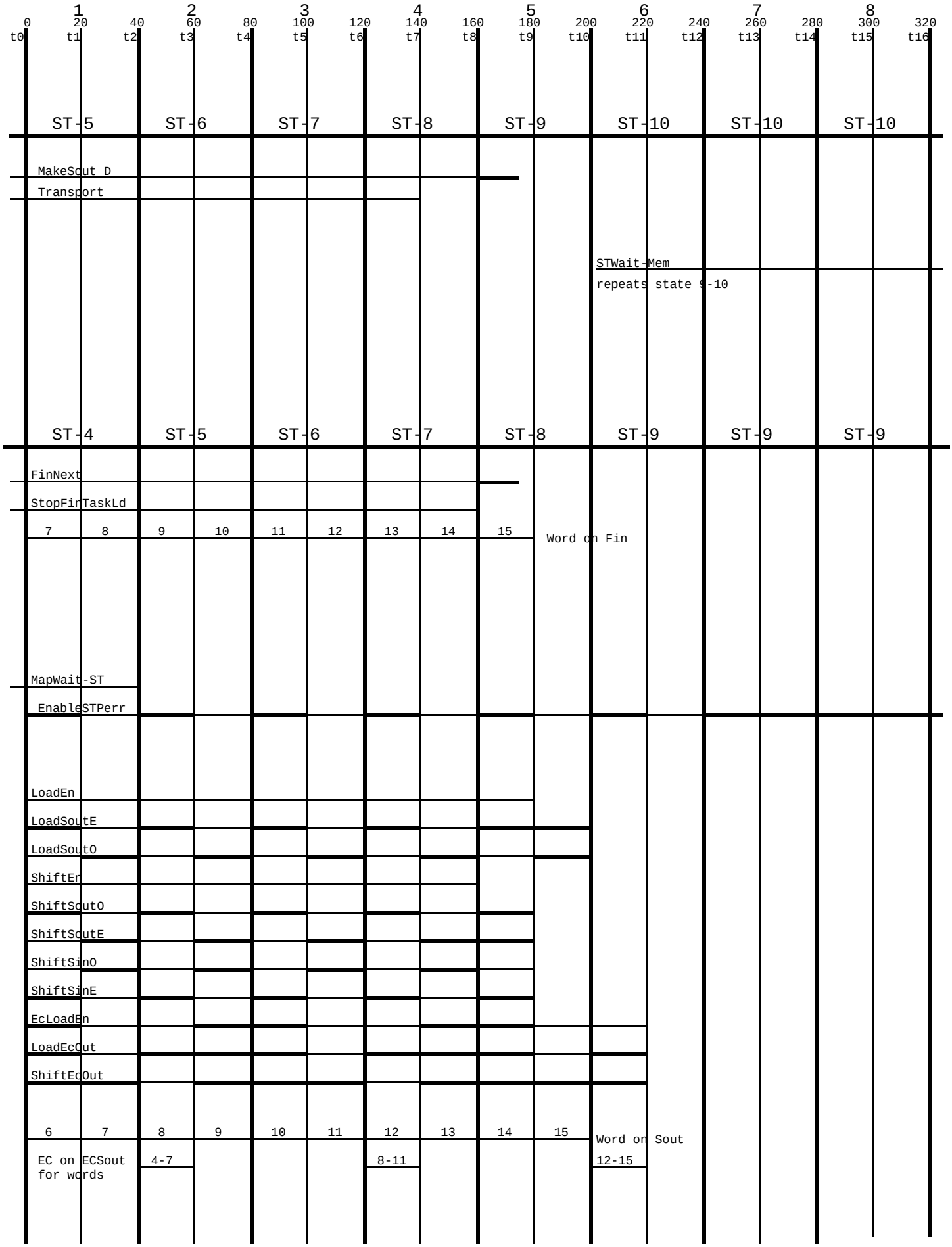

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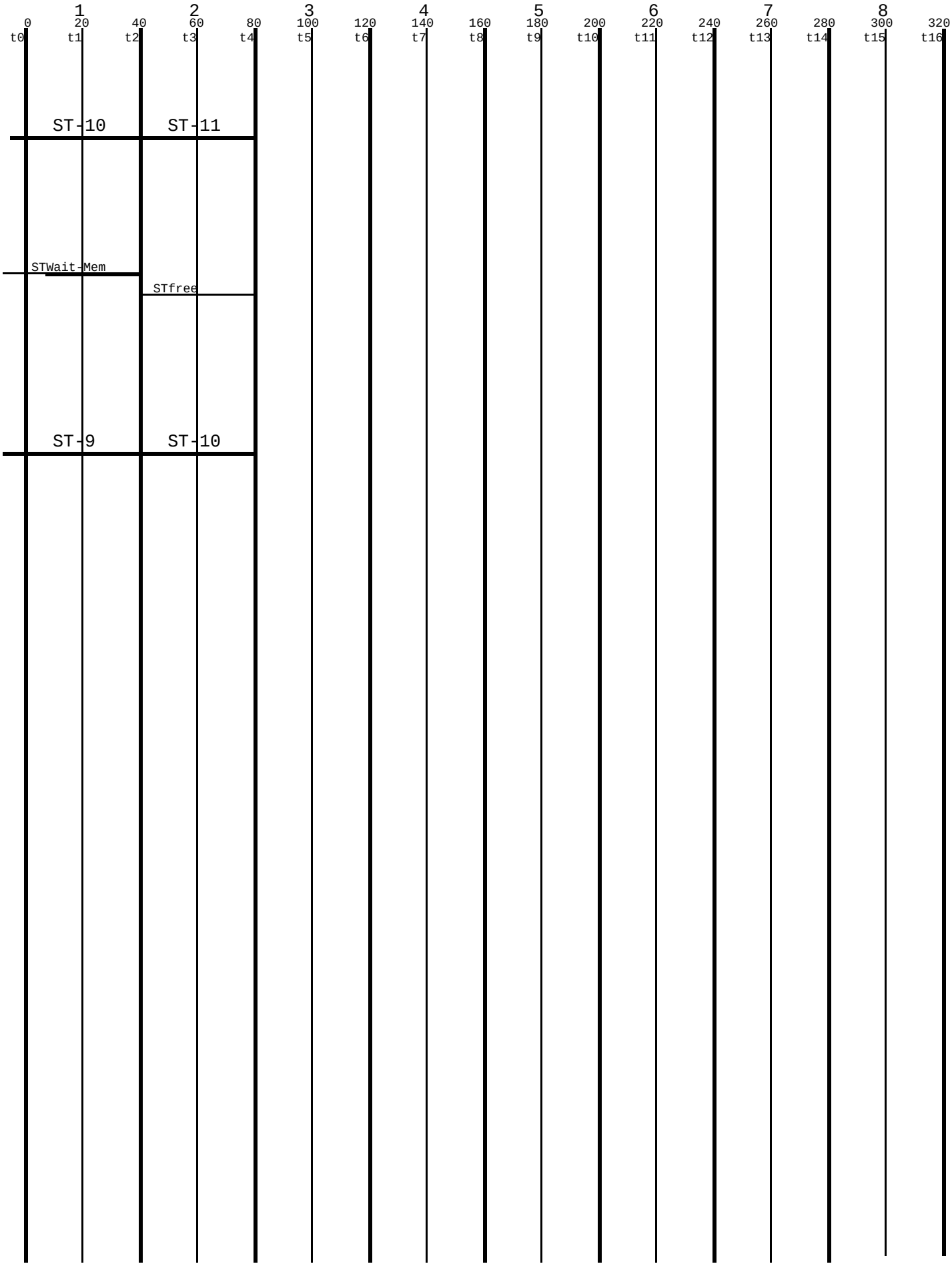

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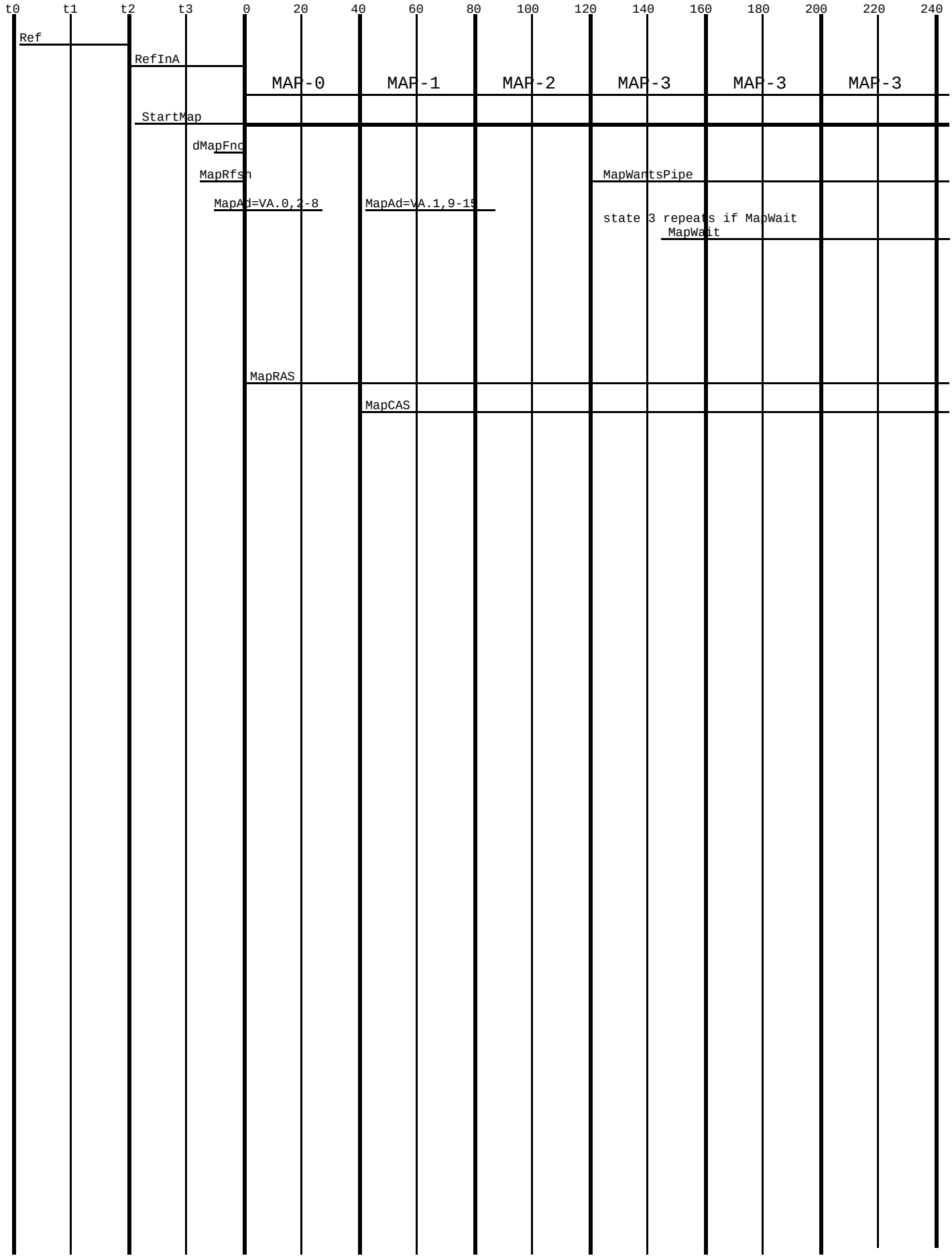

XEROX PARC/CSL	Project	Memory timing diagram Map 1	File	Directory	Rev	Date	Page
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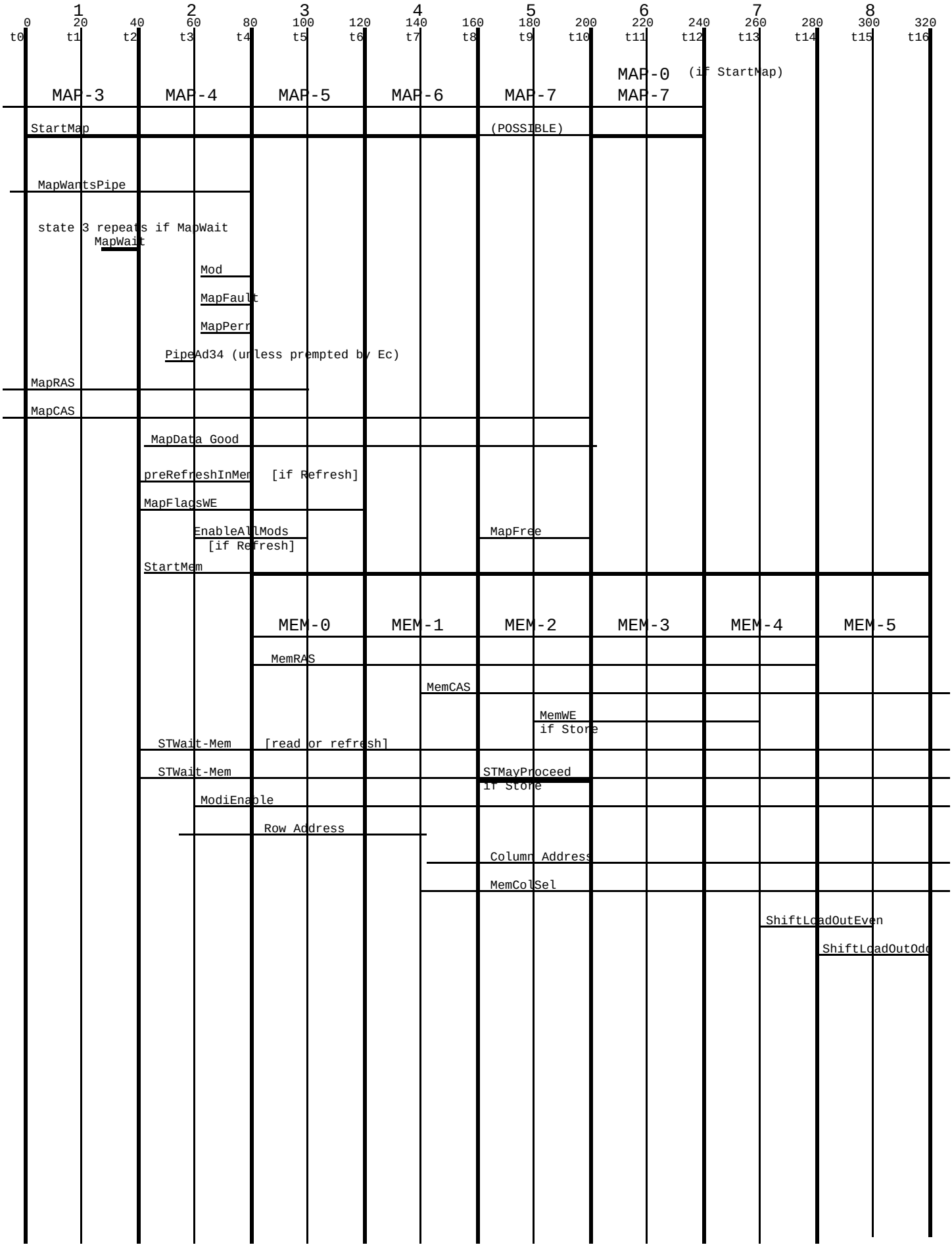

XEROX PARC/CSL	Project	Memory timing diagram Map 2	File	Directory	Rev	Date	Page
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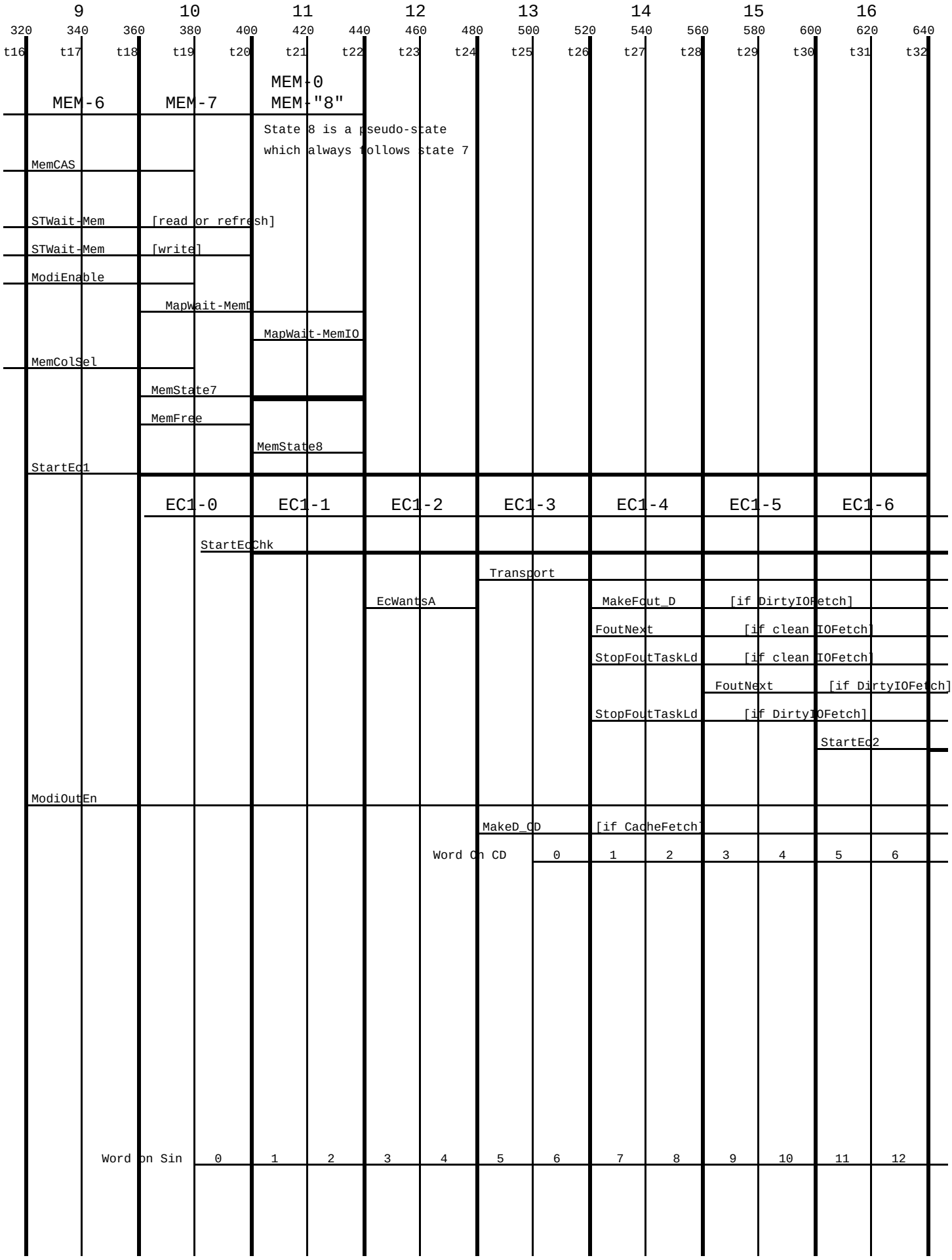
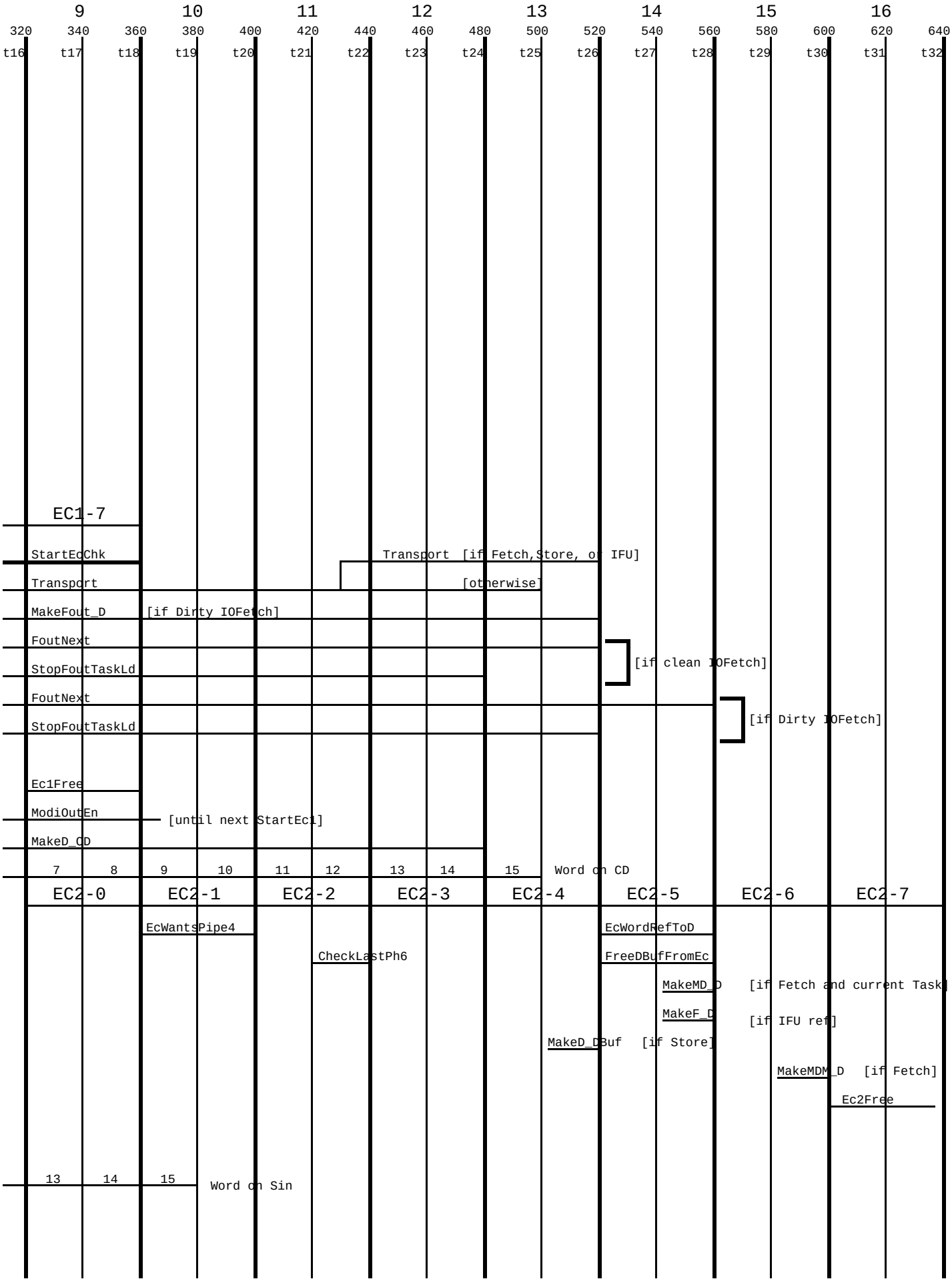


XEROX PARC/CSL	Project Dorado	Memory timing diagram Memory and Ec automata	File MemTimeEc1.sil	Directory <Clark>	Rev A	Date 1/30/78	Page



XEROX PARC/CSL	Project	Memory timing diagram Memory and Ec automata	File	Directory	Rev	Date	Page
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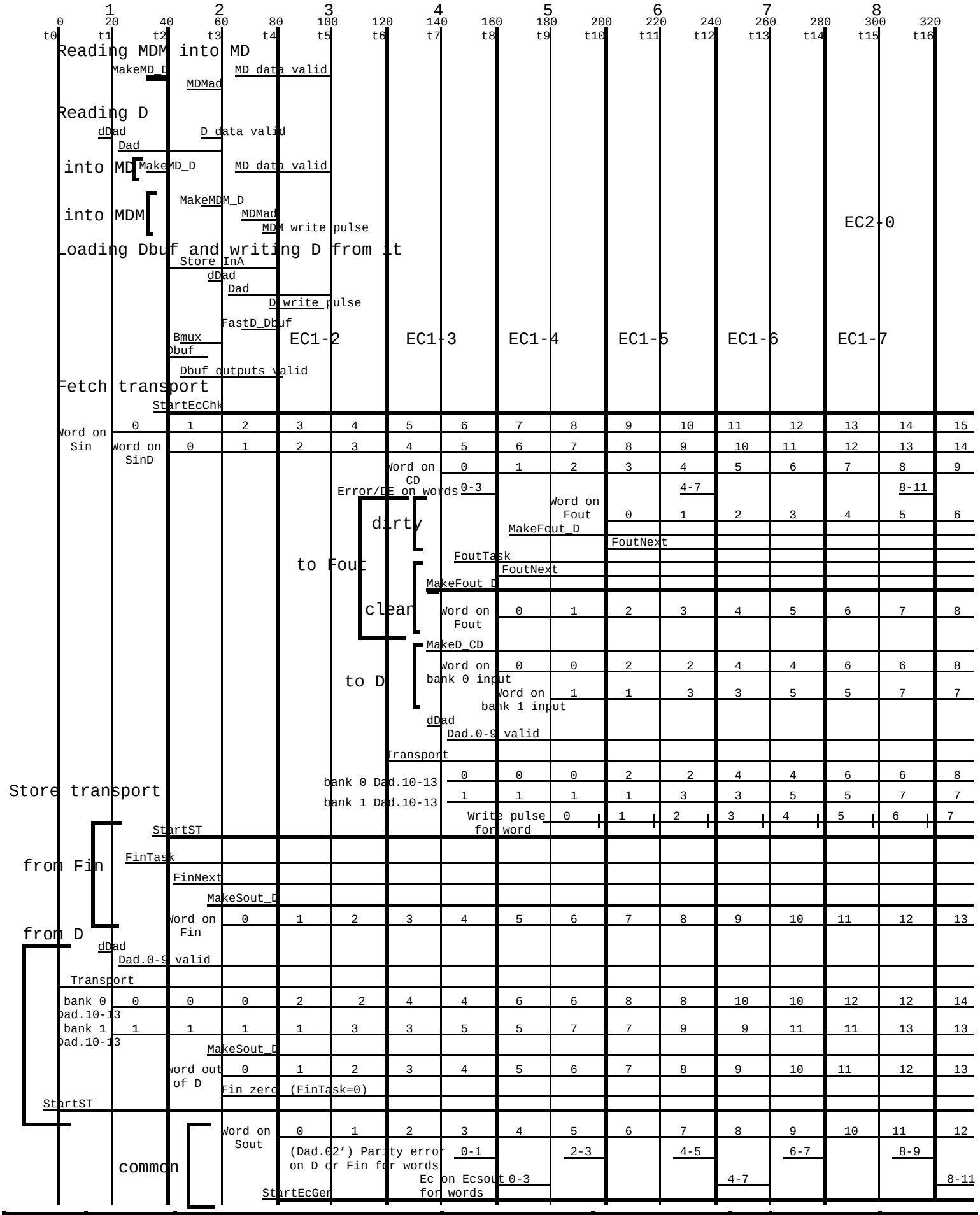

XEROX PARC/CSL	Project	MemD timing 1	File	Directory	Rev	Date	Page
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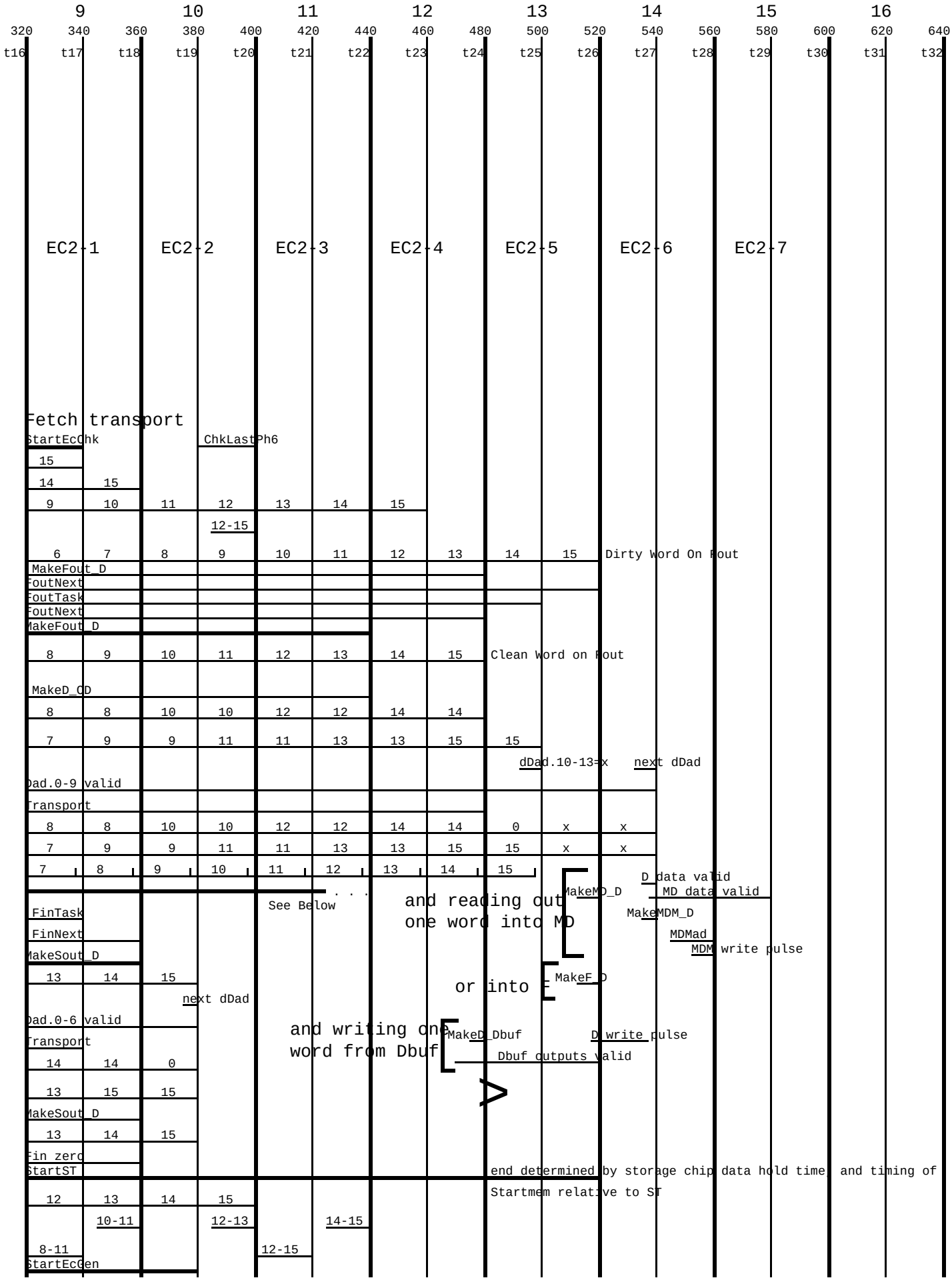

XEROX PARC/CSL	Project		File	Directory	Rev	Date	Page
	Dorado	MemD timing 2	MemDtiming2.sil	<DoradoDocs>	A	6/12/80	2 of 2