D A N D E L I O N S C H E M A T I C S

C e n t r a l P r o c e s s o r
w i t h
1 6 K C o n t r o l S t o r e
&
D E S E n c r y p t i o n

These drawings use the following [SIL] User.cm parameters:

0 = Helvetica10
1 = Helvetica7
3 = Gates32
5 = Sil.lb5
6 = Sil.lb6
7 = Sil.lb7
8 = CAS.lb8

All files are kept on [Indigo]<Dandelion>

Butler Lampson designed this processor.
Robert Garner implemented the design.
Tony West expanded the CS to 16K and added DES.
David Boggs engineered the printed circuit board.

Prom Name	Rev	Part No.	Location	Page	Comments
SwitchProm	R	F93427	i14	14	New Rev for 16K Control Store CP 256 x 4
KernPC16Prom	B	F93427	h14	15	Standard 256 x 4
CSIntProm	D	F93453	e20	22	Standard 1K x 4
StackVirtProm	I	F93427	h24	15	Standard 256 x 4
ScheduleProm	D	F93453	h18	14	Standard 1K x 4
ErrorProm	E	F93453	g14	15	Standard 1K x 4
IBProm-PC.0	G	F93453	i17	05	Standard 1K x 4
IBProm-PC.4	G	F93453	h17	05	Standard 1K x 4
DesMpProm.0	B	F93427	a16	33	Added to control DES logic 256 x 4
DesMpProm.4	B	F93427	b16	33	Added to control DES logic 256 x 4
DesSpProm	A	F93427	b15	33	Added to control DES logic 256 x 4

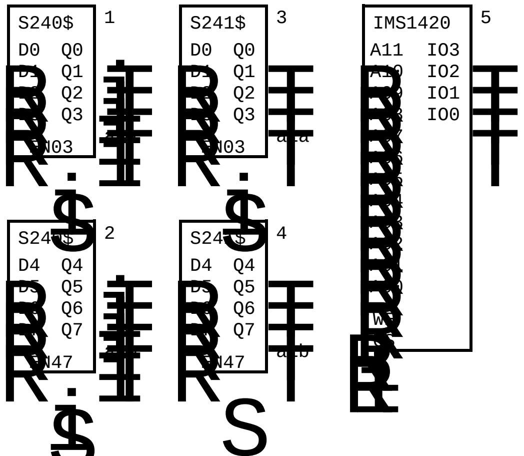
Prom files are stored on [Indigo]<Dandelion>CPE>Proms>*

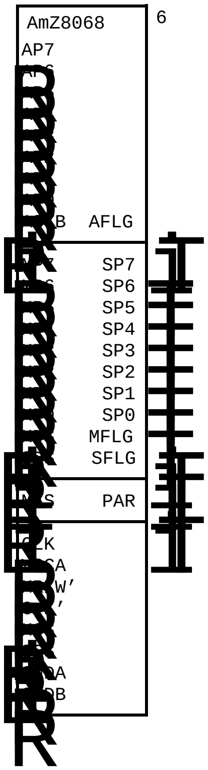
Bringover /a[Indigo]<Dandelion>CPE>DfFiles>Proms.df to fetch all files, sources, tools, etc.

Labels:

Switch i14 Rev-R	KernPC16 h14 Rev-B	CSInt e20 Rev-D	StackVirt h24 Rev-I	Schedule h18 Rev-D	Error g14 Rev-E	IB-PC.0 i17 Rev-G	IB-PC.4 h17 Rev-G	DesMp.0 a16 Rev-B	DesMp.4 b16 Rev-B	DesSp b15 Rev-A
Switch i14 Rev-R	KernPC16 h14 Rev-B	CSInt e20 Rev-D	StackVirt h24 Rev-I	Schedule h18 Rev-D	Error g14 Rev-E	IB-PC.0 i17 Rev-G	IB-PC.4 h17 Rev-G	DesMp.0 a16 Rev-B	DesMp.4 b16 Rev-B	DesSp b15 Rev-A
Switch i14 Rev-R	KernPC16 h14 Rev-B	CSInt e20 Rev-D	StackVirt h24 Rev-I	Schedule h18 Rev-D	Error g14 Rev-E	IB-PC.0 i17 Rev-G	IB-PC.4 h17 Rev-G	DesMp.0 a16 Rev-B	DesMp.4 b16 Rev-B	DesSp b15 Rev-A
Switch i14 Rev-R	KernPC16 h14 Rev-B	CSInt e20 Rev-D	StackVirt h24 Rev-I	Schedule h18 Rev-D	Error g14 Rev-E	IB-PC.0 i17 Rev-G	IB-PC.4 h17 Rev-G	DesMp.0 a16 Rev-B	DesMp.4 b16 Rev-B	DesSp b15 Rev-A

Font 4 Macros



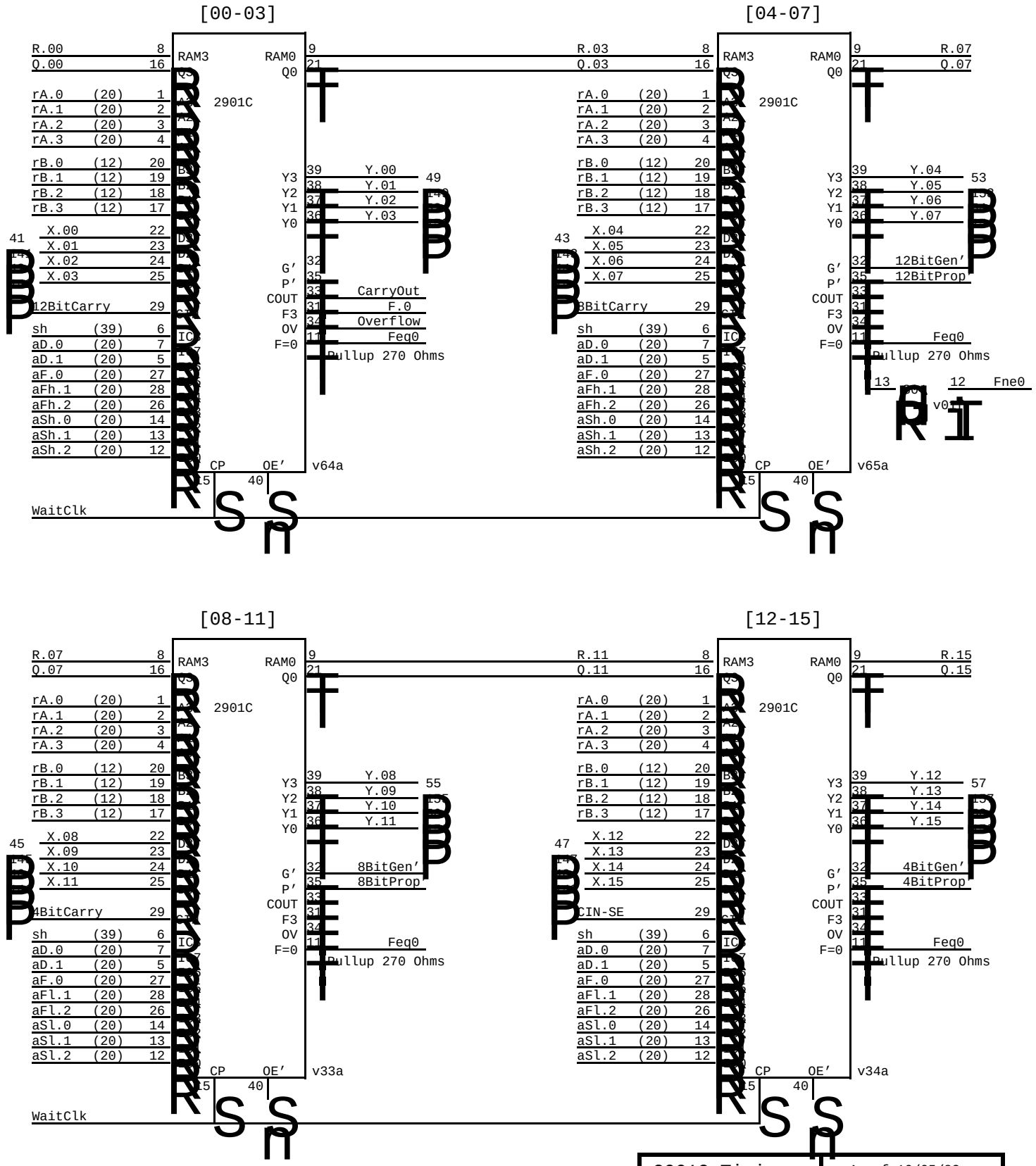


Important Notes:

Only macros 0-9 are valid component names and will not be expanded by Analyze
Some of these drawings contain instances of the macros above.
Those that do have a warning on them, see below left.
There is a corresponding CPEDict.analyze that should be prepended
to the dictionary chain.

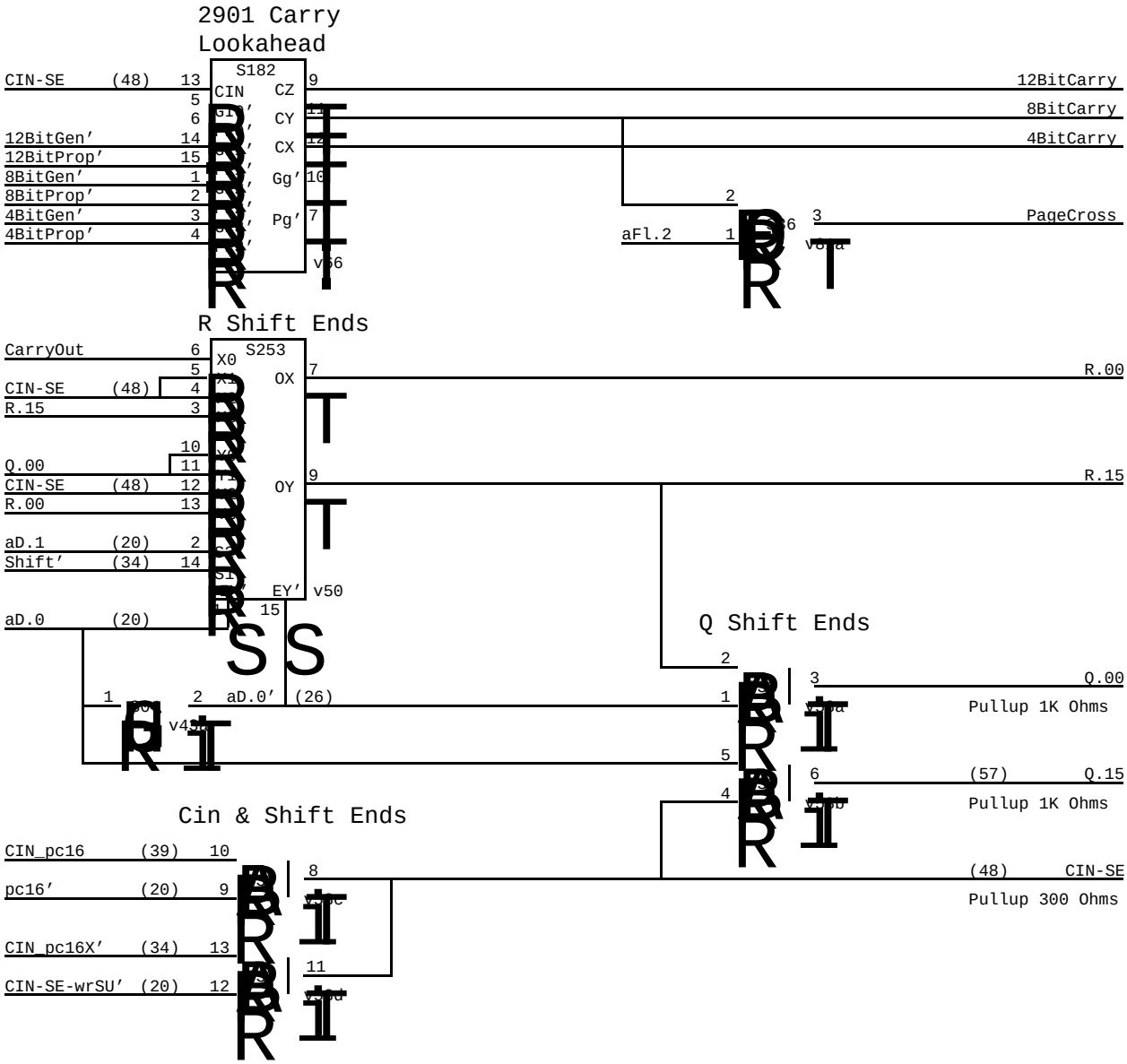
Warning: This drawing contains font 4 macros!

XEROX PARC	Project CPE	Reference Prom Index & Font 4 Macros	File CPE01.sil	Drawn by Tony West	Rev Ba	Date 5/30/83	Page 02



2901C Timing			As of 10/05/82		
Setup	sh,,aD	10			
Setup	aF	30			
Setup	aS	30			
rA	to G,P	37		rA	to Y 40
D	to G,P	30		D	to Y 30
				Cn	to Y 22
rA	to Cout	40		aS	to Y 35
D	to Cout	30		aF	to Y 35
Cin	to Cout	20		aD	to Y 25

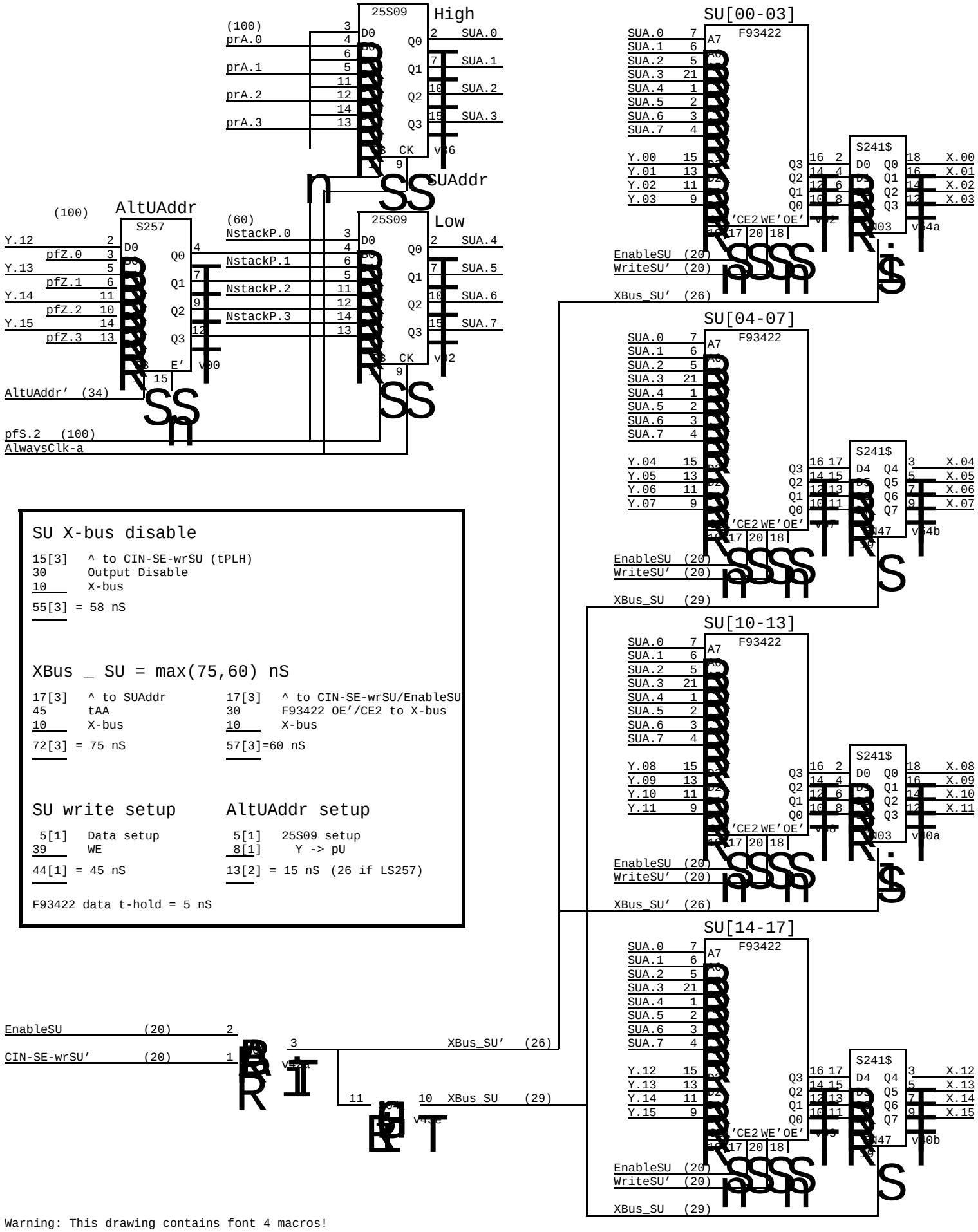
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	2901 ALUs	CPE02.sil	Bob Garner	Ba	5/30/83	03



aD.1	Shift	Shift configuration
0	0	Cout — R — ~ — Q — ~Cin
0	1	Cin — R — ~ — Q — ~Cin
1	0	Cin — R — Cin
1	1	R

aD.0 = 0 implies right shift

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	Lookahead, Shift Ends, Cin	CPE03.sil	Bob Garner	Ba	5/30/83	04



SU X-bus disable

15[3] ^ to CIN-SE-wrSU (tPLH)
30 Output Disable
10 X-bus

55[3] = 58 nS

XBus _ SU = max(75,60) nS

17[3] ^ to SUAddr
45 tAA
10 X-bus

72[3] = 75 nS

17[3] ^ to CIN-SE-wrSU/EnableSU
30 F93422 OE'/CE2 to X-bus
10 X-bus

57[3]=60 nS

SU write setup

5[1] Data setup
39 WE

44[1] = 45 nS

AltUAddr setup

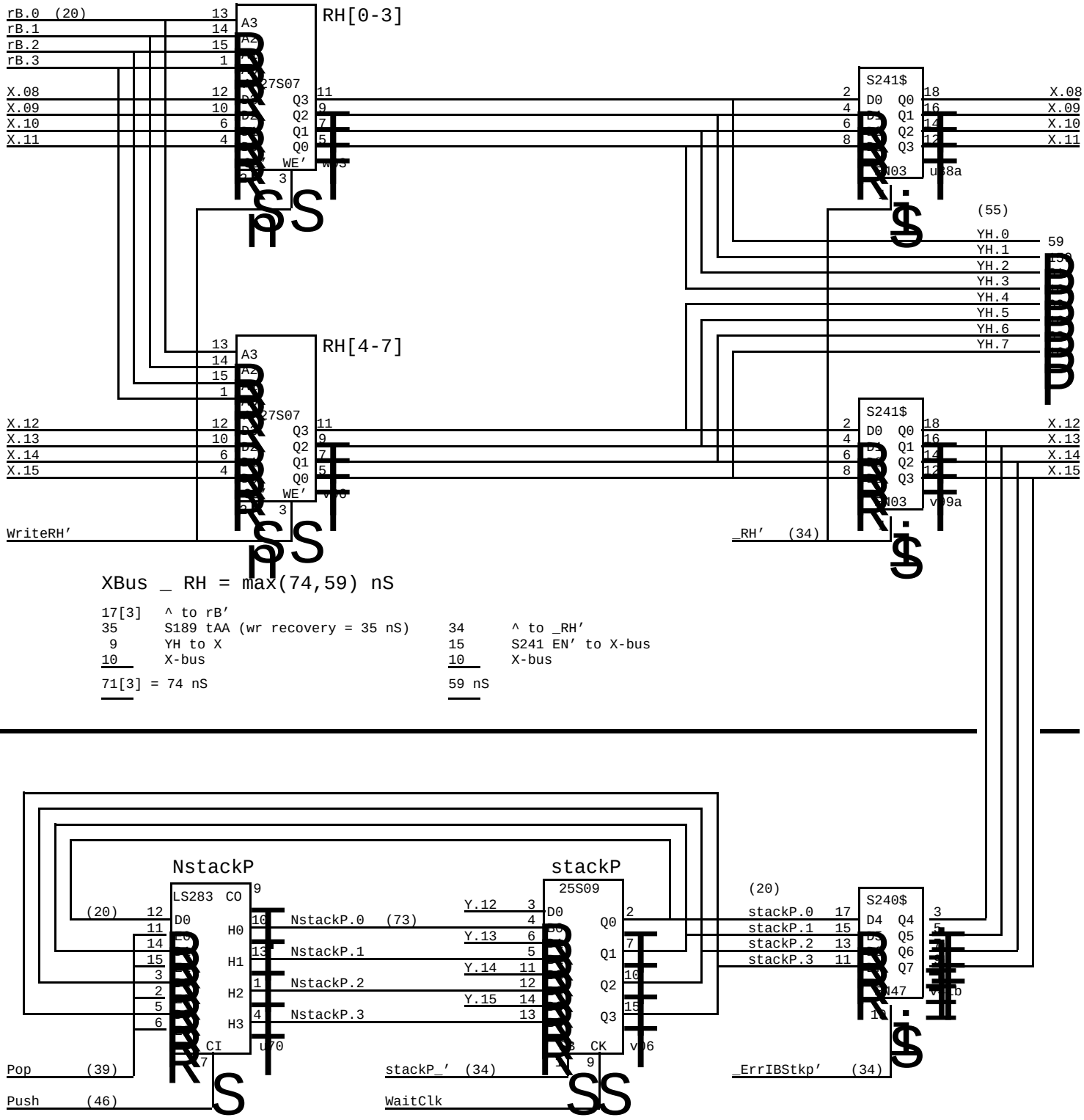
5[1] 25S09 setup
8[1] Y -> pU

13[2] = 15 nS (26 if LS257)

F93422 data t-hold = 5 nS

Warning: This drawing contains font 4 macros!

XEROX PARC	Project CPE	Drawing SU Registers	File CPE04.sil	Designer Bob Garner	Rev Ba	Date 5/30/83	Page 05



XBus _ RH = max(74,59) nS

17[3]	^ to rB'		34	^ to _RH'
35	S189 tAA (wr recovery = 35 nS)		15	S241 EN' to X-bus
9	YH to X		10	X-bus
10	X-bus			
71[3] = 74 nS			59 nS	

Push Timing

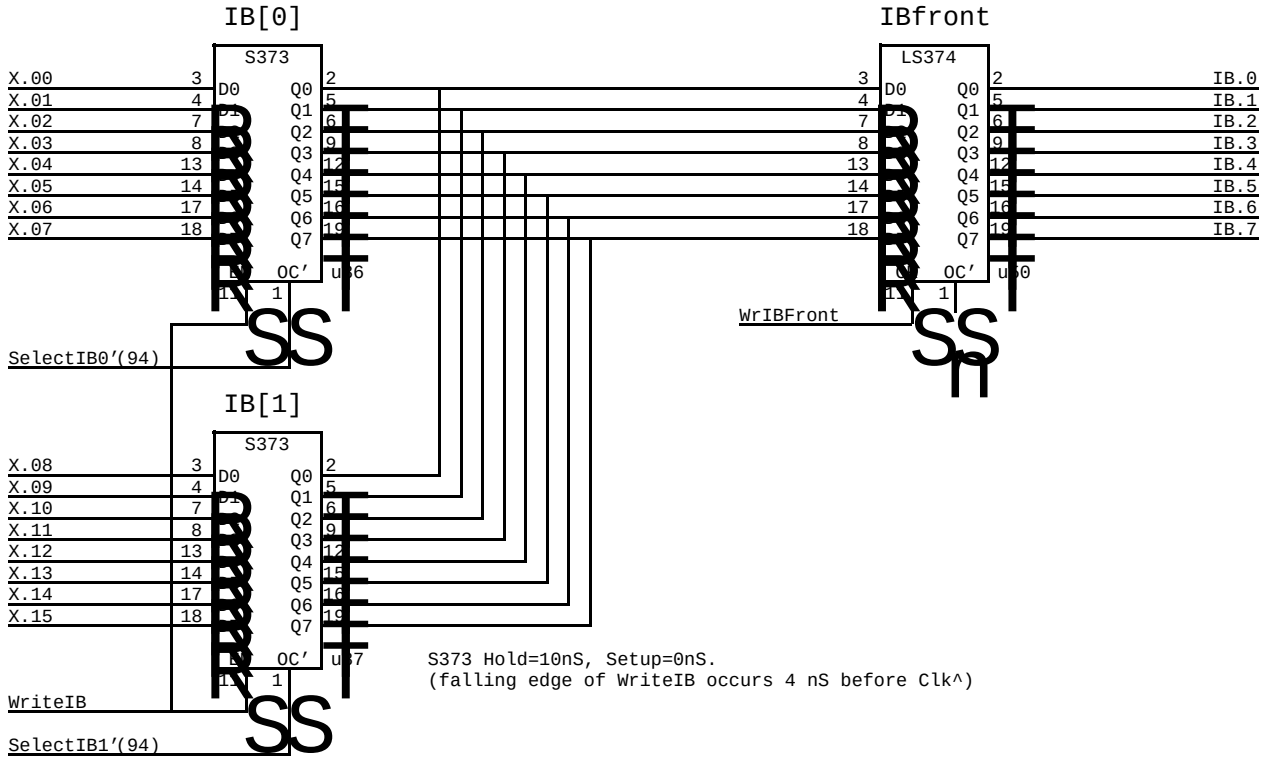
46	^ to Push
24[3]	Push to NstackP
5[1]	25S09 setup
75[4] = 79 nS	

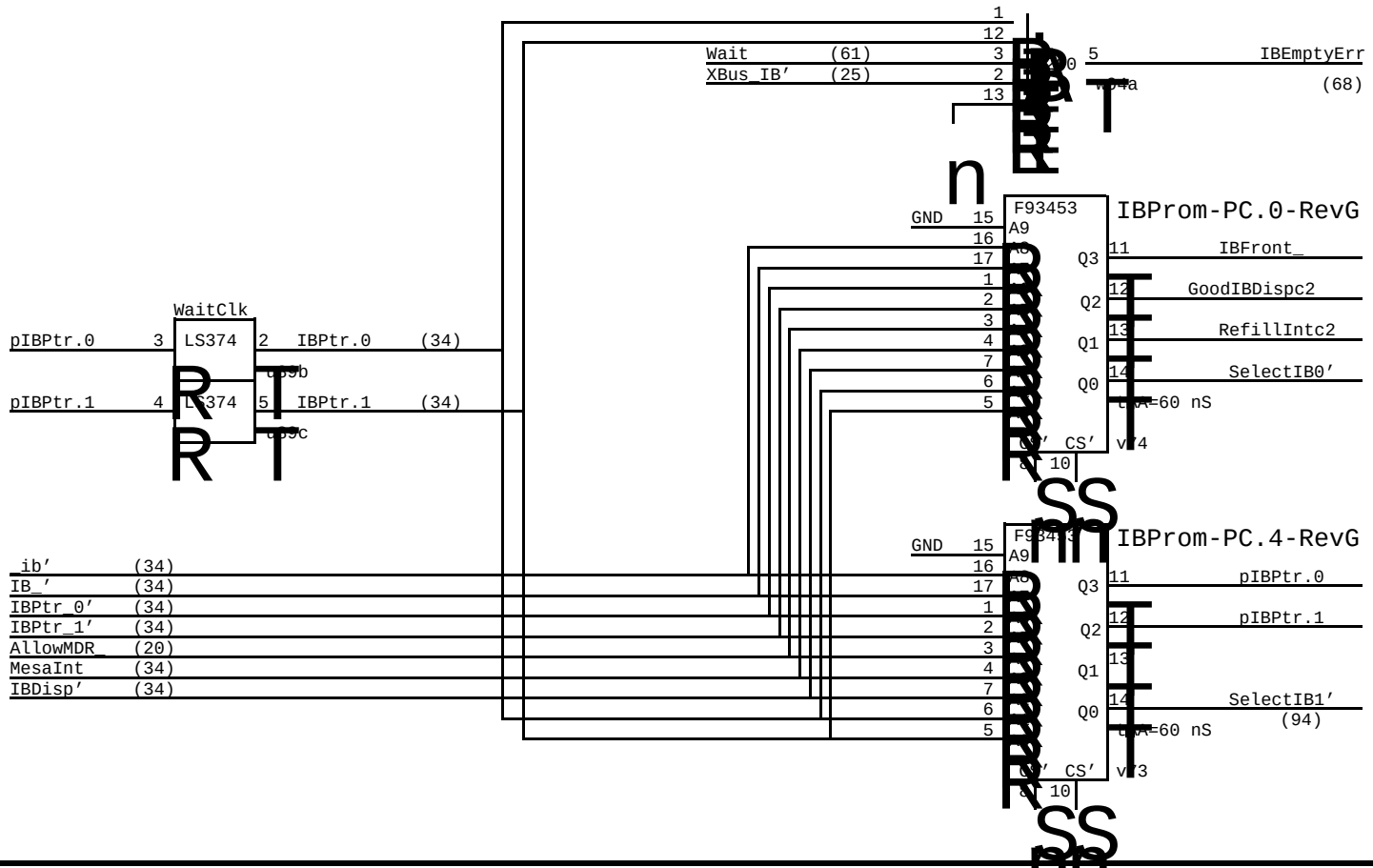
XBus _ stackP = max(59, 38) nS

17[3]	^ to stackP	34	^ to _ErrIntstackP'
7	S240 data to X-bus	15	S240 EN' to X-bus
10	X-bus	10	X-bus
34[3] = 38 nS		59 nS	

Warning: This drawing contains font 4 macros!

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	RH, stackP	CPE05.sil	Bob Garner	Ba	5/30/83	06





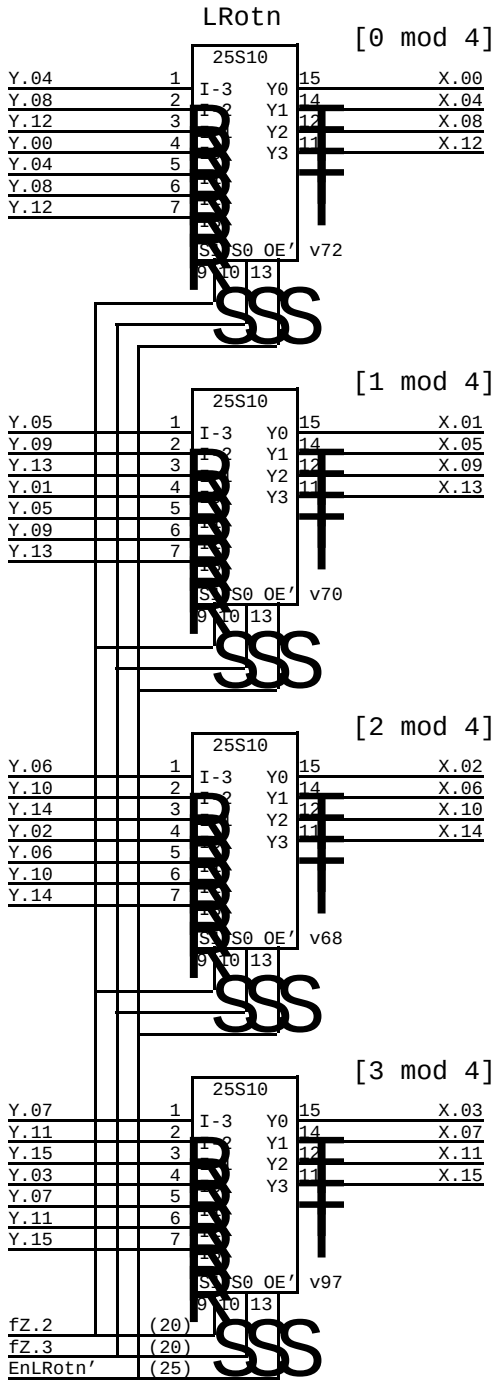
Timing for HM7649 IBProm (Old Proms -- not 2nd sourced)

IBFront _ Xbus = (x+37, x+36) nS

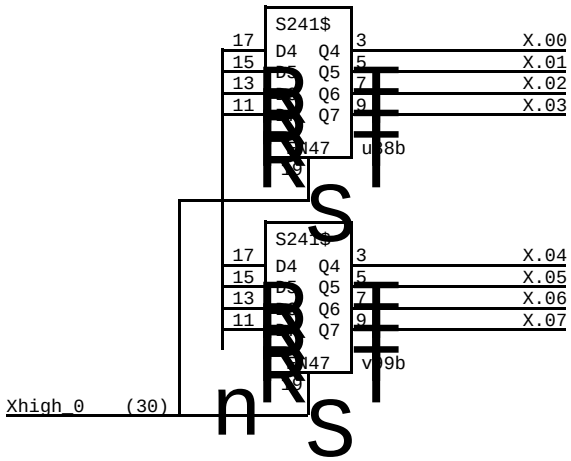
IBfront_IB[1]

x	Xbus to IB	x	Xbus to IB	94	WriteIB rises	34	^ to IBPtr_1'
43	WriteIB rises 43 nS before end of cycle	13[1]	S373 Data to NB	18[2]	S373 EN to NB	60	tAA
- 6	Difference between S373 "EN to Q" and "Data to Q"	20[2]	LS374 setup	20[2]	LS374 setup	18[2]	SelectIB1' to NB
x+37 nS	18[2] - 13[1] = 6 nS. Data can arrive 6 nS after WriteIB goes high.	x+36 nS		132[4]=136 nS		20[2]	LS374 setup
						132[4]=136 nS	

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	Instruction Buffer	CPE06.sil	Bob Garner	Ba	5/30/83	07



fZ.2	fZ.3	Rotate
0	0	Left 0
0	1	Left 12
1	0	Left 8
1	1	Left 4



Zero disable X-bus

```
30      ^ to Xhigh_0
15      S241 EN to X-bus
10      X-bus
55 nS
```

Xbus[0-7] _ 0

```
30      ^ to Xhigh_0
15      S241 OE
10      X-bus
55 nS
```

Xbus _ Y LRotn = max(y+22, 56, 50) nS

```
 y      ^ to Y bus
12      25S10 data in to out
10      X-bus
 y + 22 nS
```

```
25      ^ to EnLRotn'
21      25S10 OE
10      X-bus
56 nS
```

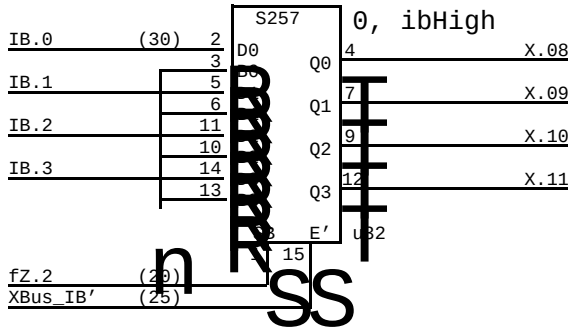
```
20      ^ to fZ.2
20      25S10 Select to X-bus
10      X-bus
50 nS
```

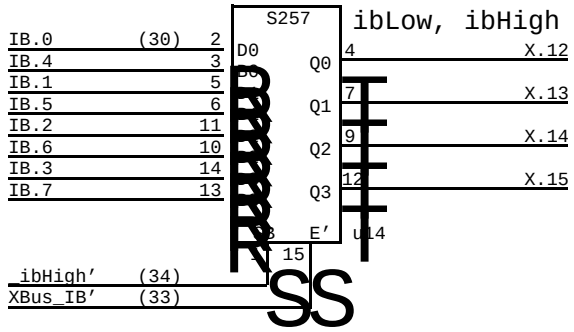
LRotn disable X-bus

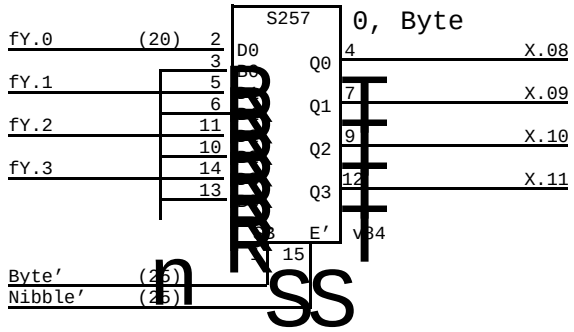
```
25      ^ to EnLRotn'
15      25S10 OE' to X-bus
10      X-bus
50 nS
```

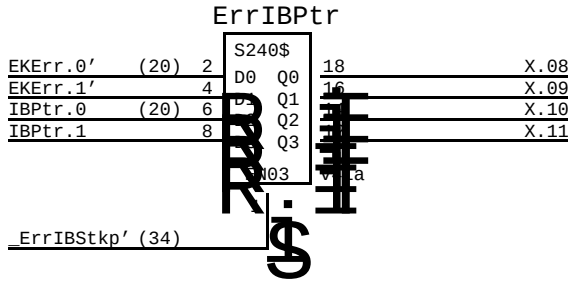
Warning: This drawing contains font 4 macros!

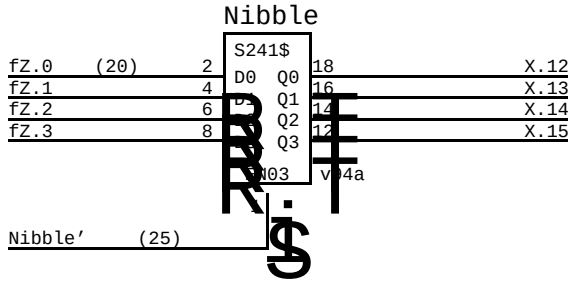
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	X Bus: LRotn, RH, ZeroHigh X	CPE07.sil	Bob Garner	Ba	5/30/83	08











IB disable X-bus

25 ^ to XBus_IB'
14 S257 E' to X-bus
10 X-bus

49 nS

Byte disable X-bus

25 ^ to Nibble'
14 S257 E' to X-bus
10 X-bus

49 nS

Nibble disable X-bus

25 ^ to Nibble'
15 S241 EN' to X-bus
10 X-bus

50 nS

Xbus_IB=max(56,56,59) nS

34[4] ^ to IB
8 S257 data to Xbus
10 X-bus

52[4] = 56 nS

25 ^ to Xbus_IB'
21 S257 E' to Xbus
10 X-bus

56 nS

34 ^ to_ibHigh'
15 S257 SB to Xbus
10 X-bus

59 nS

Xbus _ Nibble = max(39, 50) nS

20 ^ to fZ
9 S241 data to X-bus
10 X-bus

39 nS

25 ^ to Nibble'
15 S241 EN' to X-bus
10 X-bus

50 nS

Xbus _ Byte = max(38, 56,50) nS

20 ^ to fY
8 S257 data to X-bus
10 X-bus

38 nS

25 ^ to Nibble'
21 S257 E' to X-bus
10 X-bus

56 nS

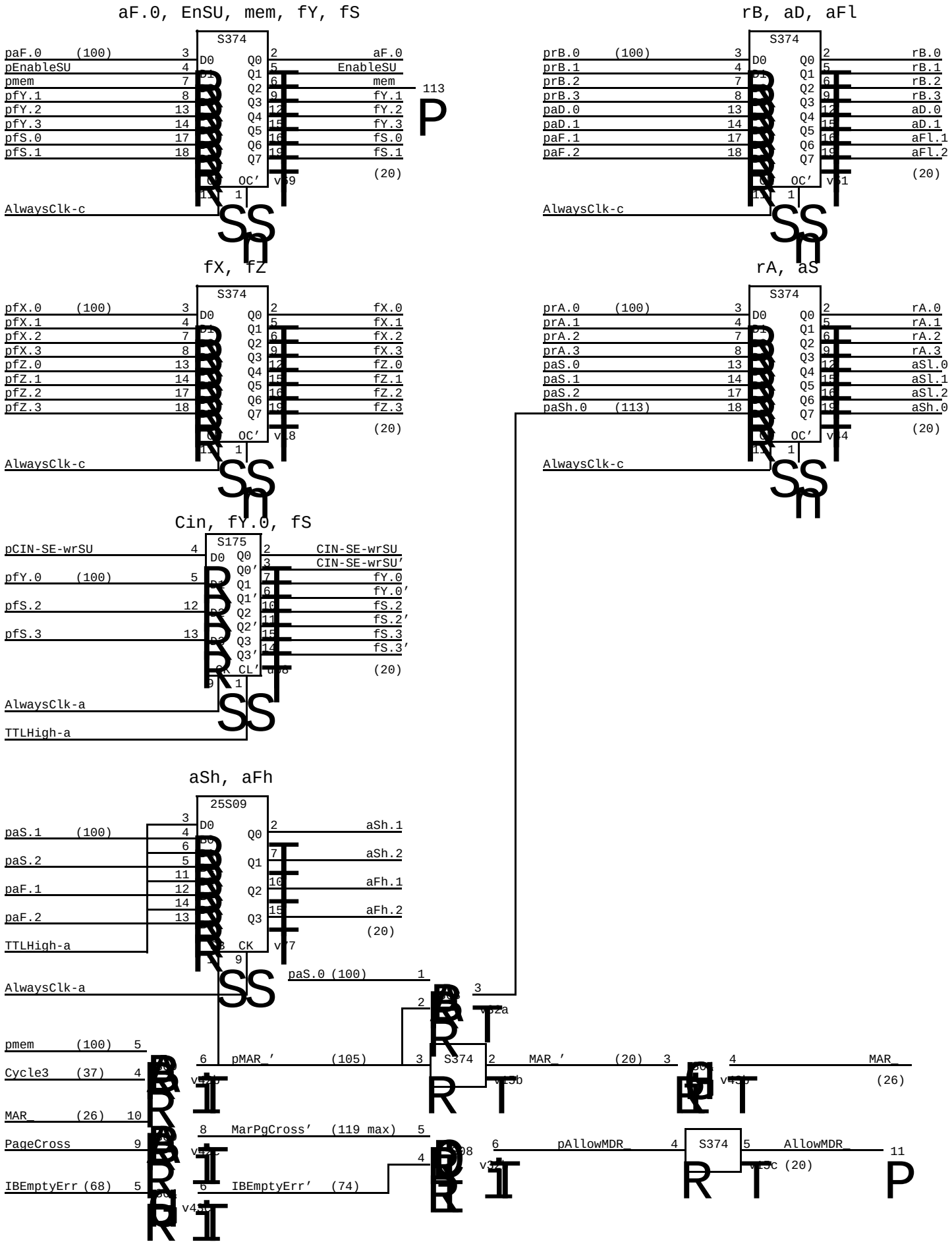
25 ^ to Byte'
15 S257 SB to Xbus
10 X-bus

50 nS

See stackP timings for ErrIBPtr

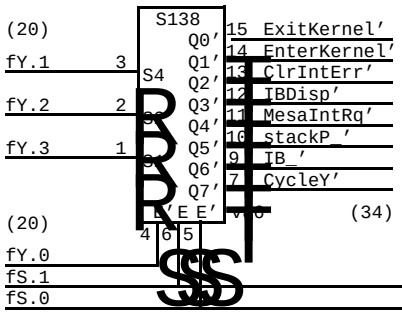
Warning: This drawing contains font 4 macros!

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	X Bus: IB, Constants, ErrIntstackP	CPE08.sil	Bob Garner	Ba	5/30/83	09

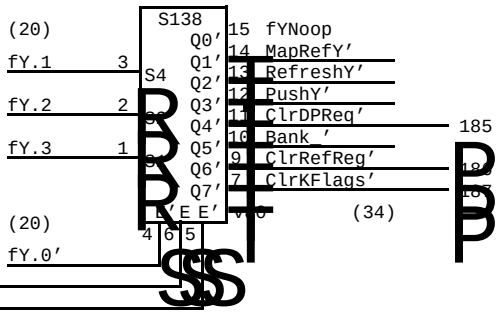


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	Microinstruction Register	CPE09.sil	Bob Garner	Ba	5/30/83	10

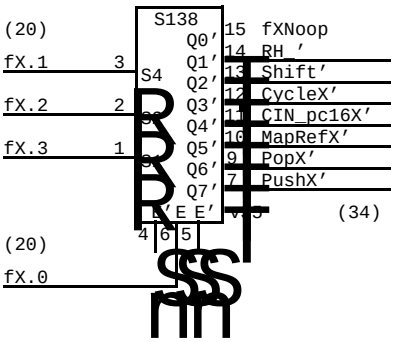
fYNorm - Low



fYNorm - High



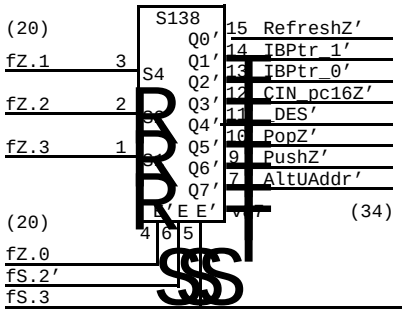
fX - High



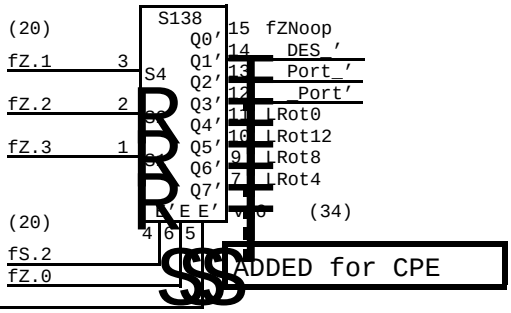
Bank_' replaces ClrIOPReq', which was connected to 184 on backplane

fX - Low is pCall/pRet

fZNorm - Low



fZNorm - High



There are 2 spare fZ decodes available for future expansion

Notes on 16K CP additions:

Note that Bank_' is fY=D, not fZ=4, as stated in the Dandelion Hardware Manual!

Bank_' replaces ClrIOPReq', which is now obsolete. ClrIOPReq' was also connected to backplane pin 184.

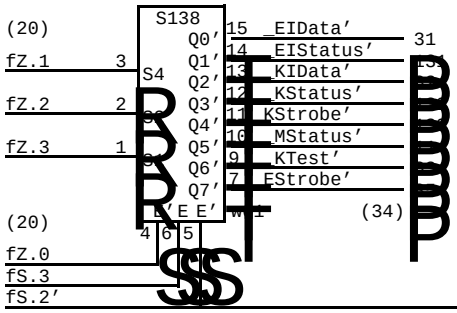
The meaning of Des_YBus' depends on which cycle it is activated in:

Des_YBus' in C2 means Write Des Address
Des_YBus' in C1 or C3 means Write Des Da

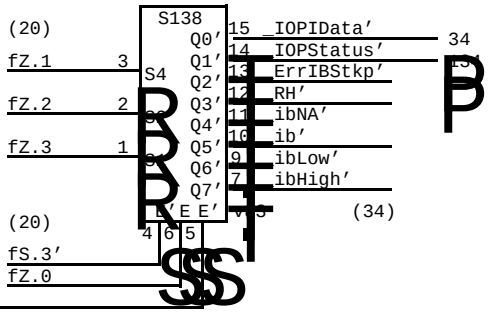
XBus_Des' can be activated in any cycle
See page sCPE31 for details of DES logic

The fZNorm-High decoder has been added in the 16K CP to derive the DES decodes.

IOXIn - Low



IOXIn - High



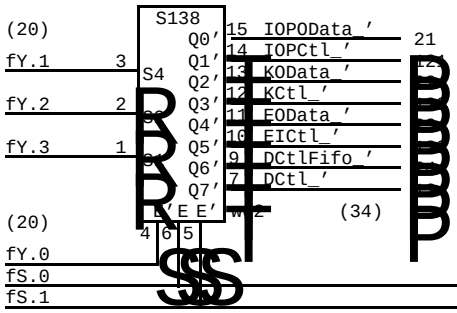
S138 Timing:

Propagation delays

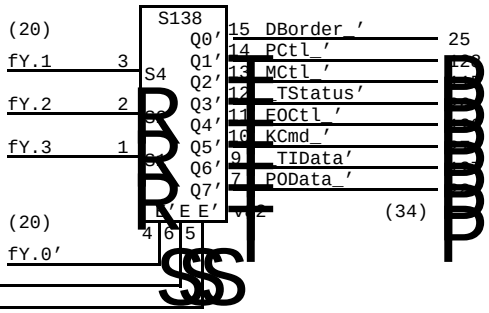
from Selects to Q'	14nS
from Enables to Q'	13nS

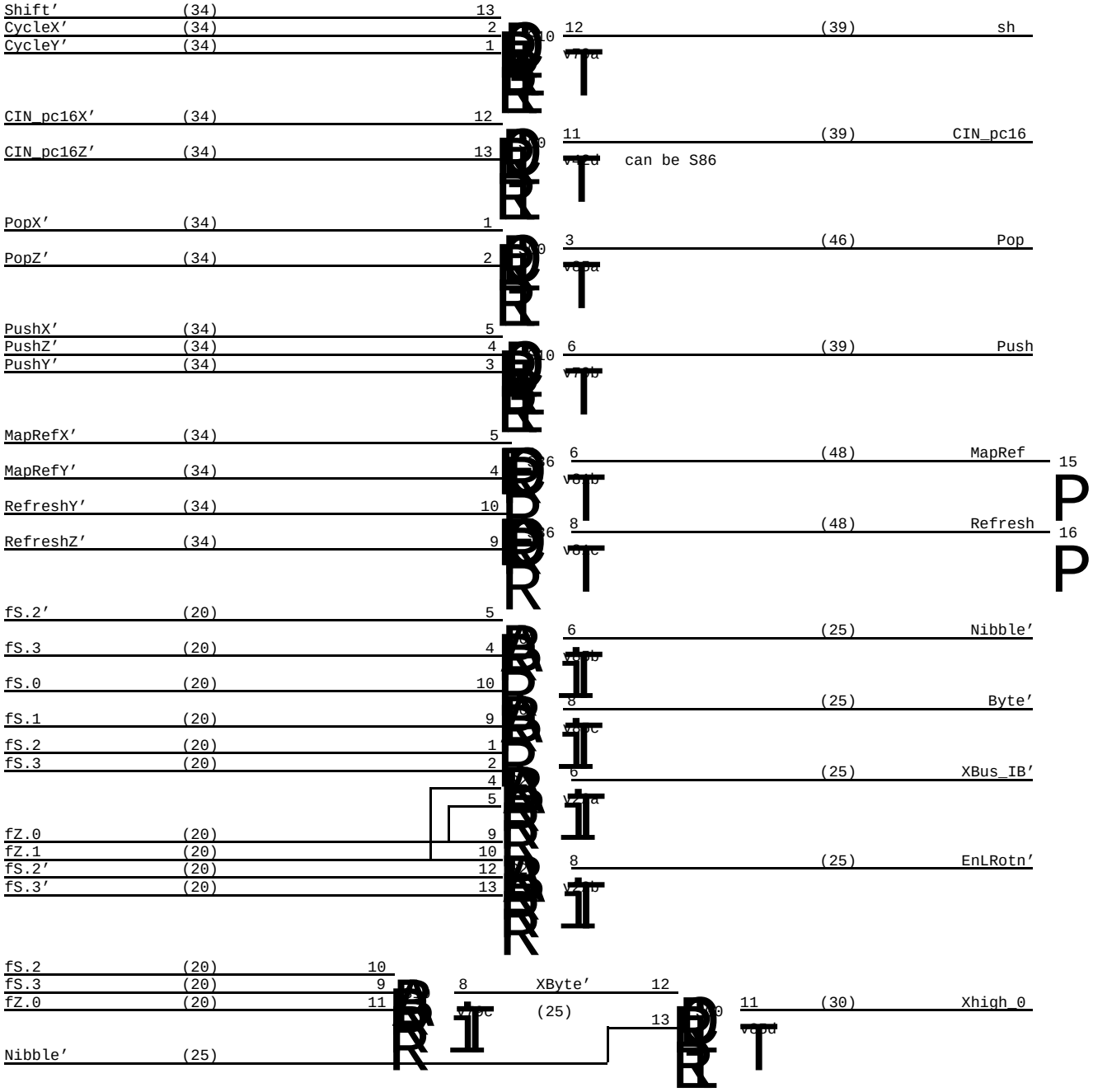
These timings are very conservative!

IOOut - Low

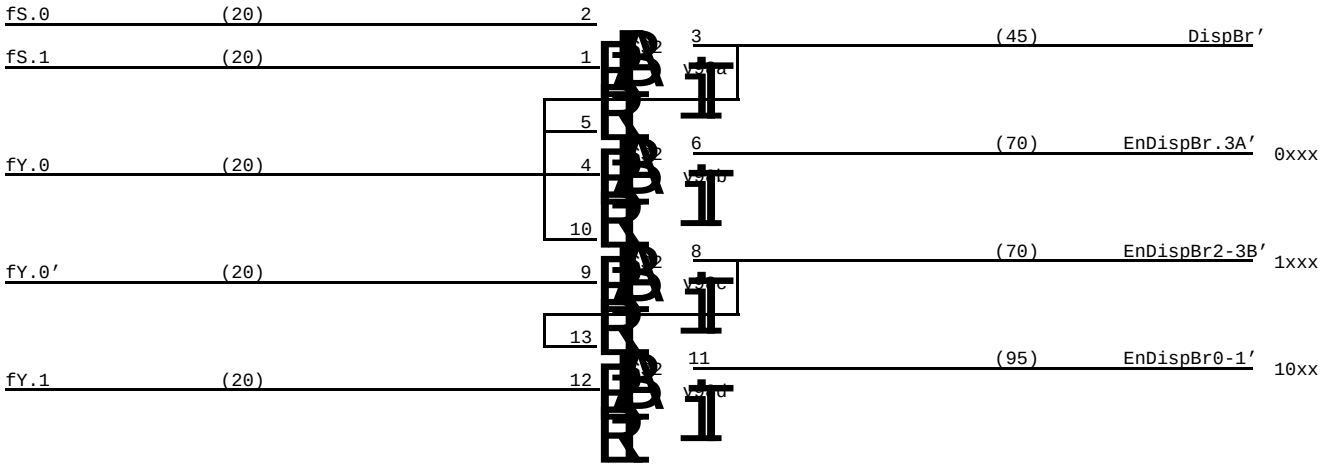


IOOut - High

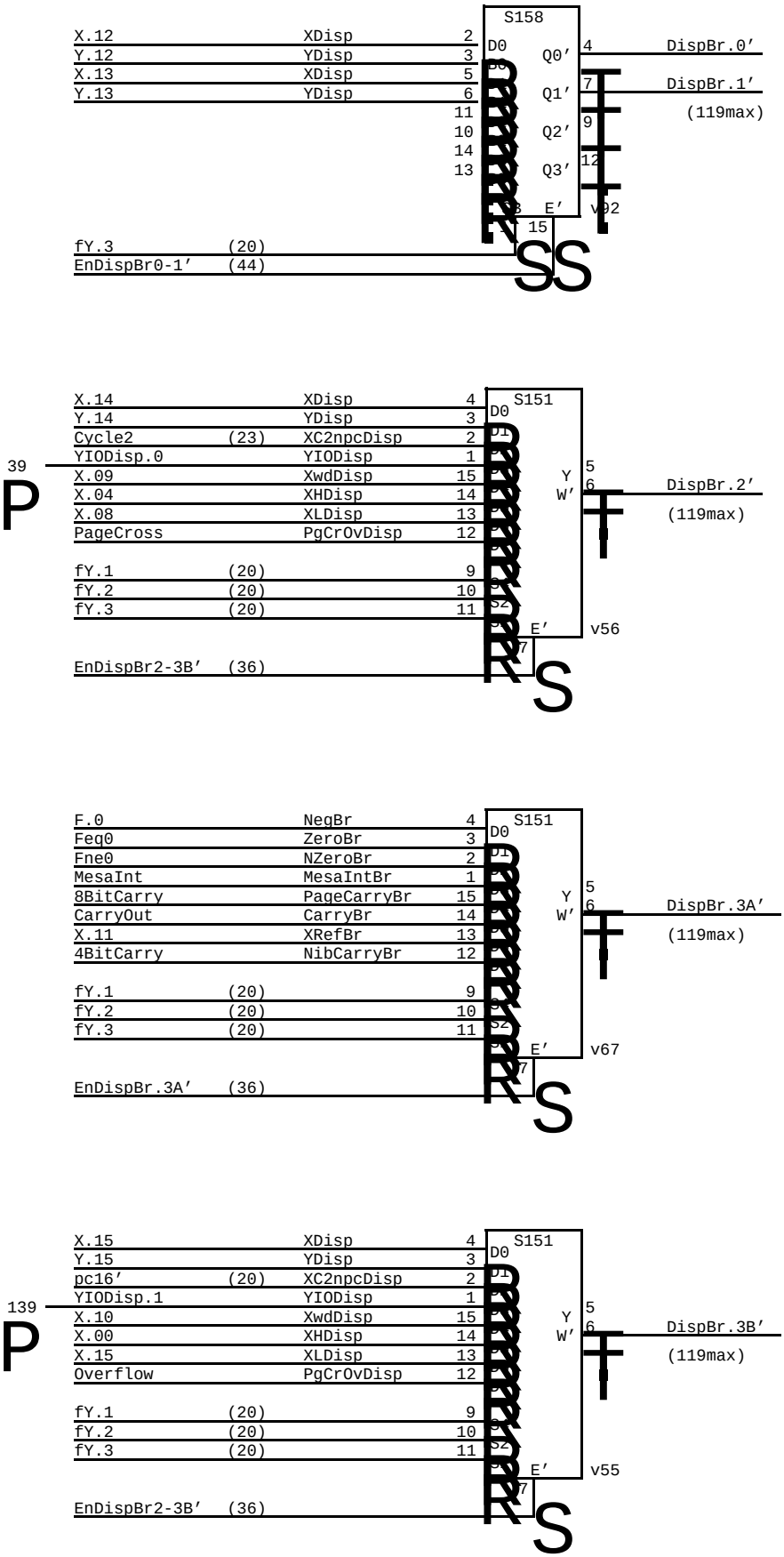




EnDispBr



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	Microinstruction Decoding II	CPE11.sil	Bob Garner	Ba	5/30/83	12



DispBr[0-1] = max(c+32,69,133

20 ^ to fY
24[3] S151 select to DispBr
18 DispBr′ setup

64[3]=69

95 ^ to EnDispBr0-1′
18[2] S151 E′ to DispBr
18 DispBr′ setup

131[2] = 133 nS

c condition source
12[2] S151 data to DispBr
18 DispBr′ setup

c+30[2]= c+32

DispBr Setup

5 S00 in to pTC
6[1] S64 in to pNIA
5[1] 25S09/S374 setup

18 nS

DispBr[2-3]=max(c+26,55,103)

20 ^ to fY
15[2] S151 select to DispBr
18 DispBr′ setup

51[4]=55 nS

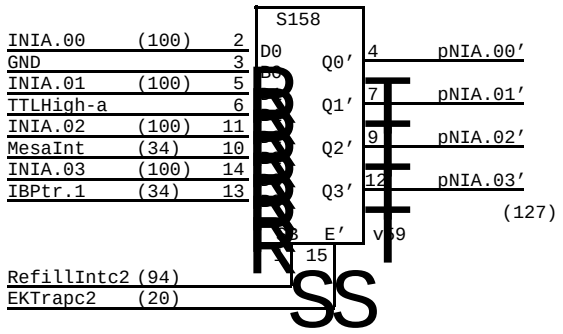
70 ^ to EnDispBr.3A′
13[2] S151 E′ to DispBr
18 DispBr′ setup

101[2] = 103 nS

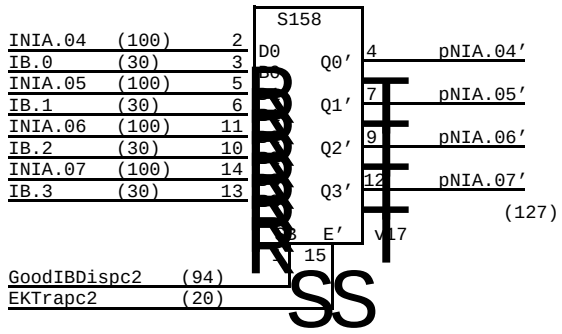
c condition source
7[1] S151 data to DispBr
18 DispBr′ setup

c+23[3]=c+26 nS

pNIA[0-3]



pNIA[4-7]

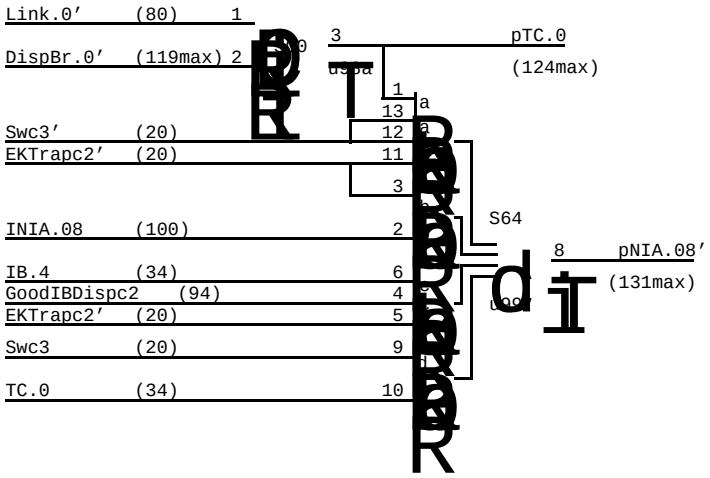


pNIA[0-7]=max(127, 120, 46) nS

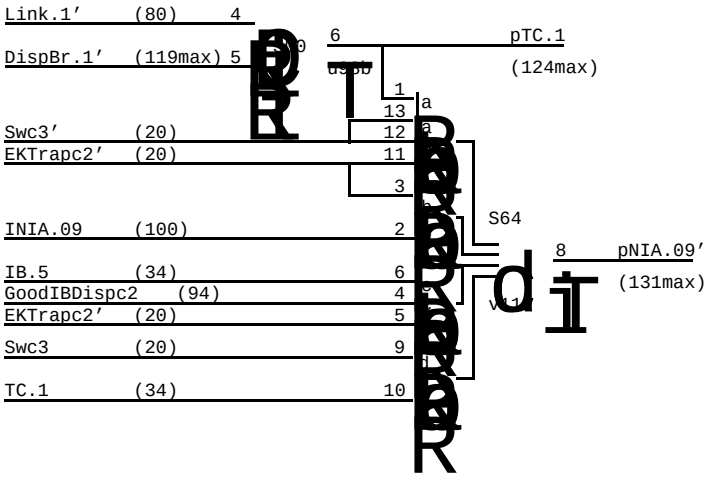
94	^ to RefillIntc2	100	^ to INIA	20	^ to EKErrc2
24[3]	LS158 SB to pNIA′	12[2]	LS158 data to pNIA′	18[2]	LS158 E′ to pNIA′
5[1]	25S09/S374 setup	5[1]	25S09/S374 setup	5[1]	25S09/S374 setup
123[4]=127 nS		117[3]=120 nS		43[3]=46nS	

(See page 11 for pNIA[8-11] timing)

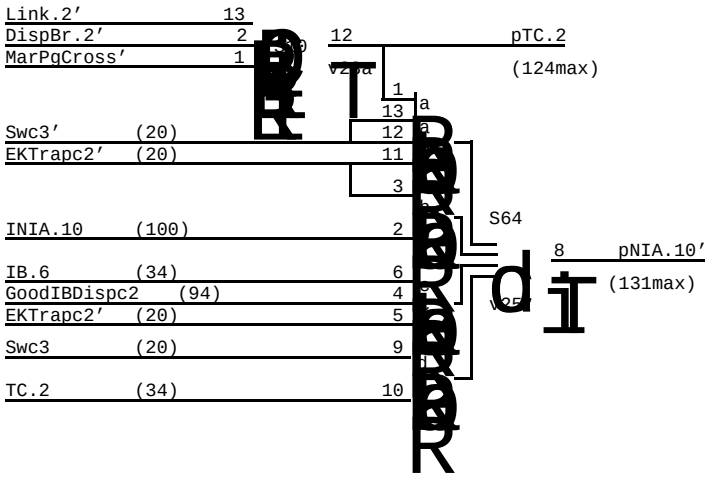
pNIA.8



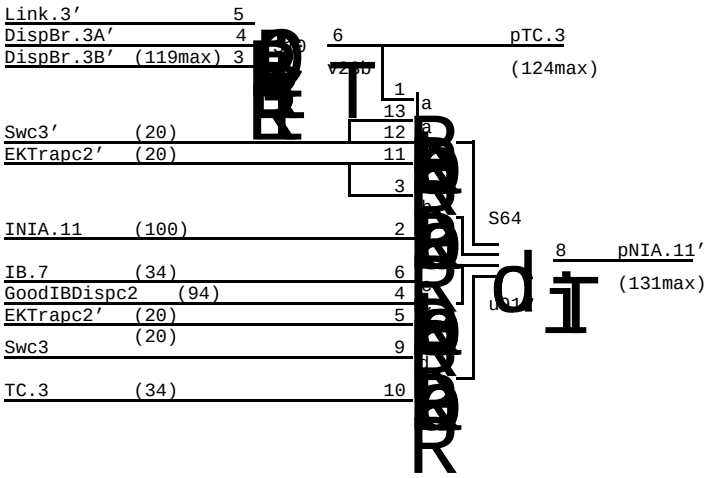
pNIA.9



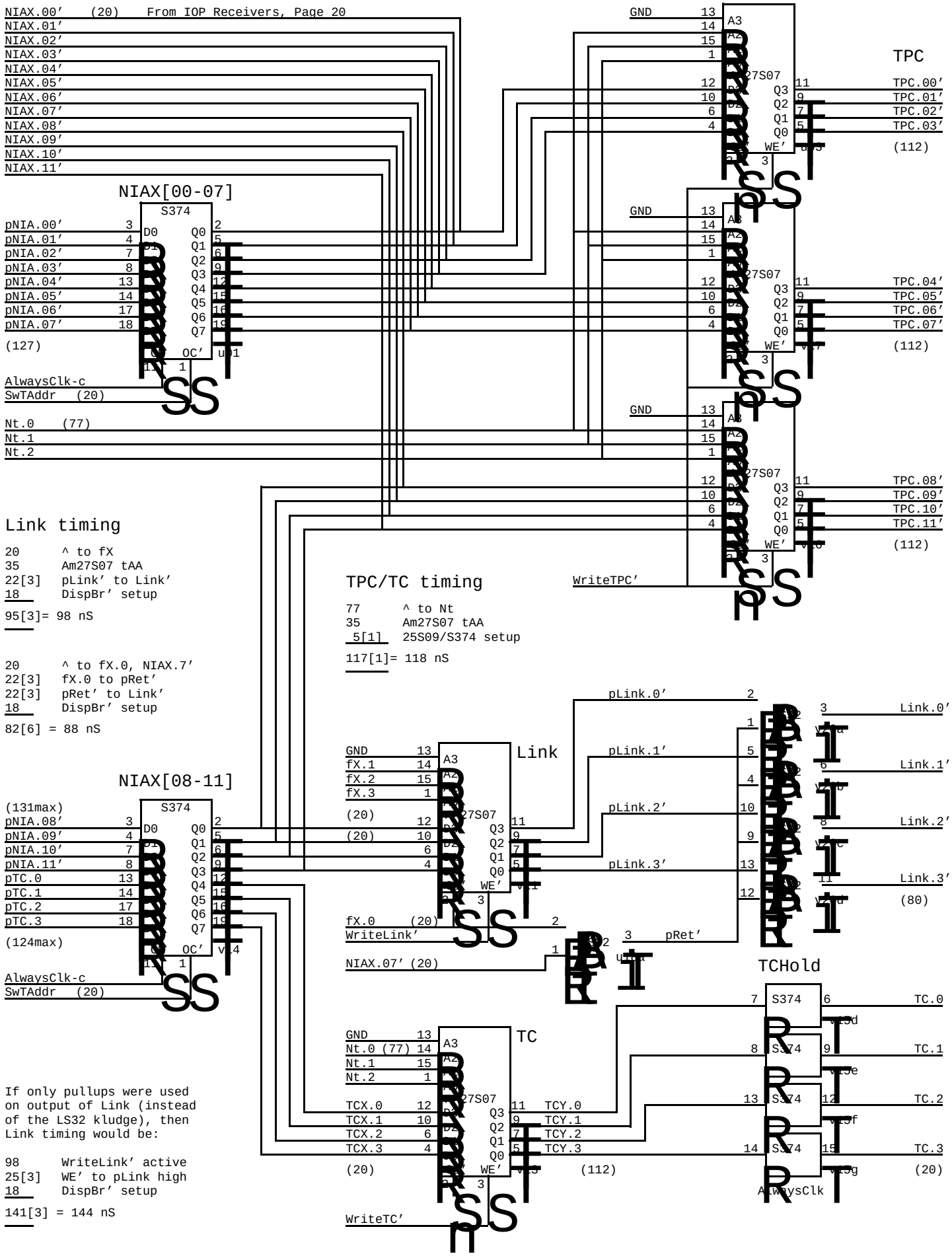
pNIA.10



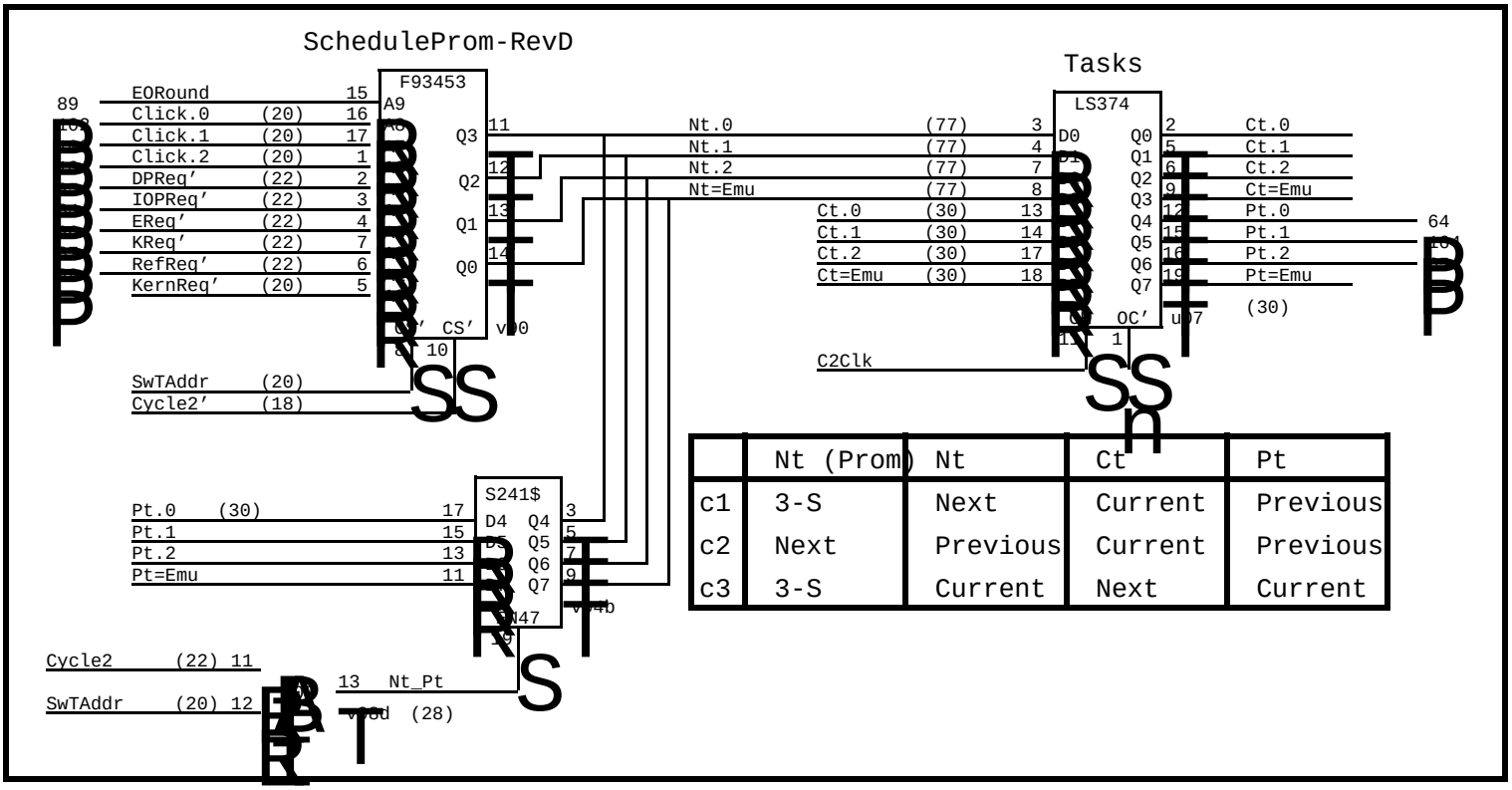
pNIA.11



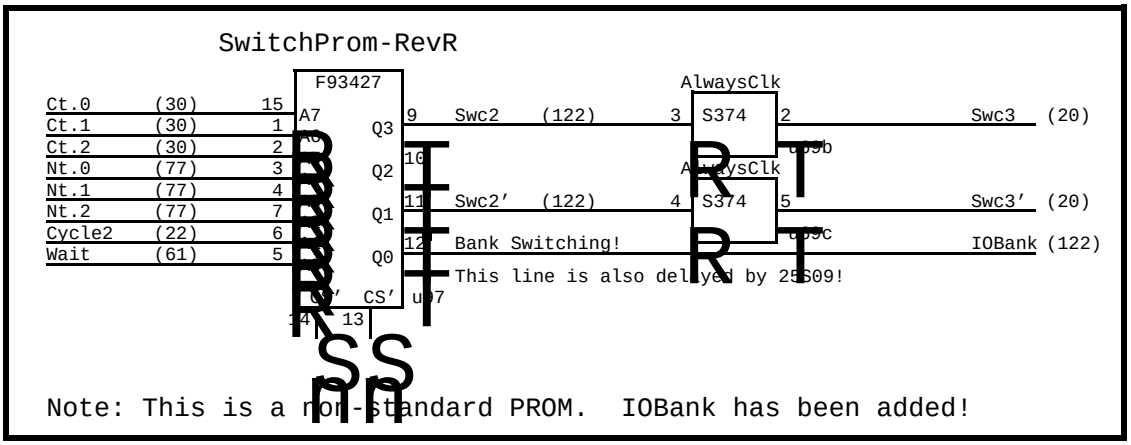
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	pNIA, pTC (Branching)	CPE13.sil	Bob Garner	Ba	5/30/83	14



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	TPC, TC, & Link	CPE14.sil	Bob Garner	Ba	5/30/83	15



	Nt (Prom)	Nt	Ct	Pt
c1	3-S	Next	Current	Previous
c2	Next	Previous	Current	Previous
c3	3-S	Current	Next	Current



Note: This is a non-standard PROM. IOBank has been added!

Task Numbers

0	Emulator
1	Display/LSEP
2	Ethernet
3	Refresh
4	Disk
5	IOP
6	Control Store R/W
7	Kernel

Swc2 timing=max(133,101,101)

22	^ to Kreq'	20	^ to SwTAddr	28	^ to Nt_Pt
55	F93453 addr to Nt	25	F93453 CS' to Nt	15[2]	S241 EN to Nt
45	F93427 addr to Swc2	45	F93427 addr to Swc2	45	F93427 addr to Swc2
10[1]	25S09 SB setup	10[1]	25S09 SB setup	10[1]	25S09 SB setup
132[1]=133 nS		100[1]=101 nS		98[3]=101 nS	

Click Assignment

0	Ethernet
1	Disk
2	IOP
3	Ethernet/Disk
4	Display/LSEP/Rfrsh

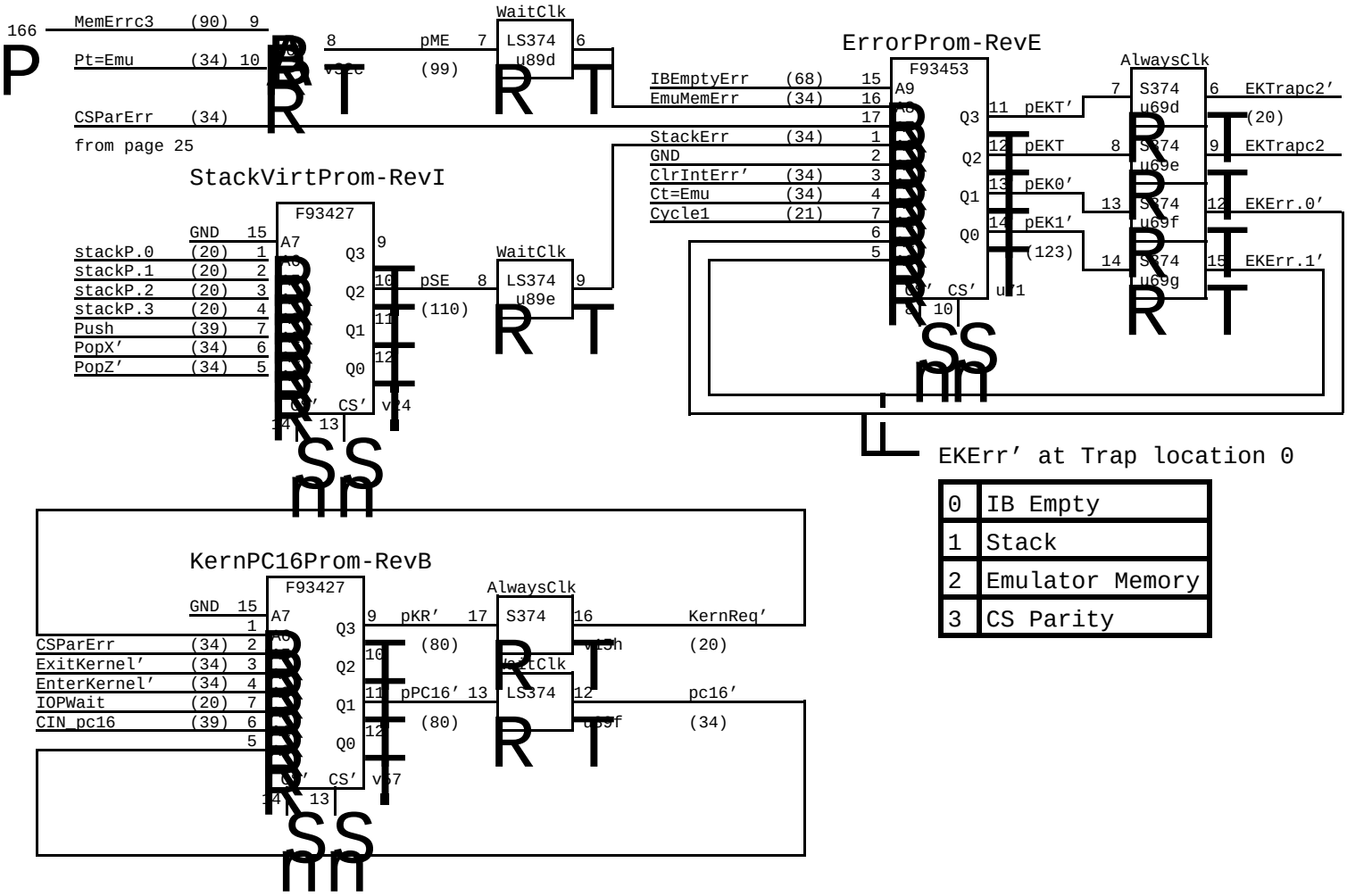
Notes:

When Disk = SA4000, Click 3 is Ethernet only.
When Disk = Trident, Click 3 is Ethernet on even rounds, Trident on Odd rounds (ie, 10-click rou

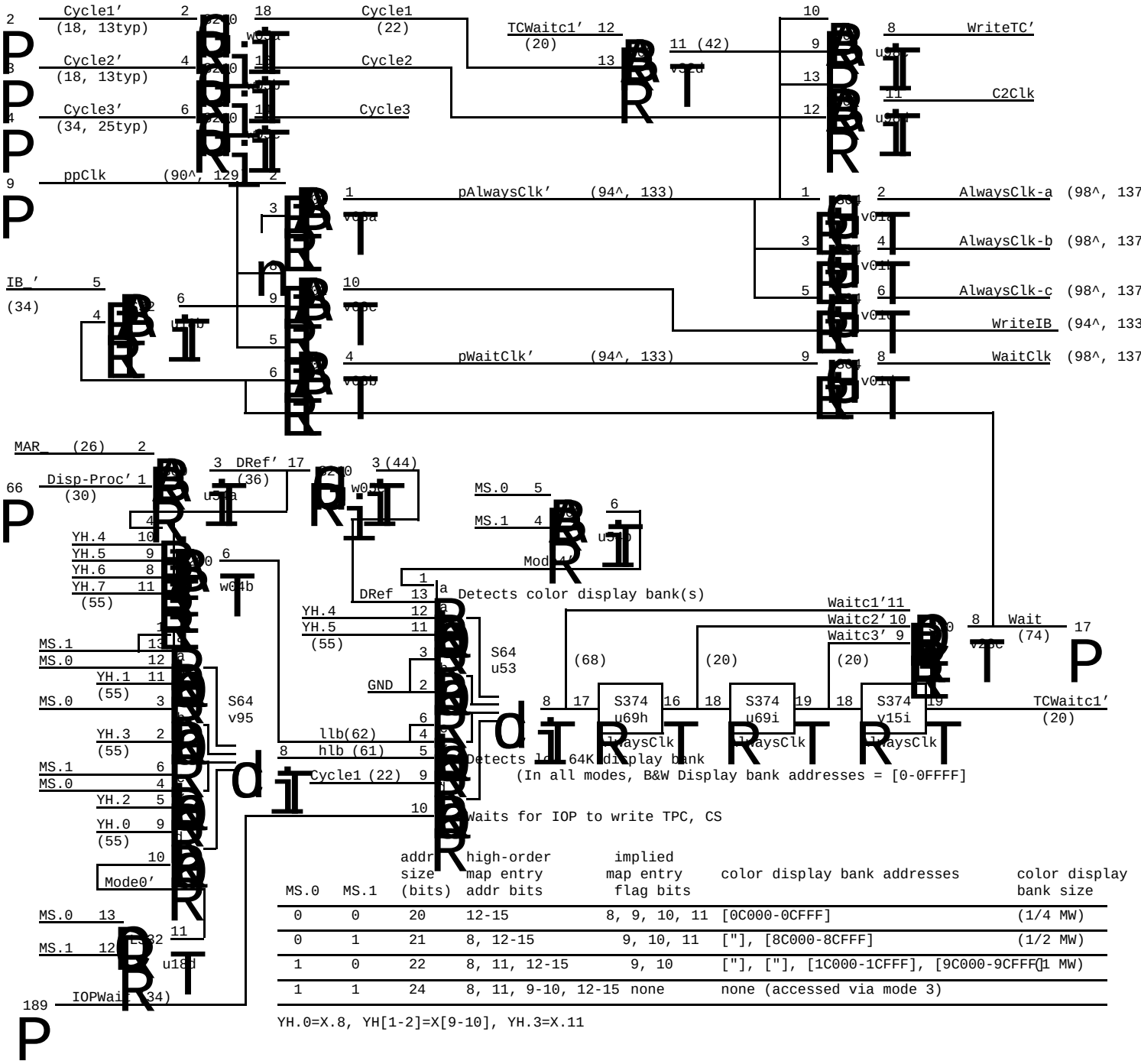
The Display & LSEP-refresh tasks never both use Click 4

Warning: This drawing contains font 4 macros!

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	Schedule, Switch, & Tasks	CPE15.sil	Bob Garner	Ba	5/30/83	16



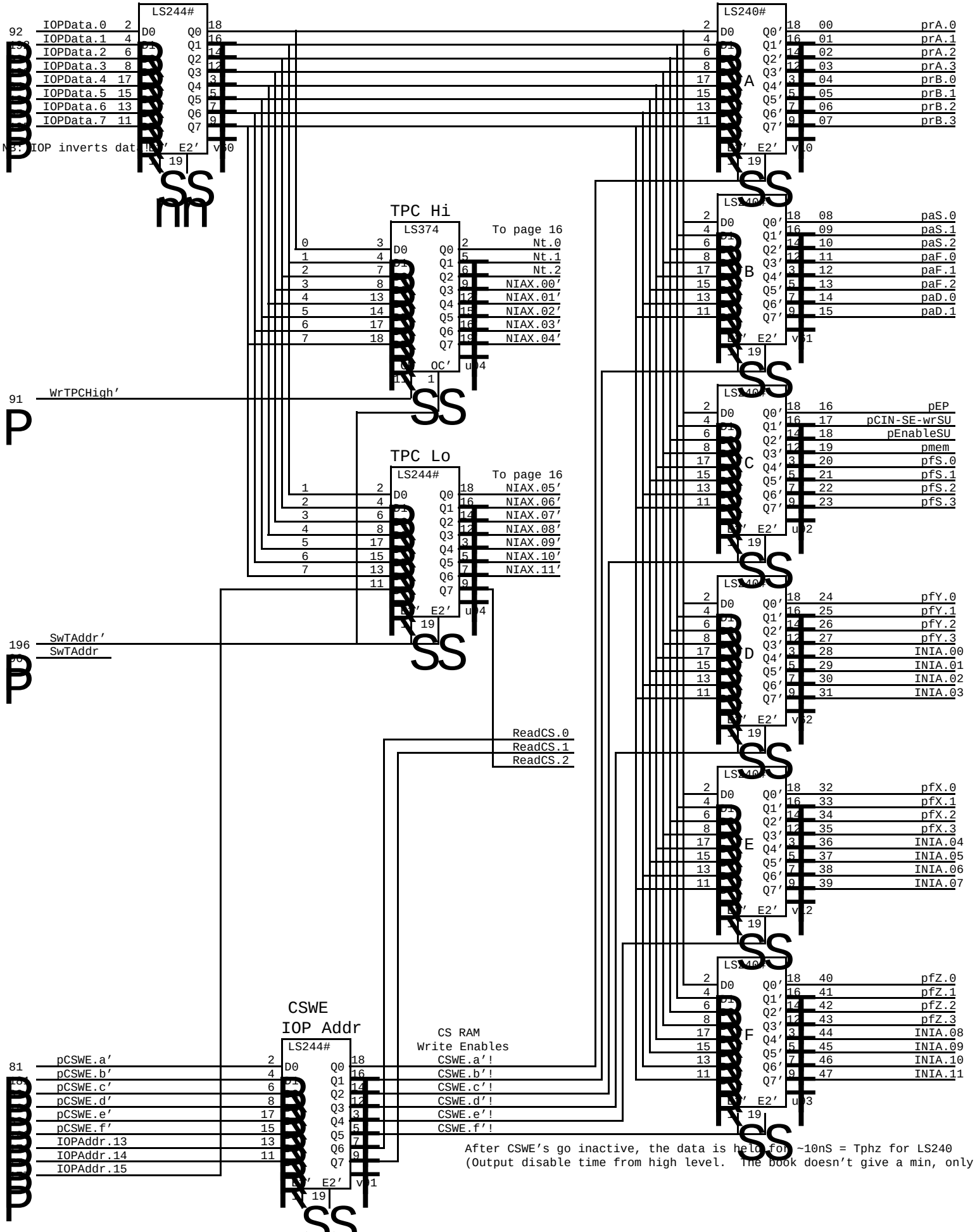
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	Error, Emulator, & Kernel Proms	CPE16.sil	Bob Garner	Ba	5/30/83	17



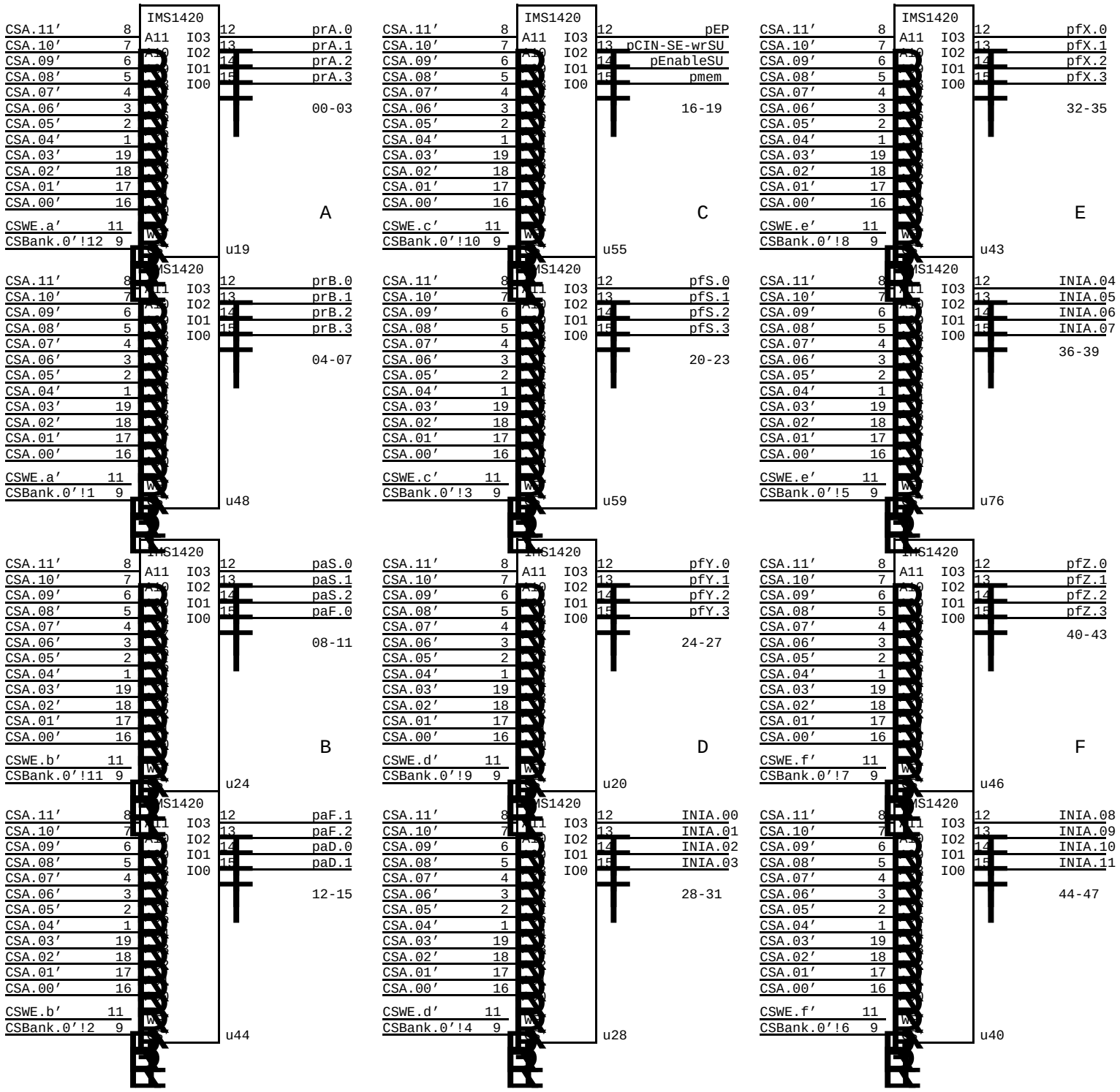
MS.0	MS.1	addr size (bits)	high-order map entry addr bits	implied map entry flag bits	color display bank addresses	color display bank size
0	0	20	12-15	8, 9, 10, 11	[0C000-0CFFF]	(1/4 MW)
0	1	21	8, 12-15	9, 10, 11	["], [8C000-8CFFF]	(1/2 MW)
1	0	22	8, 11, 12-15	9, 10	["], ["], [1C000-1CFFF], [9C000-9CFFF]	(1 MW)
1	1	24	8, 11, 9-10, 12-15	none	none (accessed via mode 3)	

YH.0=X.8, YH[1-2]=X[9-10], YH.3=X.11

XEROX PARC	Project	Drawing	File	Designers	Rev	Date	Page
	CPE	Clocks, Wait	CPE17.sil	Garner, Purcell	Ba	5/30/83	18



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	IOP Data In, CS Write	CPE18.sil	Tony West	Ba	5/30/83	19

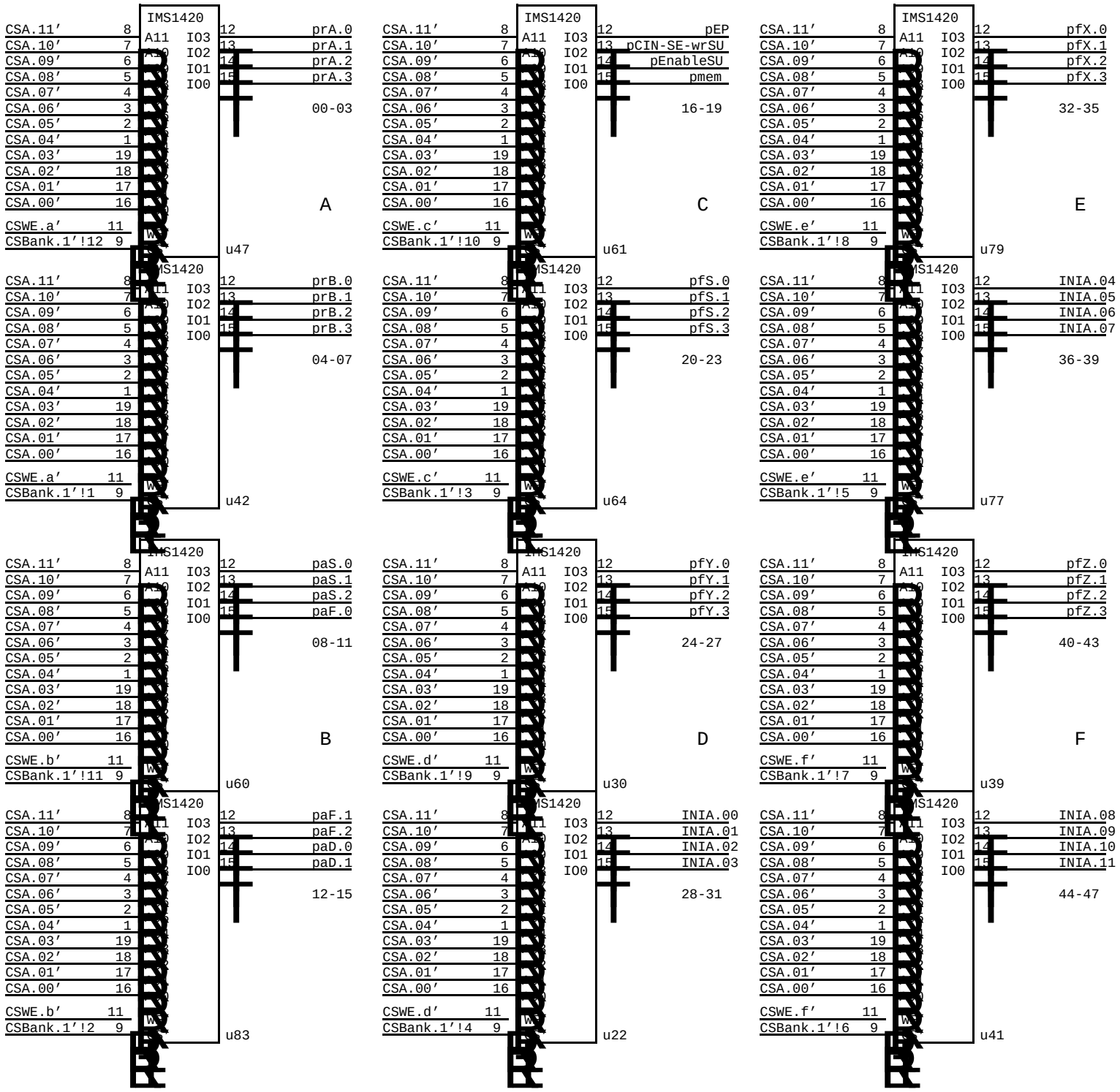


READ		WRITE - Data Hold	
Clock to CSA′ valid	17	tPLH for LS240	12
Transmission Delay	13	tPZ for LS244	10
tAA for IMS 1420-55	50		
CS Data valid at	80		22

This suggests that IMS 1420-70 would also work without any trouble.

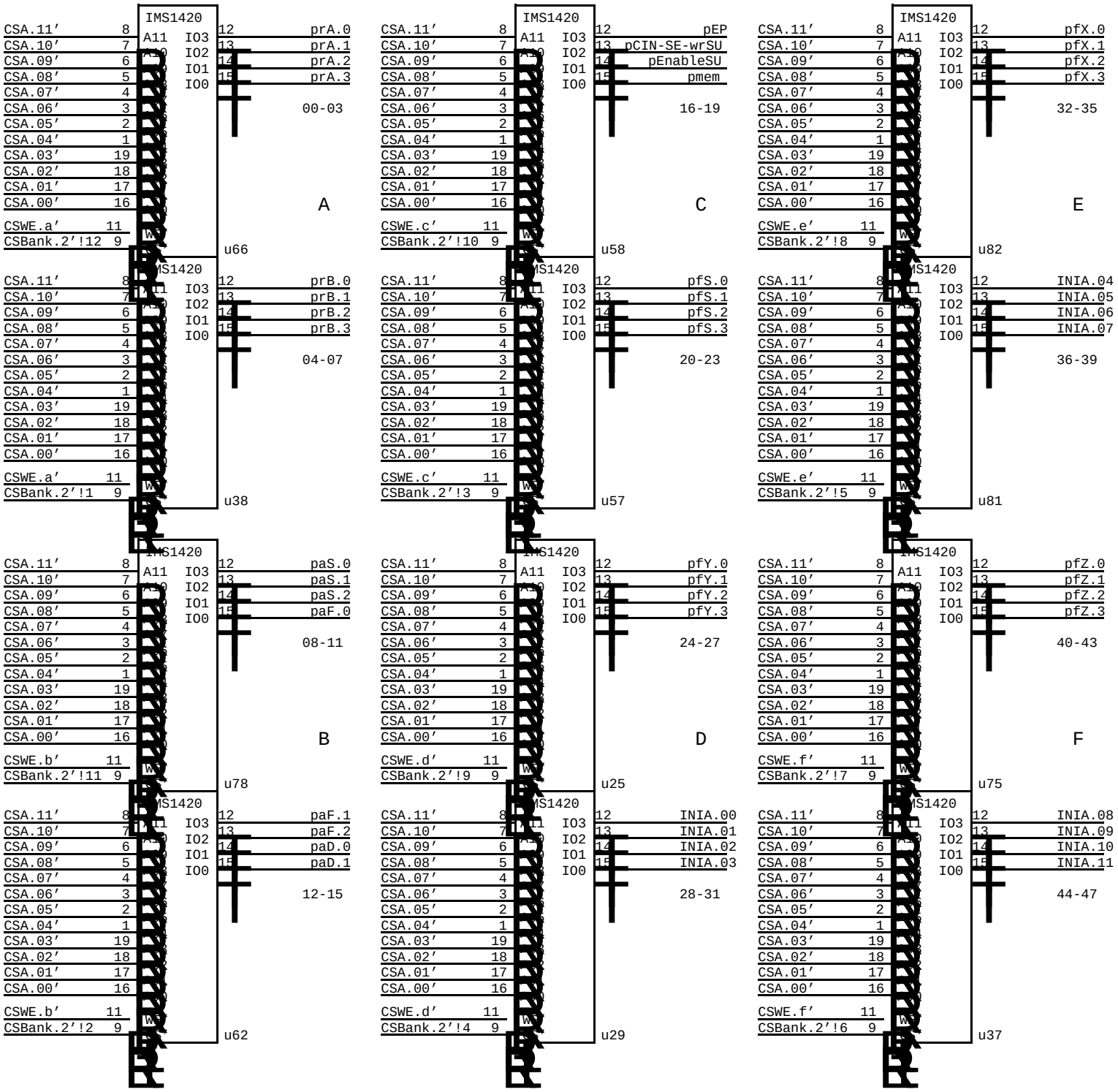
Warning: This drawing contains font 4 macros!

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	Control Store Bank 0: 0000-0FFF	CPE19.sil	Tony West	Ba	5/30/83	20



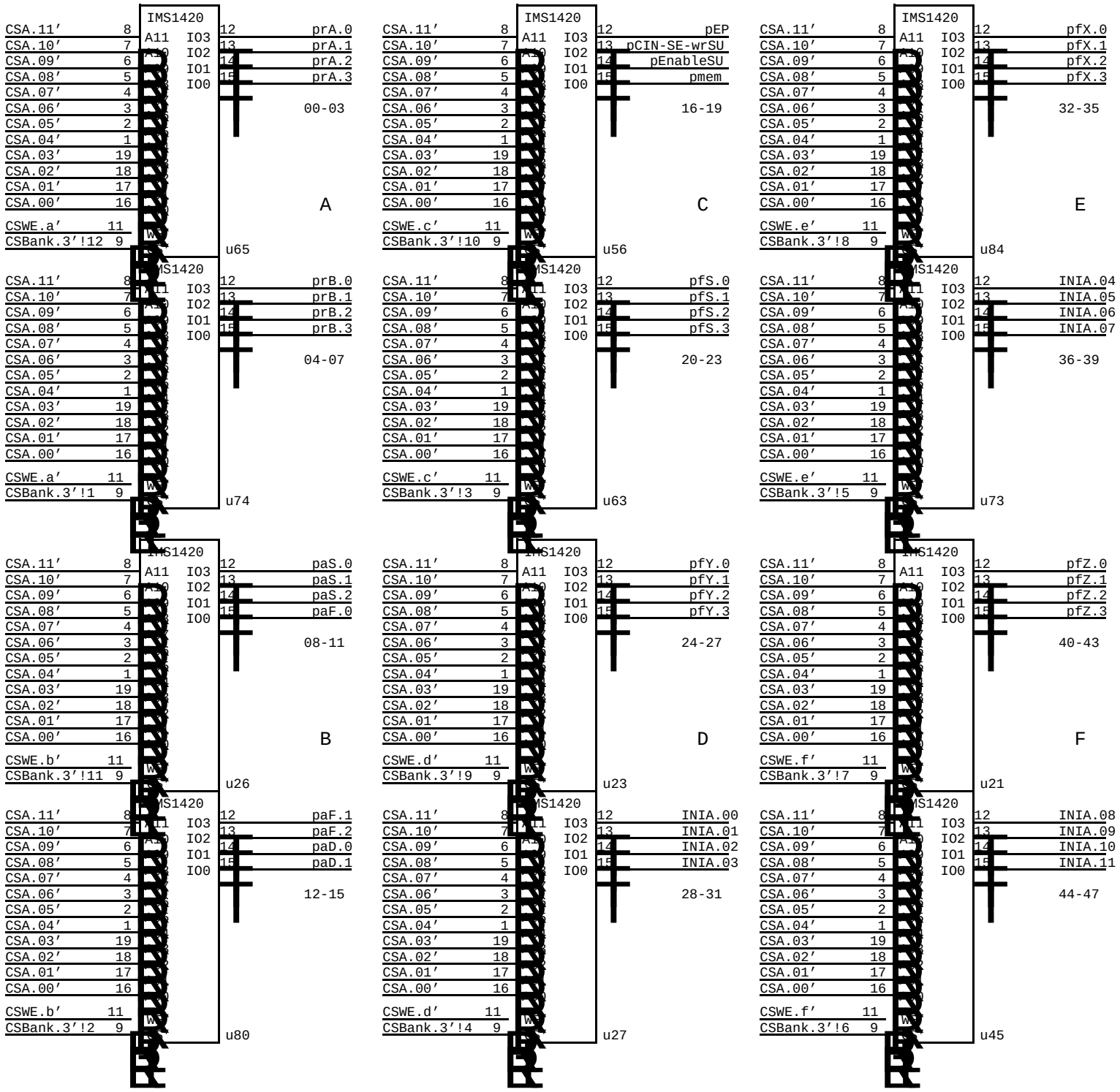
Warning: This drawing contains font 4 macros!

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	Control Store Bank 1: 1000-1FFF	CPE20.sil	Tony West	Ba	5/30/83	21



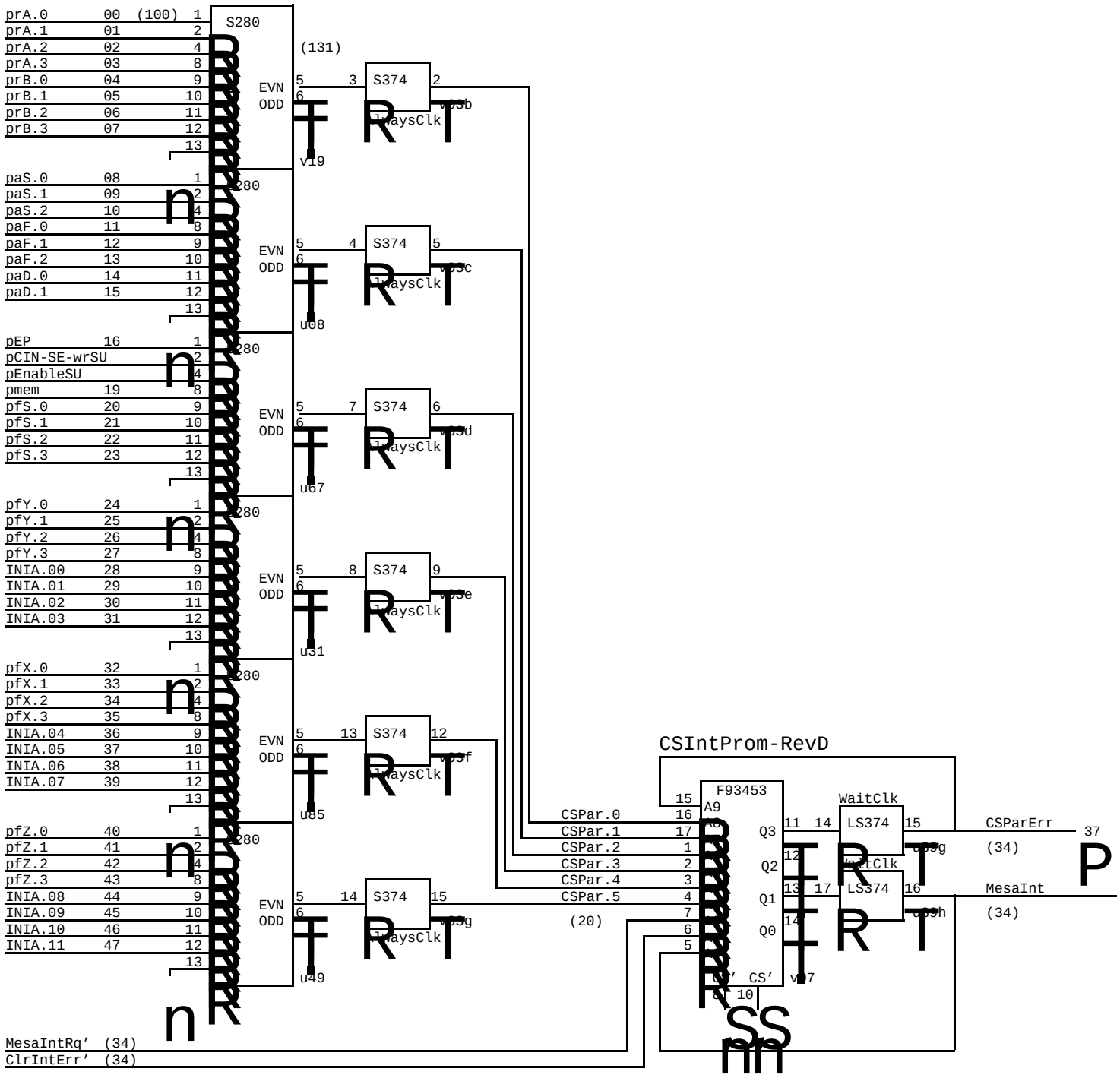
Warning: This drawing contains font 4 macros!

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	Control Store Bank 2: 2000-2FFF	CPE21.sil	Tony West	Ba	5/30/83	22



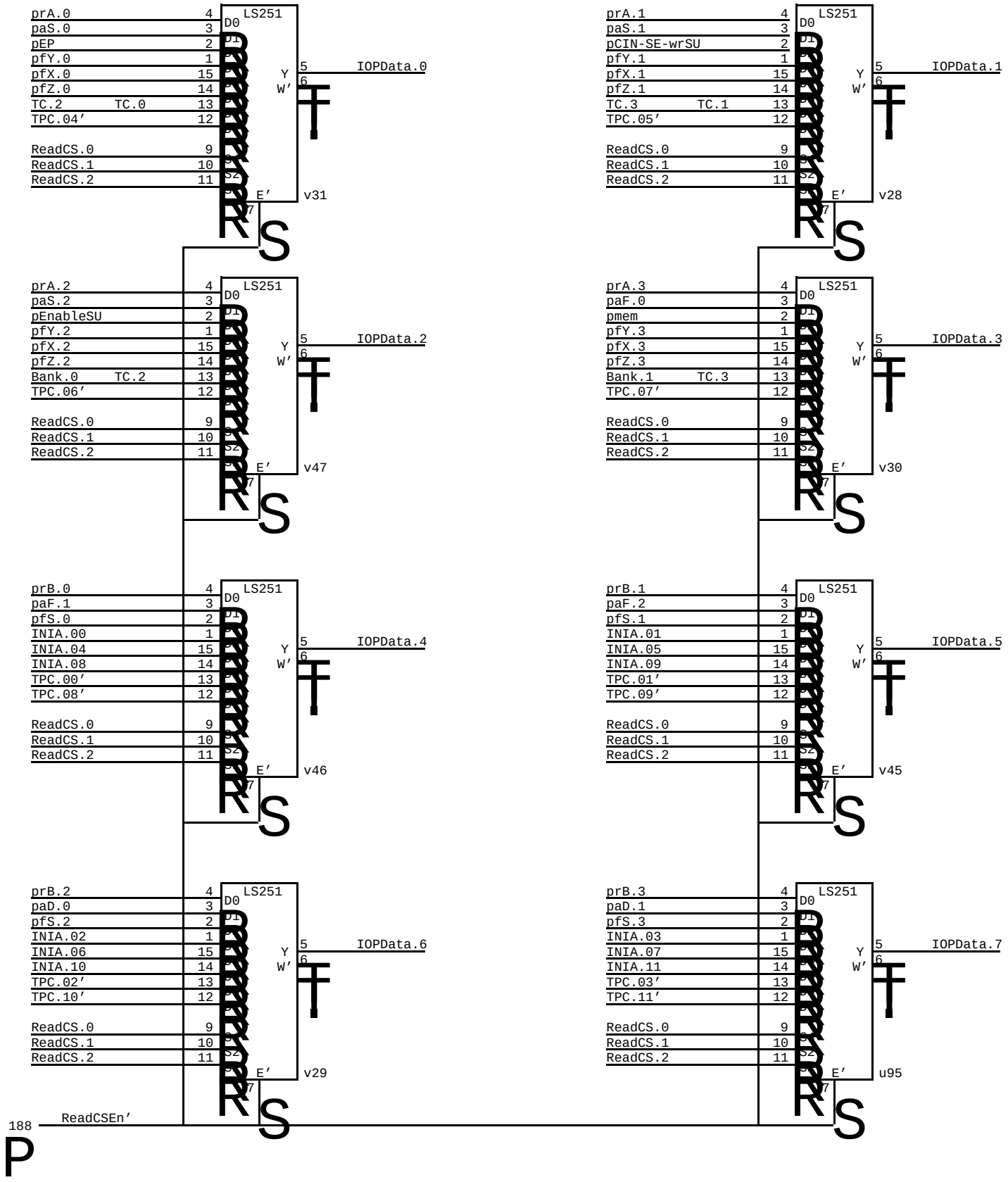
Warning: This drawing contains font 4 macros!

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	Control Store Bank 3: 3000-3FFF	CPE22.sil	Tony West	Ba	5/30/83	23

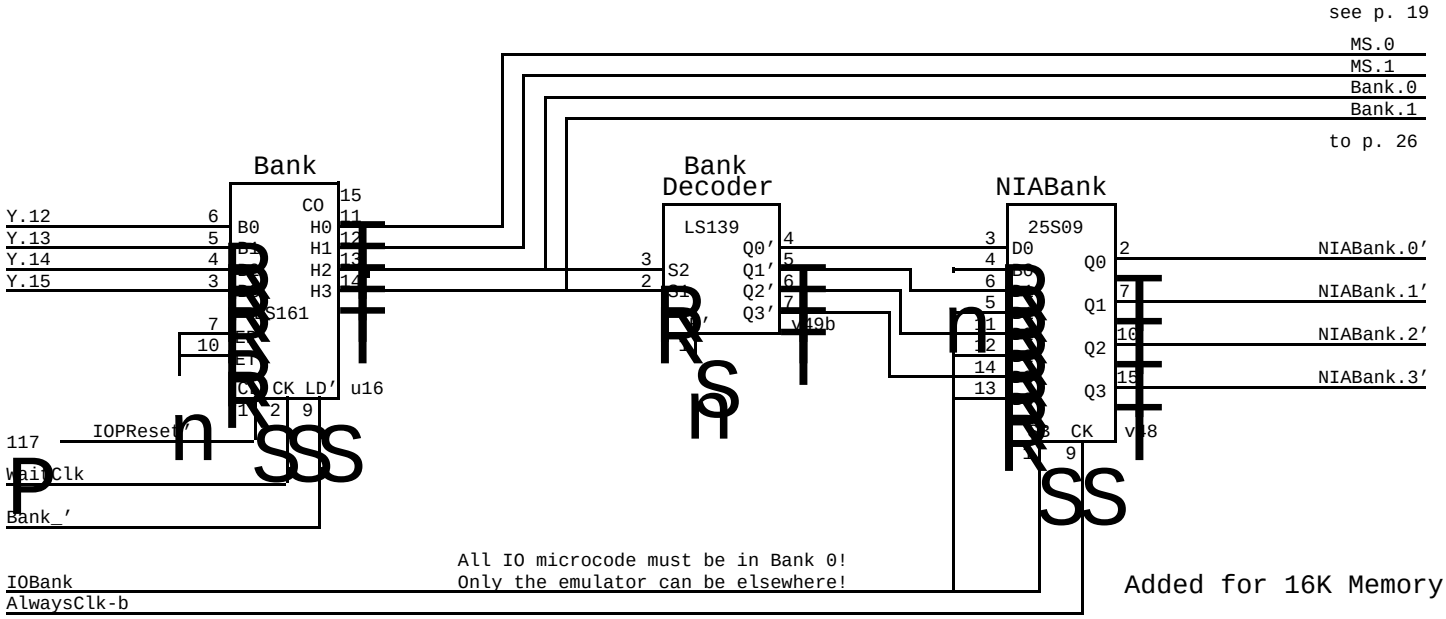


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	Control Store Parity Checker	CPE23.sil	Bob Garner	Ba	5/30/83	24

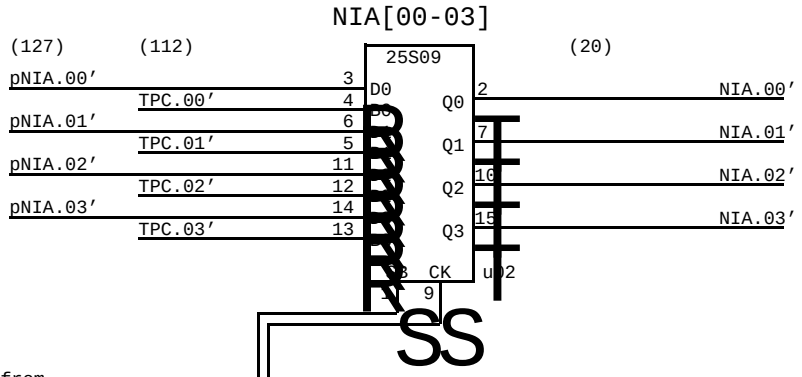
NB: TC[0-3] have been replaced by Bank[0-3].



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	IOP Data Out from CP	CPE24.sil	Bob Garner	Ba	5/30/83	25



This section is standard



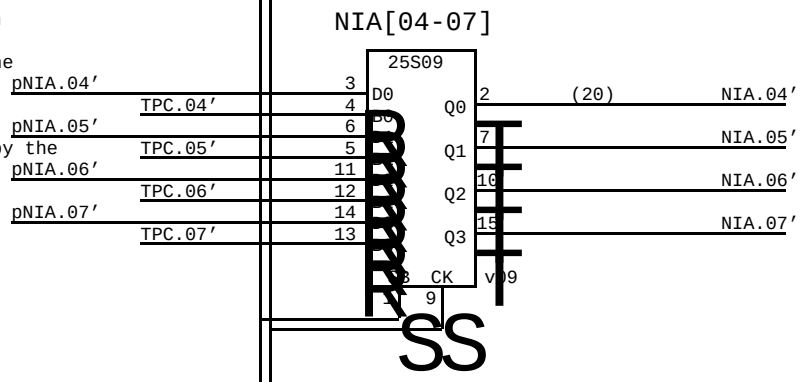
NOTE on Control Store Addresses

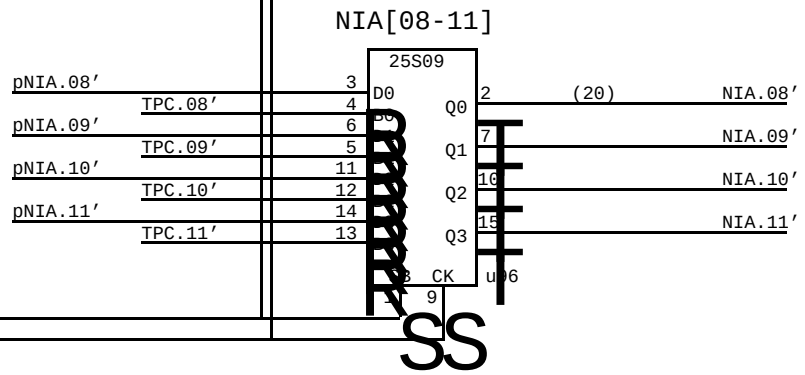
The next instruction address for the control store comes from one of two basic places:

1. TPC registers if switching tasks
2. From the INIA field of the previous microinstruction

In the case of (1), task 6's TPC registers are used by the IOP to provide the address when the IOP wants to read or write data into the control store.

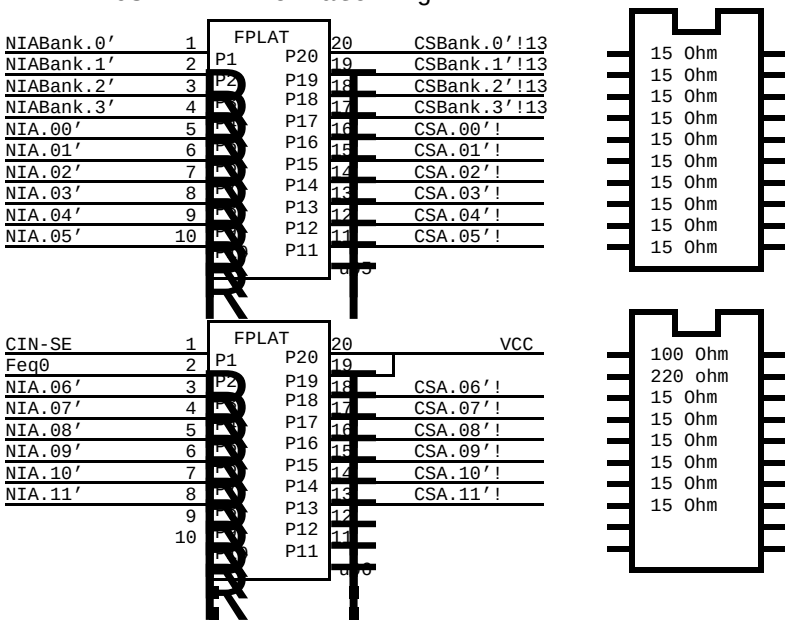
In the case of (2), the INIA field is suitably modified by the trap and conditional branch logic on page 16



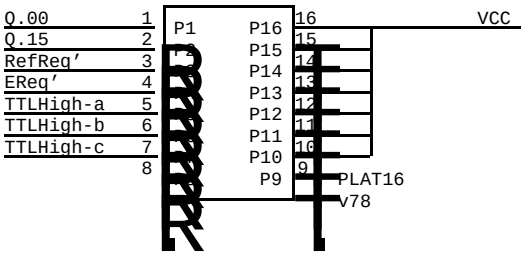


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	NIA, Bank Logic	CPE25.sil	Bob Garner	Ba	5/30/83	26

CS NIA Line Matching



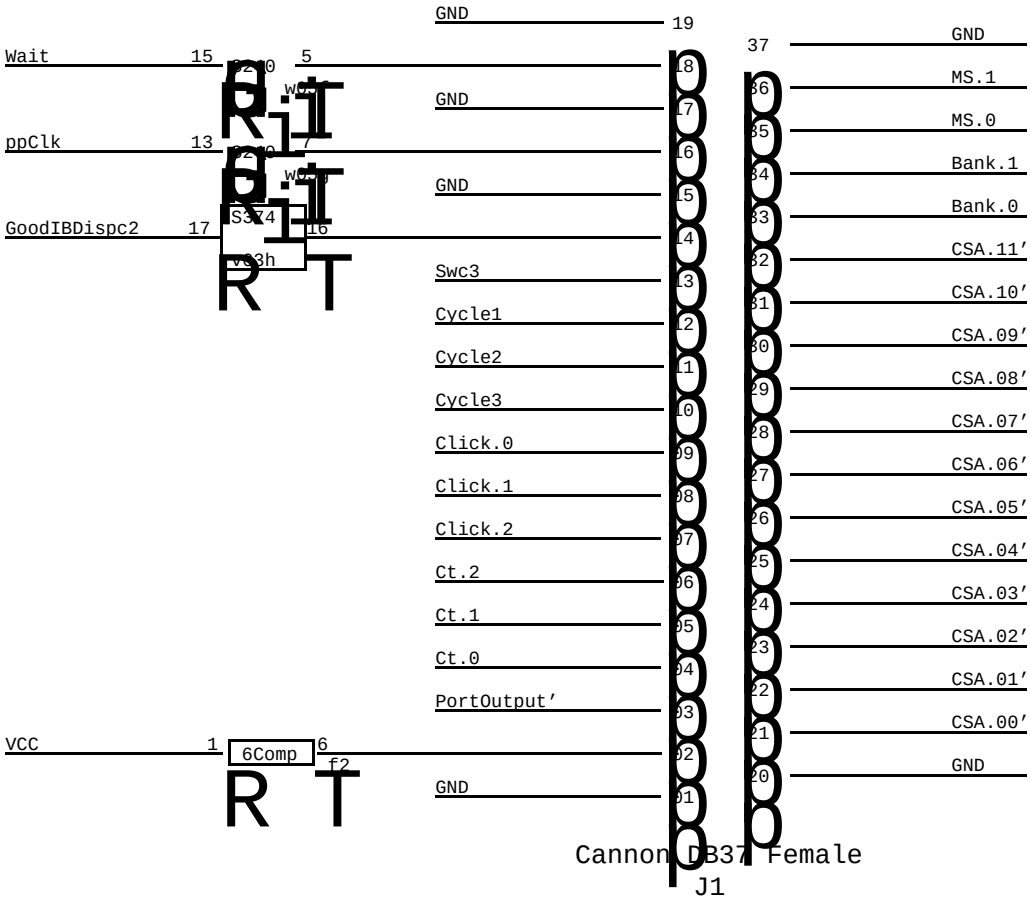
1 KOhm Pullups



Beckman Resnet DIP

898-1-1K

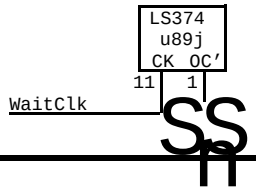
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	Resistors	CPE26.sil	Tony West	Ba	5/30/83	27



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	Debugger Box Connector	CPE27.sil	David Boggs	Ba	5/30/83	28

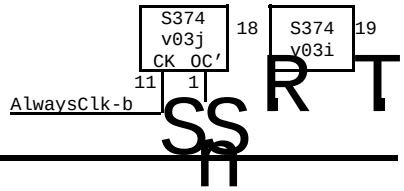
LS374 u89

b IBPtr.0
c IBPtr.1
d EmuMemErr
e StackErr
f pc16'
g CSParErr
h MesaInt
i SFLG'



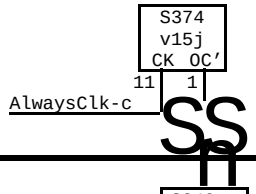
S374 v03

b CSPar.0
c CSPar.1
d CSPar.2
e CSPar.3
f CSPar.4
g CSPar.5
h GoodIBDispc3
i



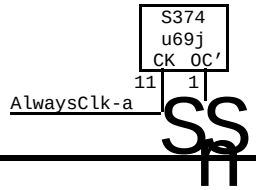
S374 v15

b MAR_'
c AllowMDR_
d TC.0
e TC.1
f TC.2
g TC.3
h KernReq'
i TCWaitc1'



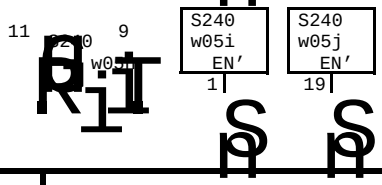
S374 u69

b Swc3
c Swc3'
d EKTrapc2'
e EKTrapc2
f EKErr.0'
g EKErr.1'
h Waitc2'
i Waitc3'



S240 w05

a Cycle1
b Cycle2
c Cycle3
d Cycle3'
e DRef
f WaitPin'
g Click.2Pin'



S04 v43

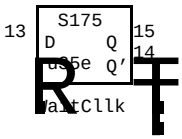
a aD.0'
b MAR_
c IBEmptyErr'
d Des_YBus
e XBus_SU
f Port_

S04 v39

a AlwaysClk-a
b AlwaysClk-b
c AlwaysClk-c
d WaitClk
e RH_
f Fne0

S175 u35

b MAS'
c MDS'
d SDS'
e
f *anon*



S00 v42

a XBus_SU'
b pMAR_'
c MarPgCross'
d CIN_pc16

S00 v85

a Pop
b Nibble'
c Byte'
d Xhigh_0

S00 u36

a *anon*
b WPort
c *anon*
d DesClkDisable

S00 v93

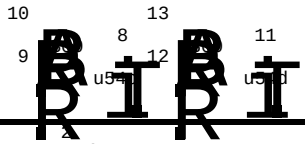
a WriteSU'
b WriteLink'
c WriteRH'
d WrIBFront

S00 u33

a pTC.0
b pTC.1
c WriteTC'
d C2Clk

S00 u54

a DRef'
b Mode4'
c
d



S02 v08

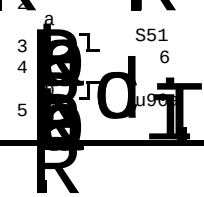
a pAlwaysCLK'
b pWaitCLK'
c WriteIB
d Nt_Pt

S08 v32

a paSh.0
b pAllowMDR_
c pME
d *anon*

S51 u90

a
b WrTPC



S10 v79

a sh
b Push
c XByte'

S10 v23

a pTC.2
b pTC.3
c Wait

S20

a XBus_IB'
b EnLRotn'

LS32 v98

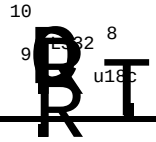
a DispBr'
b EnDispBr.3A'
c EnDispBr2-3B'
d EnDispBr0-1'

LS32 v20

a Link.0'
b Link.1'
c Link.2'
d Link.3'

LS32 u18

a pRet'
b *anon*
c
d M01



S38 v58

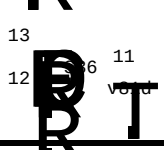
a Q.00
b Q.15
c CarryIn
d CarryIn

S51 u90

a Waitc1'
b WriteTPC'

S86 v81

a PageCross
b MapRef
c Refresh
d

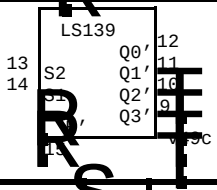


S260 w04

a IBEmptyErr
b *anon*

LS139 v49

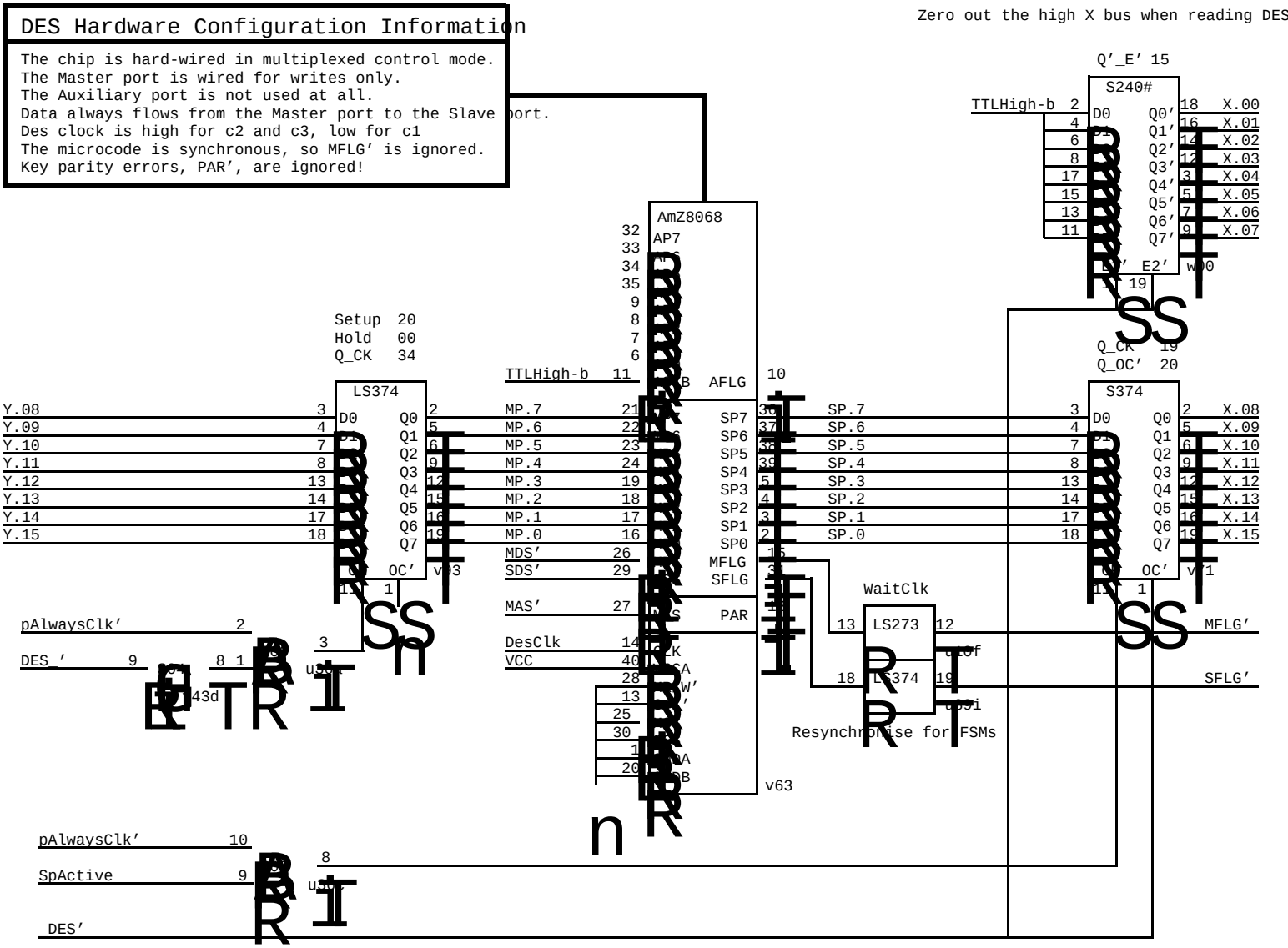
a
b bank decode



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	Part Allocation & Spares	CPE28.sil	Tony West	Ba	5/30/83	29

DES Hardware Configuration Information

The chip is hard-wired in multiplexed control mode.
The Master port is wired for writes only.
The Auxiliary port is not used at all.
Data always flows from the Master port to the Slave port.
Des clock is high for c2 and c3, low for c1
The microcode is synchronous, so MFLG' is ignored.
Key parity errors, PAR', are ignored!



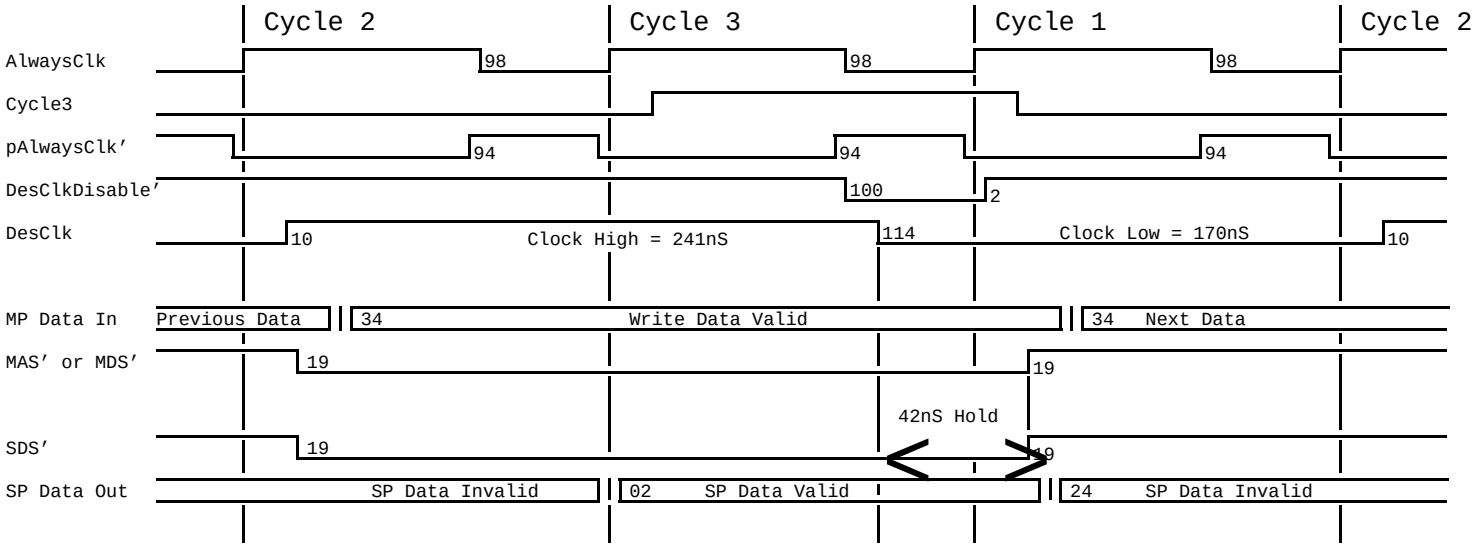
Warning: This drawing contains font 4 macros!

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	DES Encryption Hardware	CPE29.sil	Tony West	Ba	5/30/83	30

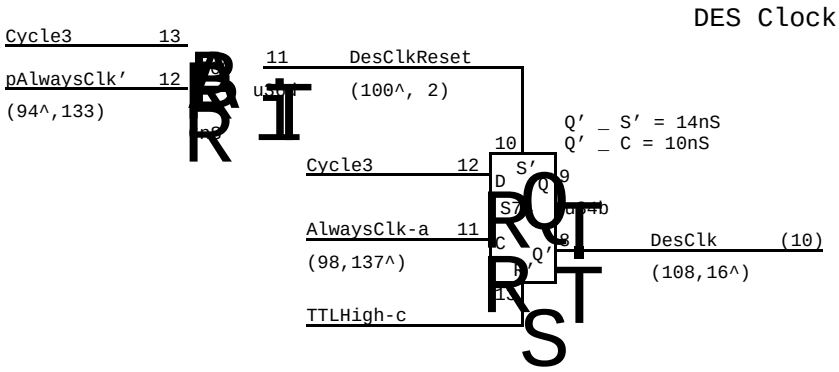
Clock & Reset		AMD #	min.	max.	actual used	Notes
Clock width HIGH		1	115		241	
Clock width LOW		2	115		170	
Clock Cycle		3	250		411	
Clock High to MAS'&MDS' High	Reset Hold	6	0	50	19	
MP and SP Strobe Times						
MAS' falling to MAS' rising (address)	MAS width Low	32	80		274	
MDS' falling to MDS' rising (data)	MDS width Low	44a	125	1000	274	Can't exceed 1000, so have to watch out for WaitC
MDS' rising to MDS' falling	MDS Recovery	46	125		137	
SDS' falling to SDS' rising (data read)	SDS width Low	44a	125	1000	274	Can't exceed 1000, so have to watch out for WaitC
SDS' rising to SDS' falling	SDS Recovery	46	125		137	
Clk falling to MDS' rising	MDS Hold	45	20	70	42	This is the difficult bit! See circuitry below
Clk falling to SDS' rising	SDS Hold	46	20	70	42	This is the difficult bit! See circuitry below
MAS Write into Master Port						
Data Valid to MAS' rising	Address Setup	36	55		268	
Data Hold after MAS' rising	Address Hold	37	60		243	
MDS Write into Master Port						
Data Valid to MDS' rising	Data Setup	47b	125		268	
Data Hold after MDS' rising	Data Hold	48	80		243	
SDS Read from Slave Port						
SDS falling to Data Valid	SP Access	49b		120		
SDS rising to Data Invalid	SP Data Hold	50	5			
SDS falling to SFLG rising	SP Flag	51		125		for last byte read

DES Clock Generator Timing

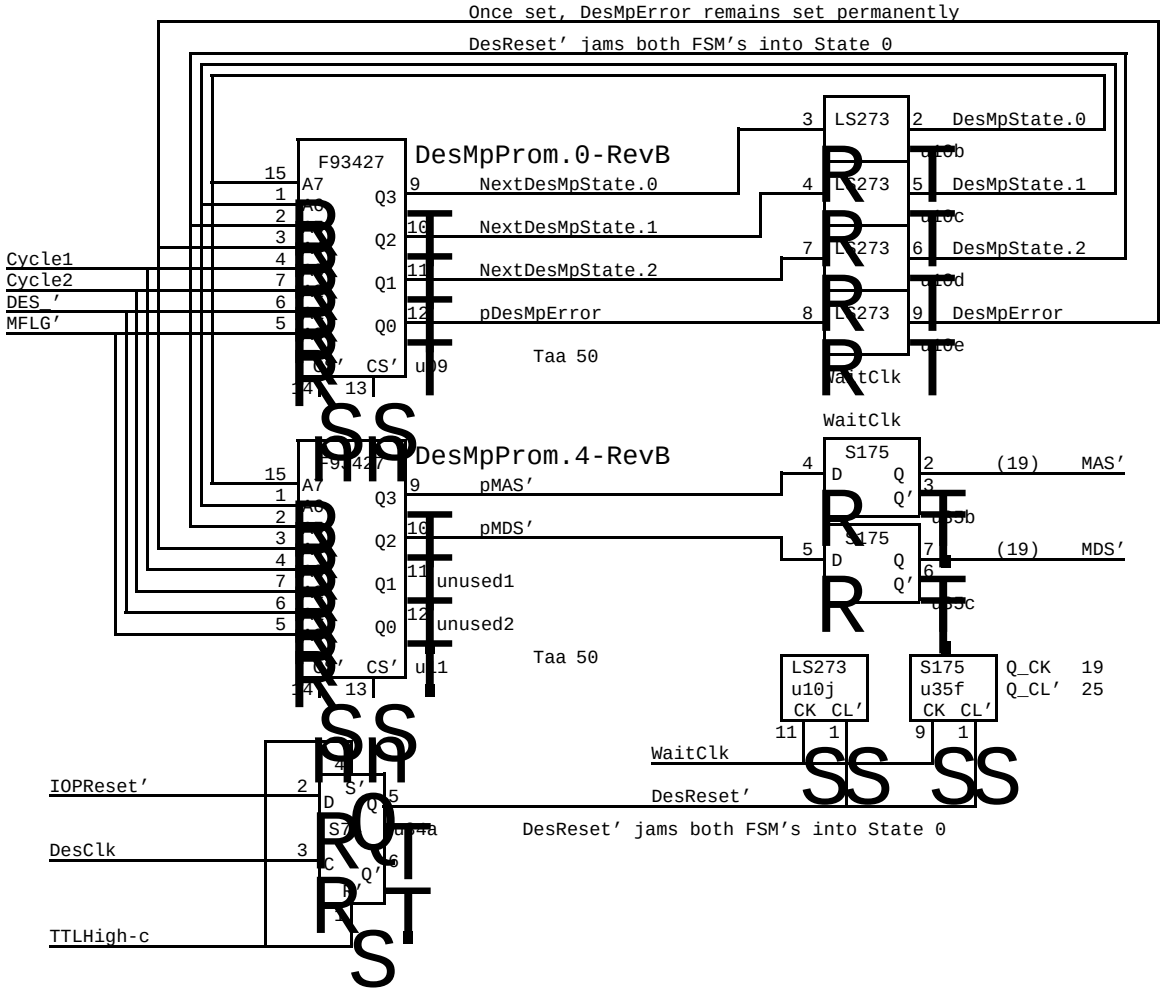
Note: Because of the requirement to hold MDS' and SDS' for 20 to 70 nanoseconds after DesClk falling, we bring DesClk down early in C
MAS', MDS' and SDS' follow at the end of Cycle 3.



DES Clock Generator

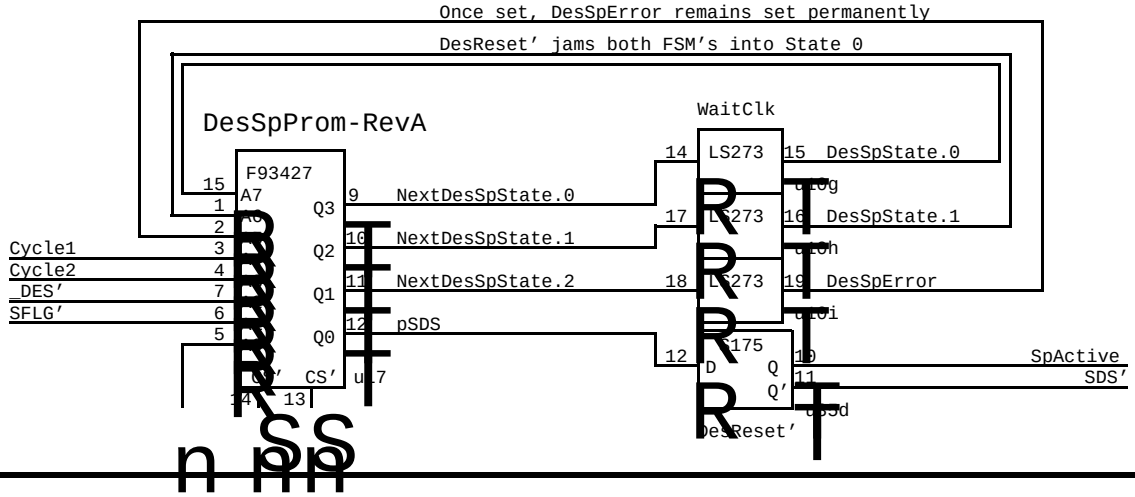


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	DES Timing & Clock Generator	CPE30.sil	Tony West	Ba	5/30/83	31

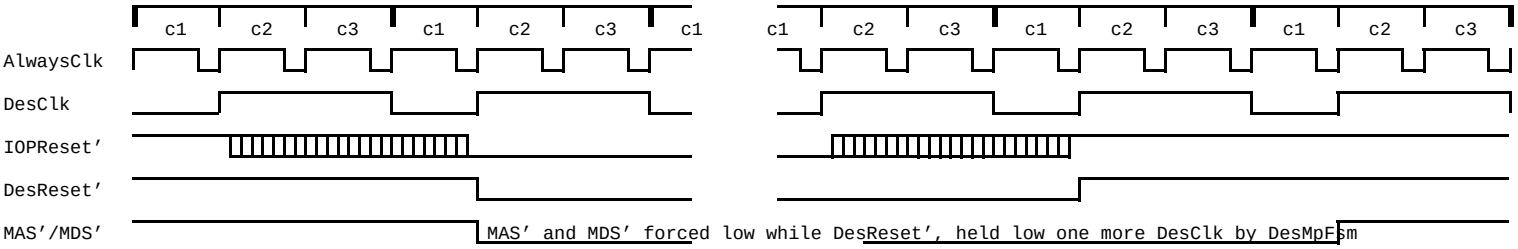


Des Master Port FSM

Des Slave Port FSM



Reset Des Chip and FSM's with IOPReset'

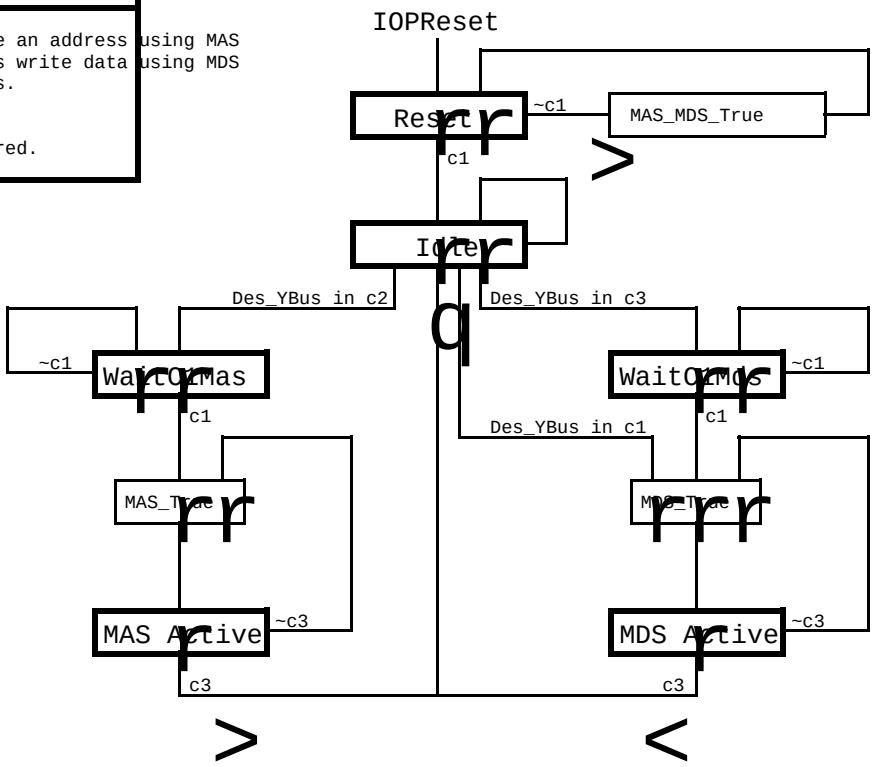


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	DES Finite-State Machines	CPE31.sil	Tony West	Ba	5/30/83	32

Note on semantics of Master Port Writes

If you write to the Des chip in c2, it means write an address using MAS
If you write to the Des chip in c1 or c3, it means write data using MDS
You may have to wait for c1 in some of these cases.

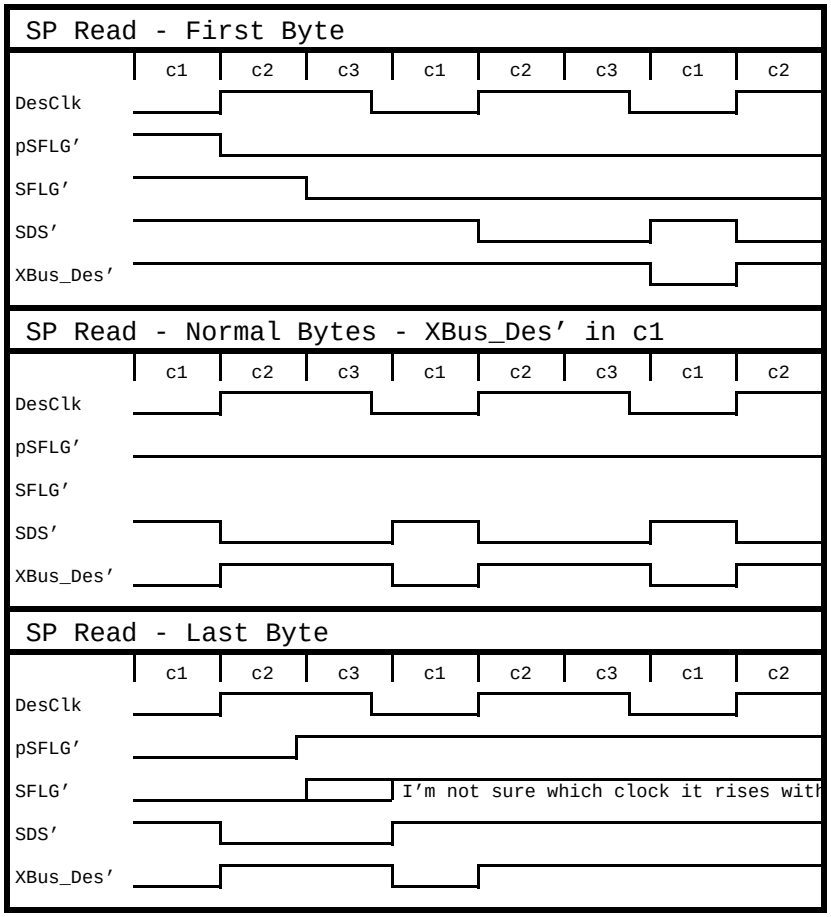
The signals are shown logical-true.
The implementation below inverts signals as required.

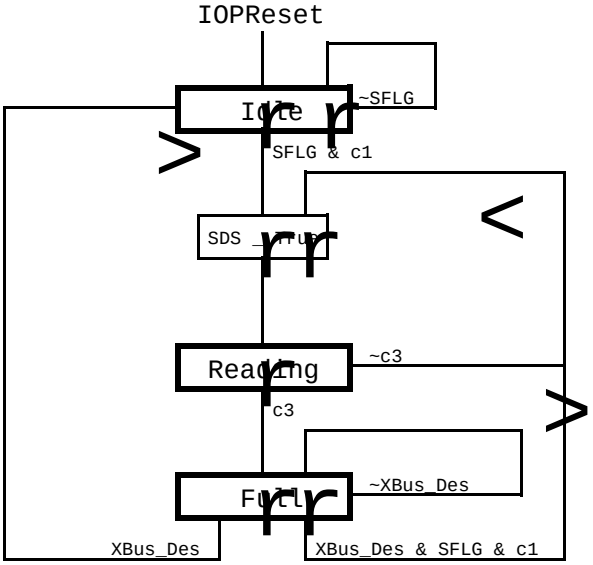


Master Port Finite-State Machine - Error handling of DesMpError signal is not shown

---

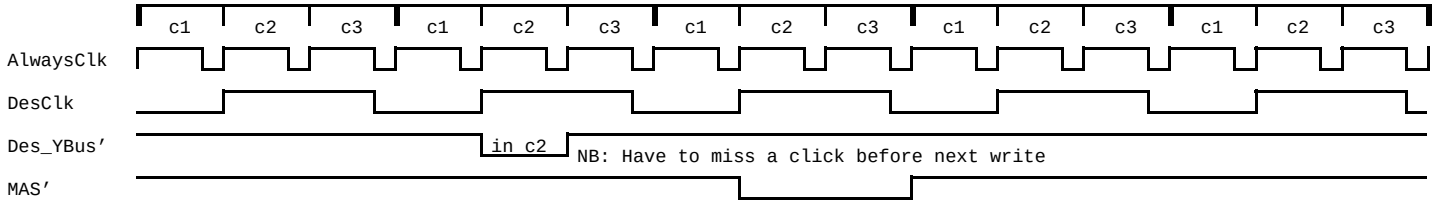
Slave Port Finite-State Machine - Error handling of DesSpError signal is not shown



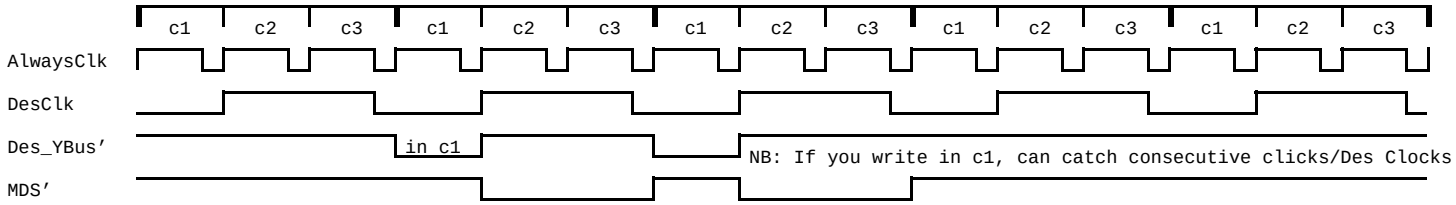


The signals are shown logical-true.
The implementation below inverts signals as required.

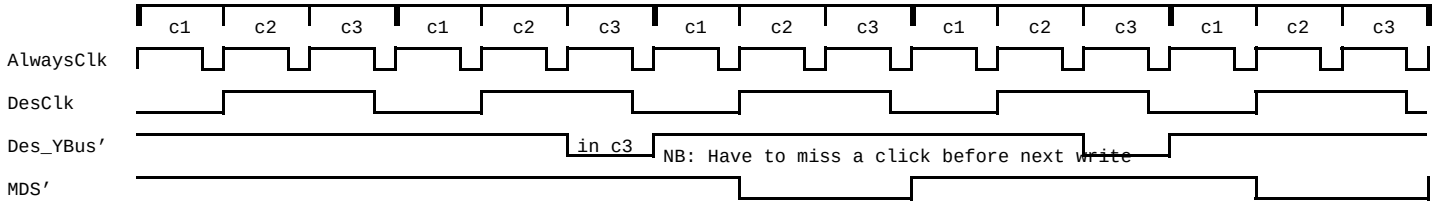
Write address into Des Master Port in C2



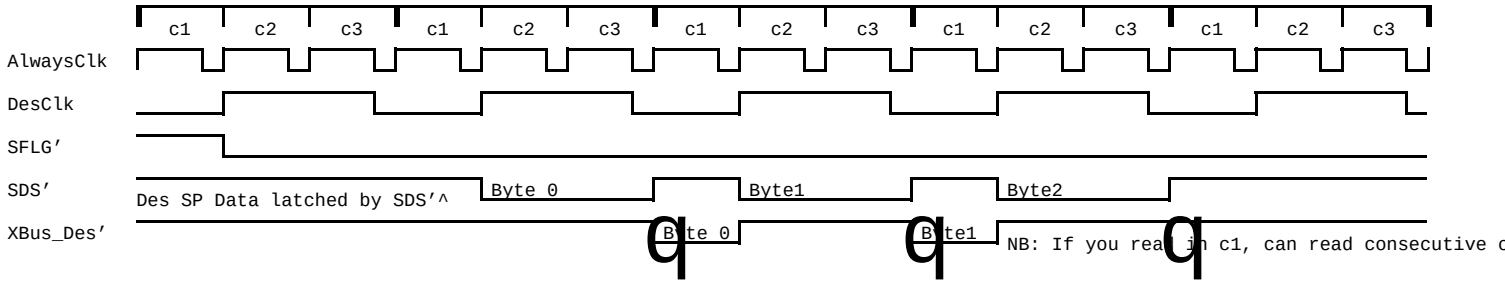
Write data into Des Master Port in C1



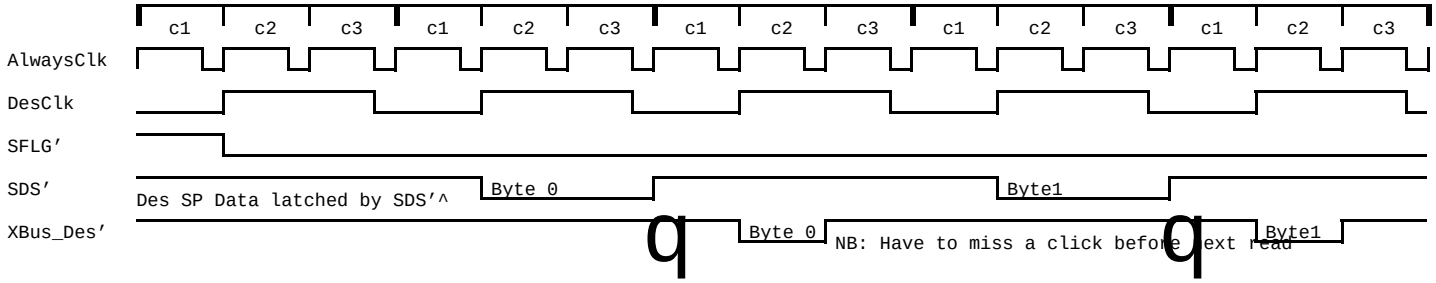
Write data into Des Master Port in C3



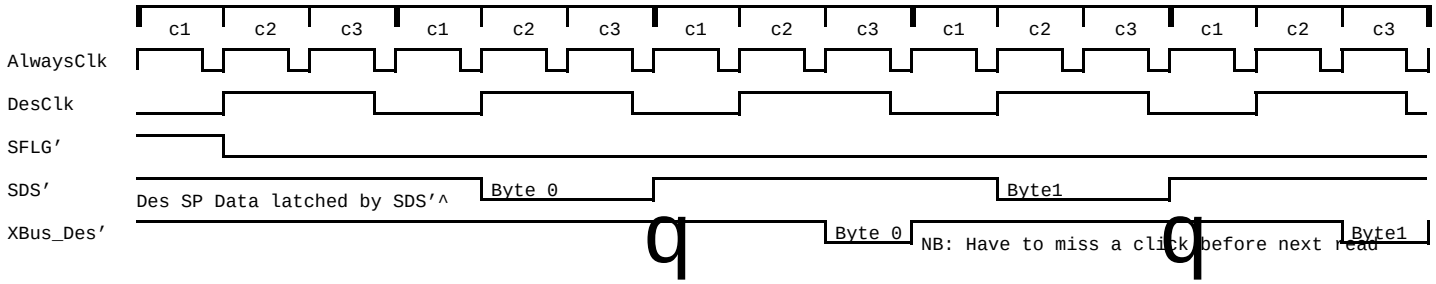
Read Data from Des Slave Port in C1



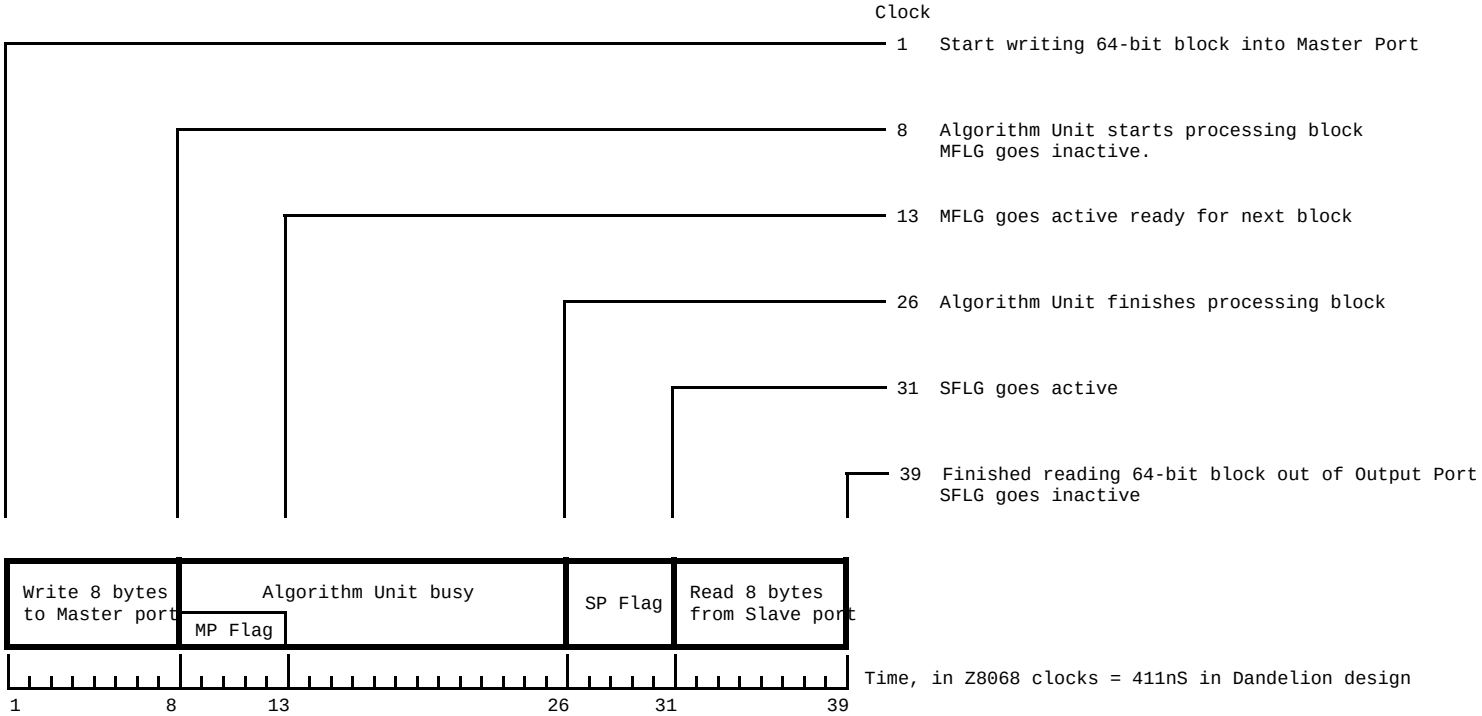
Read Data from Des Slave Port in C2



Read Data from Des Slave Port in C3



XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	CPE	DES Timing Diagrams	CPE33.sil	Tony West	Ba	5/30/83	34



WARNING! This data is not guaranteed to be correct!

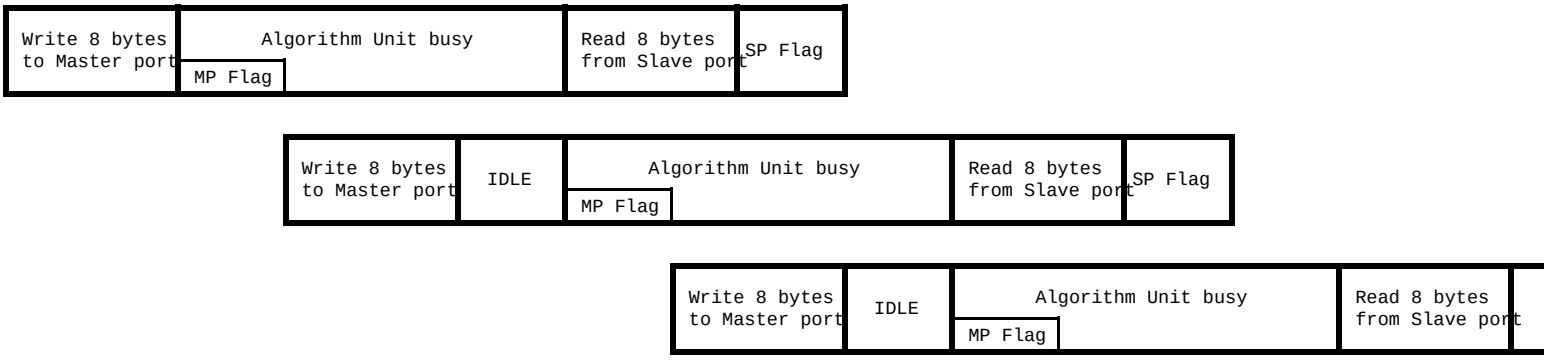
NOTES:

The longest operation in encrypting a block is the time it takes to get the data through the algorithm unit, 18 clocks. Therefore, this is the bottleneck in the pipelining scheme, and the software must aim to keep the Algorithm unit fully busy.

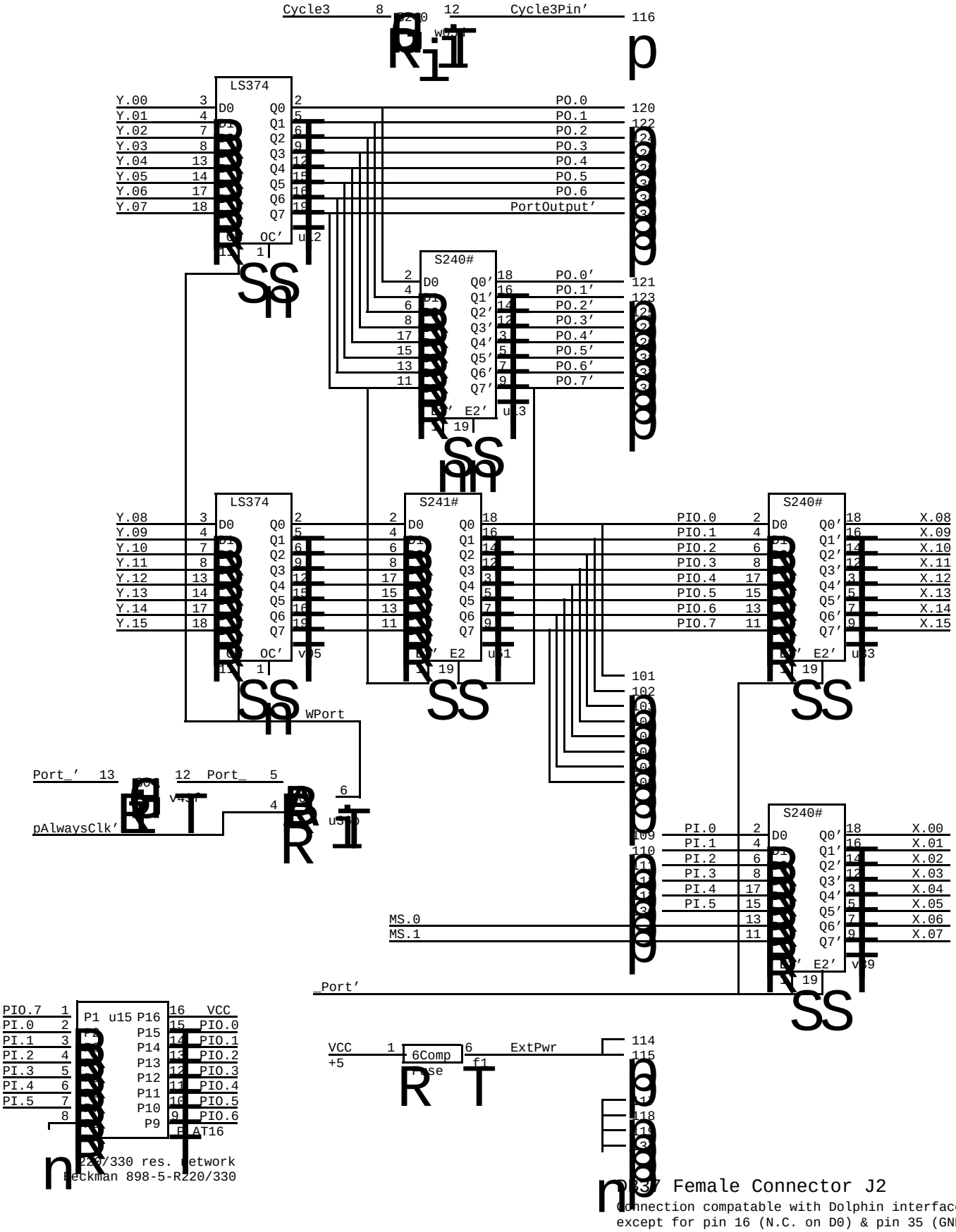
Apart from the first and last blocks, the time taken to encrypt the middle blocks is 18 clocks.

One possible pipelining scheme

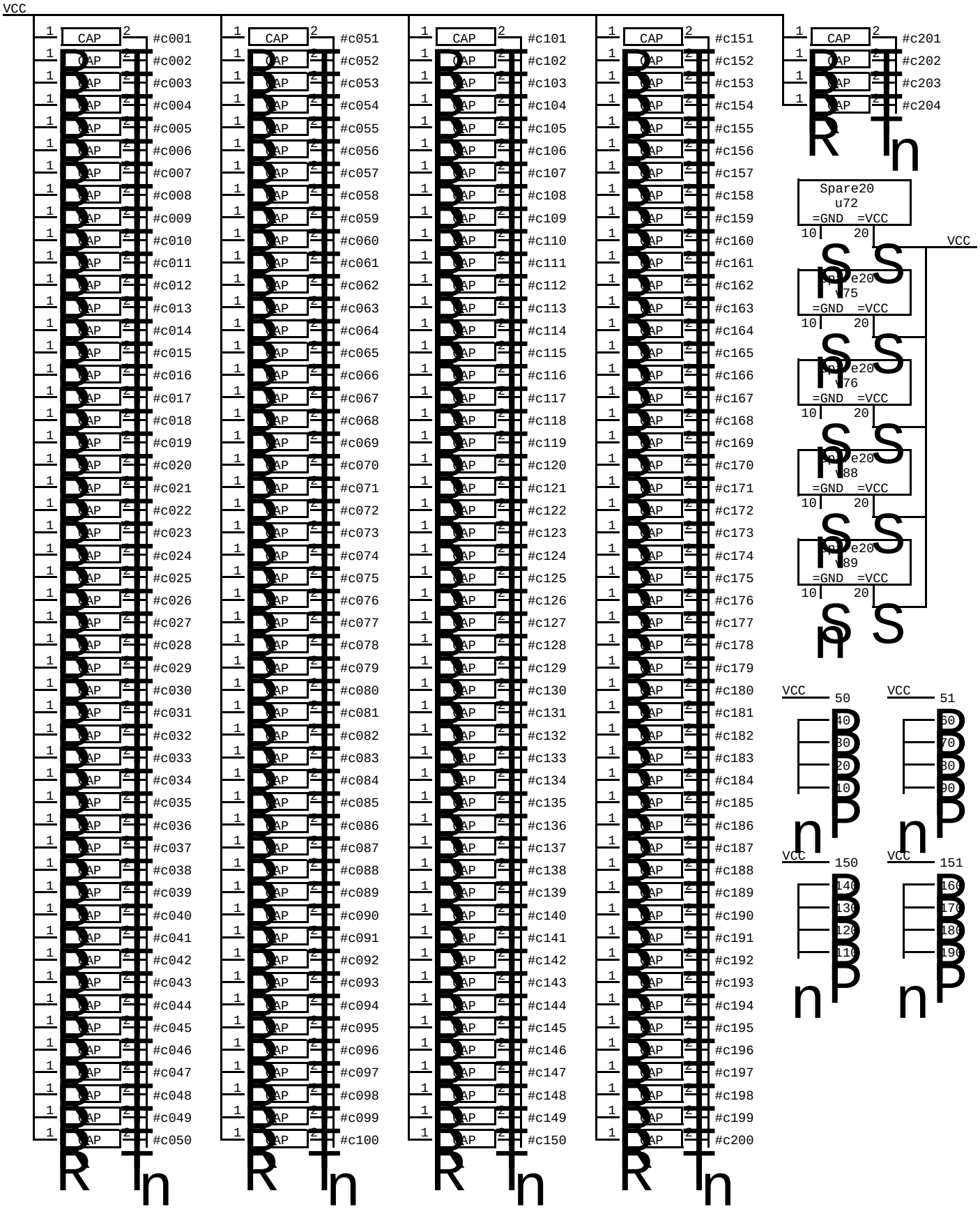
WARNING! This data is not guaranteed to be correct!



WARNING! This data is not guaranteed to be correct!



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	General Purpose 8-bit Port	CPE35.sil	Bob Garner	Ba	5/30/83	36



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	PC Odds & Ends	CPE36.sil	David Boggs	Ba	5/30/83	37