Integrated Byte Instruction Processor (IBIP)

alias Daffodil/Daisy "P-chip"

Architecture Features:

- Dandelion CP "look-alike"
  - Existent microcode is "transportable" (Mesa, InterLisp, Smalltalk)
  - 16-bit data paths
- No microtasking
  - No click structure, No "c1-c2-c3 waltz"
- Off-chip Microstore
  - 48-bit Microinstruction
  - 8K Microstore (up to 64K)
- Byte code instruction fetch unit (IFU)
  - 8 Bytes
- "Self-timed" memory interface (AP bus)
  - Double word fetch
- On-chip clock generator
  - Clock is suspended while waiting for A Chip

Technology Features:

- Lambda design rules, (λ = 2, min feature size = 4 μ)
- Estimated die size: 8.0 mm x 8.0 mm
- Polycide (No buried contacts & No second layer metal)
- Estimated number of transistors: 30K
- Estimated max power: 1.5 W
- Estimated cycle time: 140 nS