Register Name	Purpose
R	The R registers are the primary working registers of the processor. They are legal sources and destinations for virtually all arithmetic, logic and data movement operations. There are 14 R registers.
RH	The RH registers are an extension of the R registers. They are used to supply the most significant real or virtual address bits. They are 8 bits wide so real and virtual addresses up to 24 bits may be supported. There are only 14 (although maybe 16) RH registers. Note that in the current memory mapping scheme 2 to 4 of the bits that could be used to hold real address information are used for flag bits. This restricts real addresses to 20-22 bits.
Q	The Q Register is another scratchpad register. It is used in double length shifting operations (multiply, divide). It is also used as an independently addressed scratchpad register.
U	There are 128 U registers for general use. In future versions of the IBIP, there may be 256. They have one read port and one write port. It is not possible to both read and write the U registers in a single instruction. The U registers are legal sources and destinations for most arithmetic, logical and rotating operations. It is not possible to shift or rotate a value by 1 bit on the way to a U register. This is possible with the R and RH registers.
vPC, sPC	There are three versions of the Mesa program counter in the IBIP. For more information on the Mesa PC, see the Mesa Principles of Operation. The vPC is the least significant 16 bits of the virtual Mesa Program Counter. Note that the PC is defined to be an offset to the Code Base (CB) in the PrincOps. In the actual implementation, vPC holds the sum of the PrincOps PC and the CB. This is done so the addition need not be performed each time a byte of instruction stream is fetch from memory. The upper 8 bits of virtual program counter are held in an RH register. The sPC is the second version of the Mesa Program Counter. The sPC is the saved program counter. It is saved (from vPC) every time a new Mesa byte code interpretation is begun. This is signalled by IBDisp (without a trap) or AlwaysIBDisp. The Emulator uses sPC to calculate jump targets (all jump targets are computed relative to the value of the PC had at the beginning of the byte code) and to restart after traps. Note the vPC addresses bytes in memory. When doing arithmetic on the sPC, one must detect the carry out of the 9th bit (bit 7) to know if a page boundry has been crossed. One must also know if the displacement to the PC was positive or negative to determine which sense of that carry indicates page cross. the CNCDisp gives the 16 bit carry, the sign of the X bus (X.0) and the carry from Bit 7 of the ALU. Robert Garner gets a headache when he thinks about this and may replace it with CCDisp=[16 bit carry,,(9 bit carry XOR X.8)]. Stay tuned. Note that when ibSE is specified, the X Bus input, assumed to be 8 bits, is sign extended to make a 16 bit quantity.
fPCp, fPCd	These two registers make up the third version of the Mesa PC. They are the real page number (fPCp) and the page displacement (fPCd) of the fetch PC. The fetch PC is used by the Instruction Buffer to point to bytes to be fetched from memory. The fPCd and vPC are loaded in the same operation (PCs_). Since only double words are fetched, the LSB of fPCd is not sent to the Bus Interface logic (a zero is sent instead).
IB	The Instruction Buffer holds bytes of the Mesa instruction stream that were prefetched. It can hold up to 8 bytes. The IB is run by an autonomous machine. It fetches a double word from memory whenever there is room. It has priority over the Mesa Emulator for use of the bus interface.
Stkp	The Mesa Evaluation stack is held in the U registers (except for the top element, TOS, which is in an R Register). The Stkp points to the second element of the stack so it can be used as an operand quickly. The Stkp is 8 bits long for two reasons: 1) it may be larger and 2) it may be placed anywhere in the U registers (see Lampson's Frame Ring proposal).
RL	The U registers may be addressed in a number of ways. In some modes RL supplies the most significant 4 bits. This may be used if local frames are kept in the U registers (see Lampson's frame ring proposal).