Latch	Read	Write	Increment/Decrement
pMIR (4)	PhaseA	PhaseB	
MIR (4)	PhaseA PhaseB	PhaseA	
R	PhaseA	PhaseB	
RH	PhaseA	PhaseB	
U-Bypass	PhaseA	PhaseB	
U	PhaseA	PhaseA (5)	
Q	PhaseA	PhaseB	
ibPtr	PhaseA	PhaseB	
ibRdPtr	PhaseB		PhaseA
LatchibRdPtr	PhaseA	PhaseB	
ibWrtPtr	PhaseB	PhaseA	PhaseA
saveib	PhaseA	PhaseB (6)	
IB	PhaseA	PhaseB	
Stkp	PhaseA	PhaseB	PhaseB
RL	PhaseA	PhaseB	
PState	PhaseA	PhaseB	
MDu	PhaseB	RespU′ (7)	
MDv	PhaseB	RespV′ (7)	
NIA	PhaseA	PhaseB	
CSA	PhaseA PhaseB	PhaseA (8)	
Xh	PhaseA PhaseB	PhaseA	
Yh	PhaseA PhaseB	PhaseA	
cadh	PhaseA	PhaseB	
rah	PhaseB (7)	PhaseA	

Notes:

1. "Read" indicates the times at which the output data should be valid.
2. "Write" indicates the times at which the write enable pulse is active.
3. "Increment/Decrement" indicates the times at which the register is written with a value derived from its last value.
4. "MIR" refers both the the microinstruction register and its decoded outputs. All the decoded outputs become valid at the beginning of PhaseA. "pMIR" is the latch receiving the next microinstruction. MIR _ pMIR in PhaseA.
5. Written with contents of U-Bypass reg in first microinstruction following the one writing U-Bypass that does not read the U registers. If a U register is read before it can be updated from U-Bypass, the U-Bypass data is substituted for the U register data.
6. When a microinstruction contains an AwIBDisp or an IBDisp that does not cause an IBDispTrap, the IB is read in PhaseA and the saveib is written with that bytecode in PhaseB.
7. See Bus Timing diagrams (IBIPSim43-46.sily)
8. NIA is the latch in which the address of the second microinstruction following the current one is formed using the branch, dispatch and trap logic. CSA is the latch which holds the address bits actually sent to the Control Store chips. CSA is loaded with NIA in PhaseA.