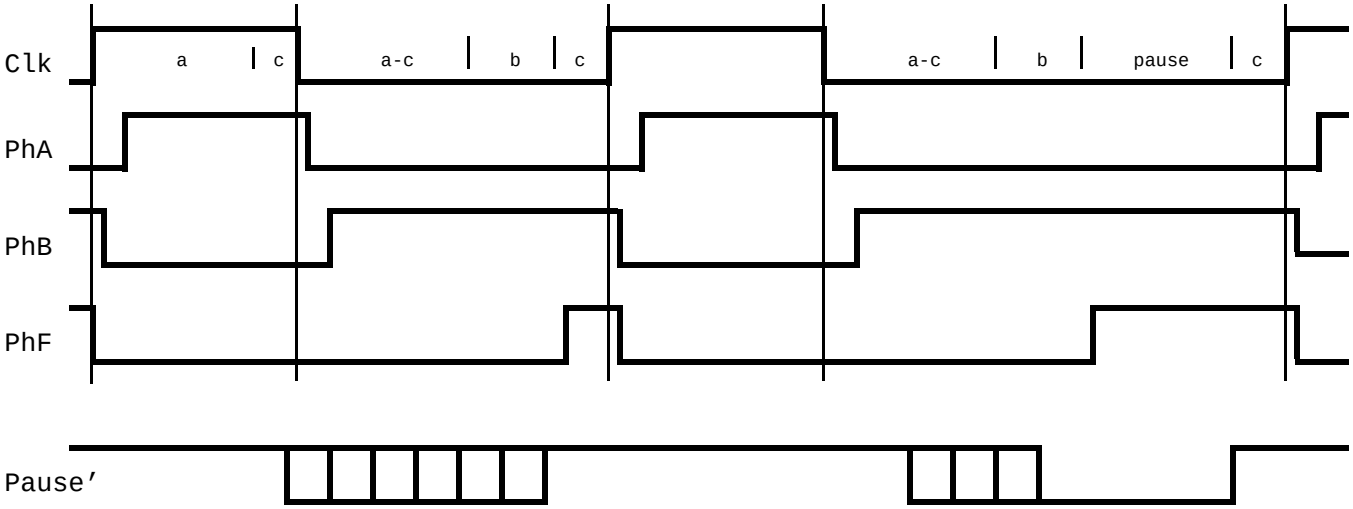

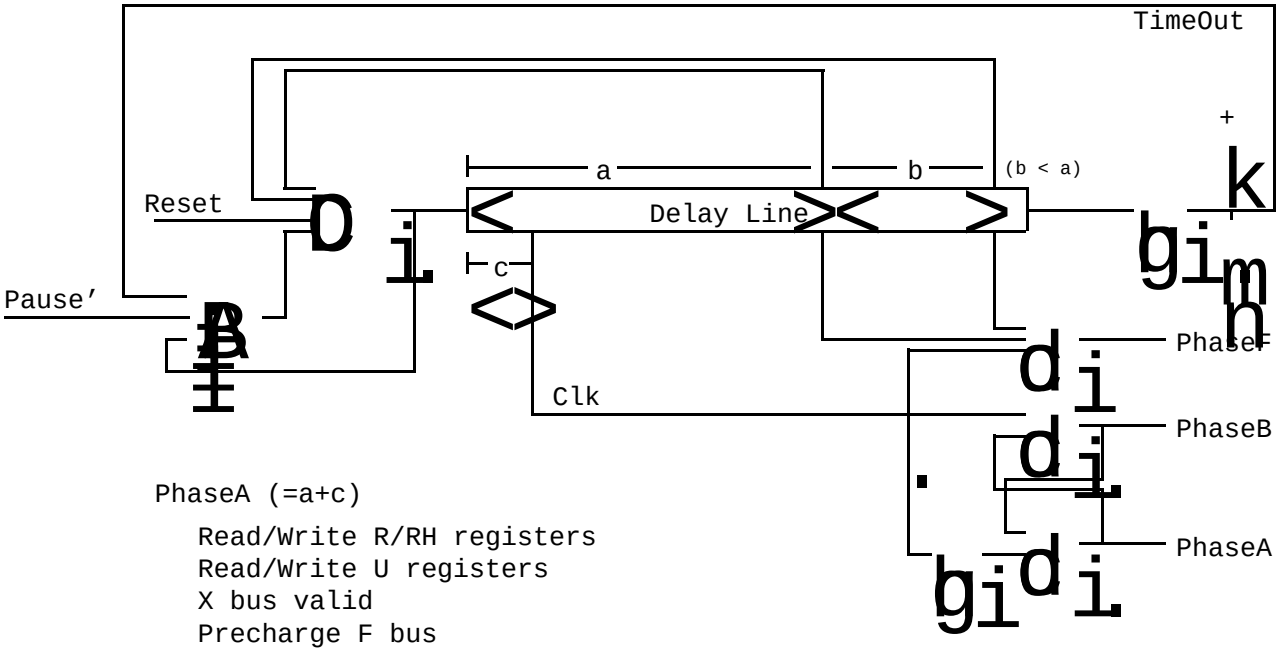

PhaseA (=a+c)

- Read/Write R/RH registers
- Read/Write U registers
- X bus valid
- Precharge F bus
- Compute ALU logical functions
- Compute F15
- Give CA, WriteData to AChip

PhaseB (=a-c+b+pause+c)

- Compute ALU carries
- F bus valid
- Precharge X bus
- Update/Write registers (Q, Fh, Stkp, vPC, fPCd)
- Precharge U/R/RH regs
- Give RA bits to AChip
- Next Microinstruction fields can be decoded

PhaseF (=pause+c)

- F Bus Valid
- c = Time for Fbus_MD, CSA_INIA or Cbus

IBIP Clocking