



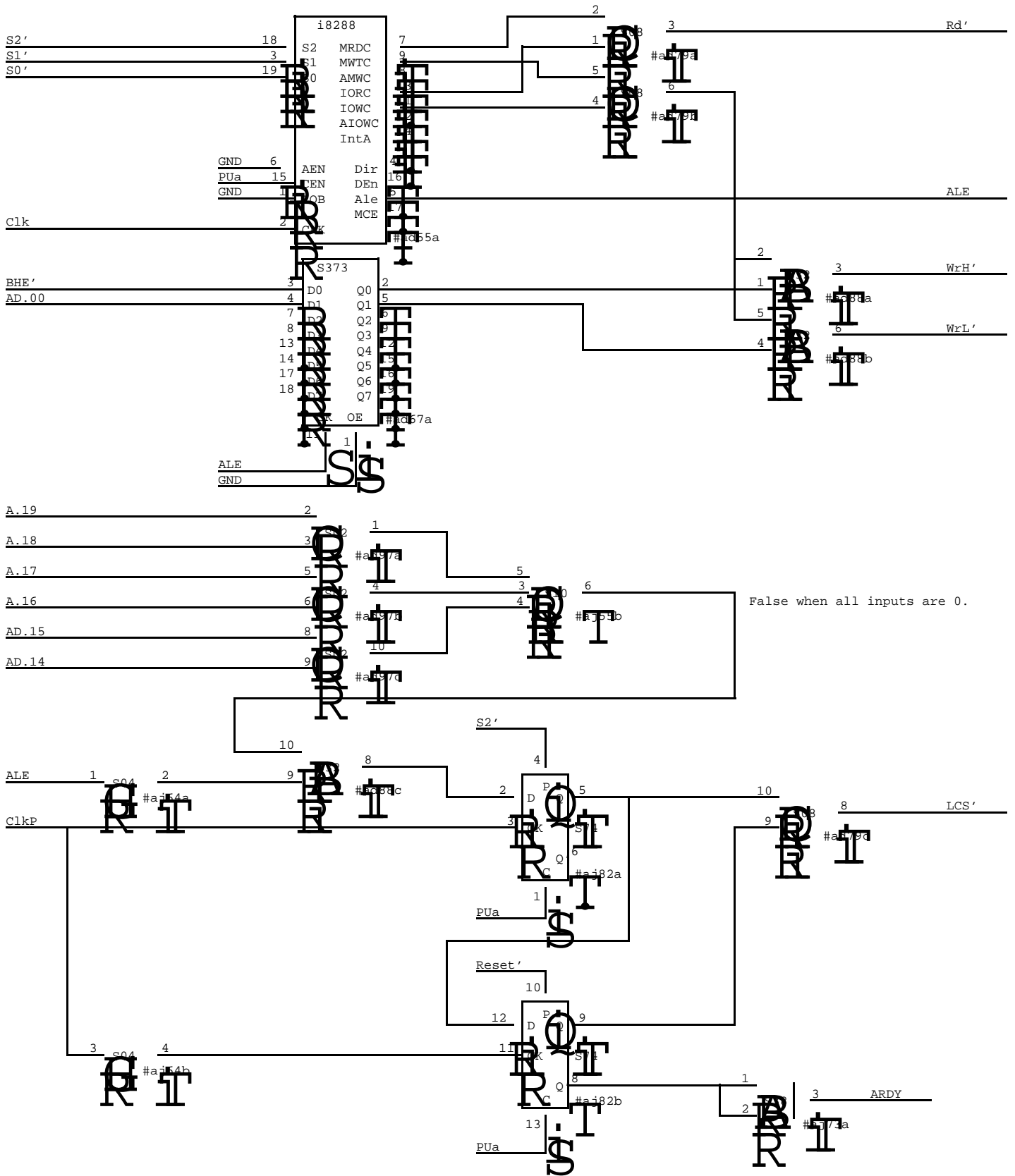
D a f f o d i l   S c h e m a t i c s

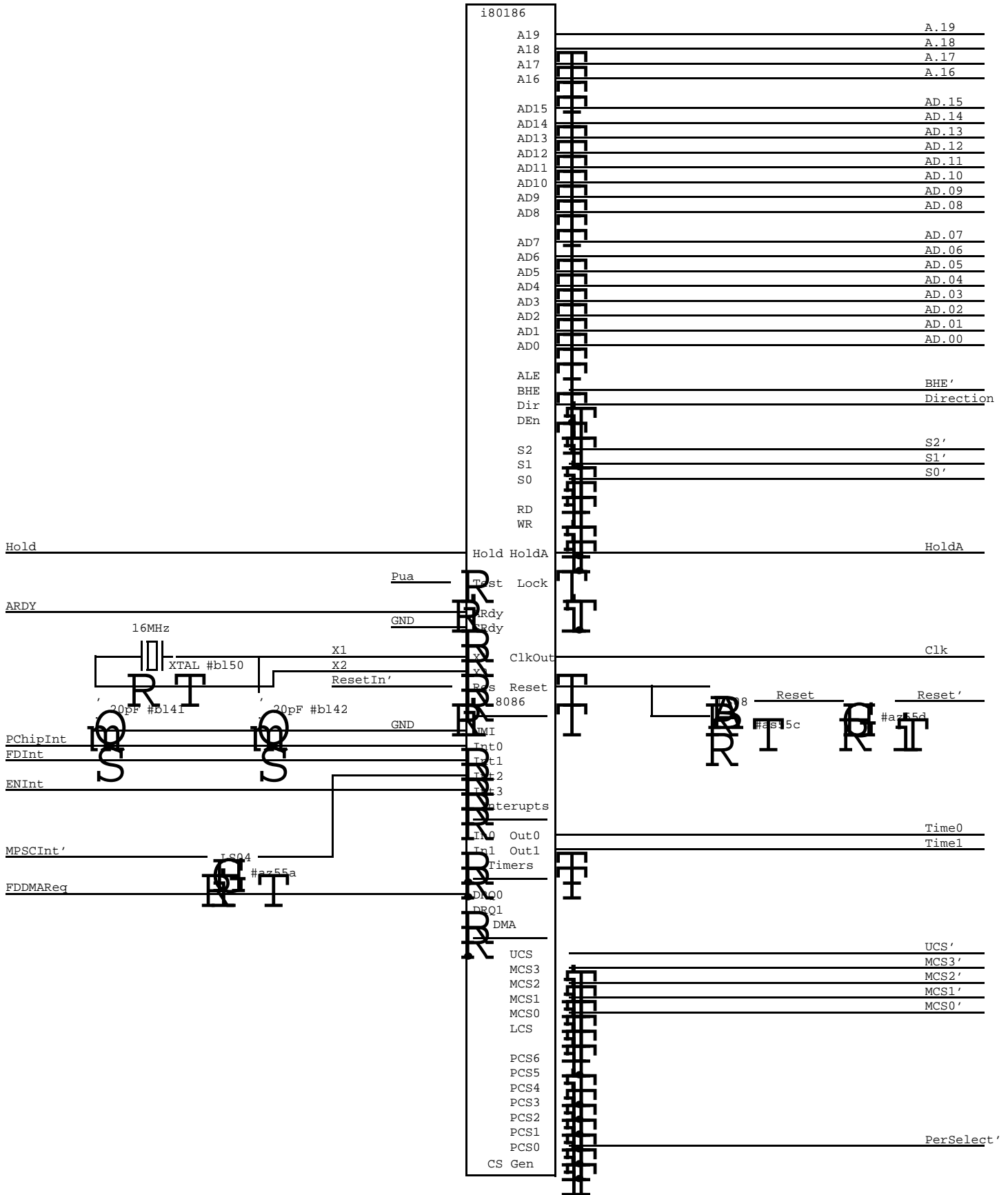
Table of contents

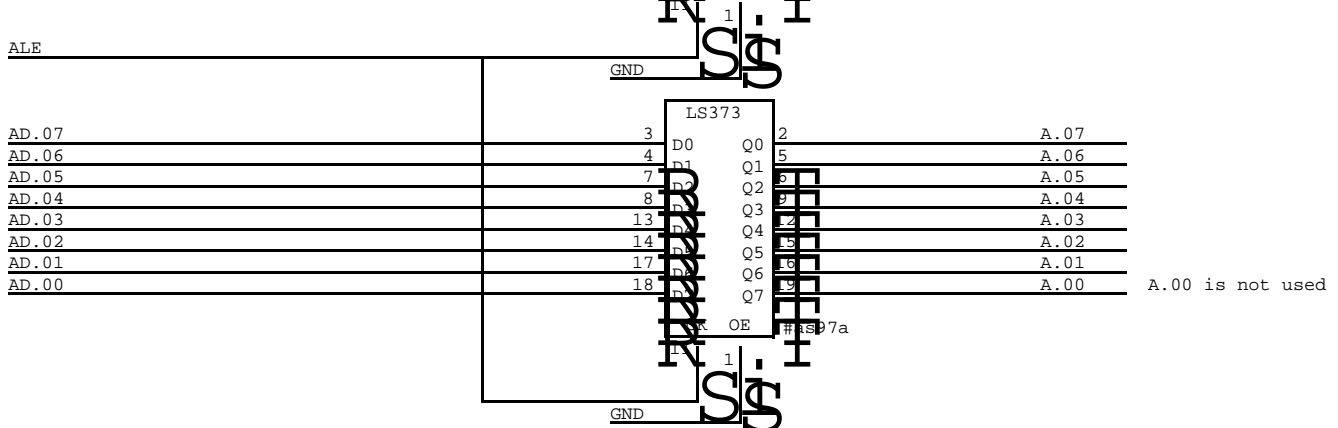
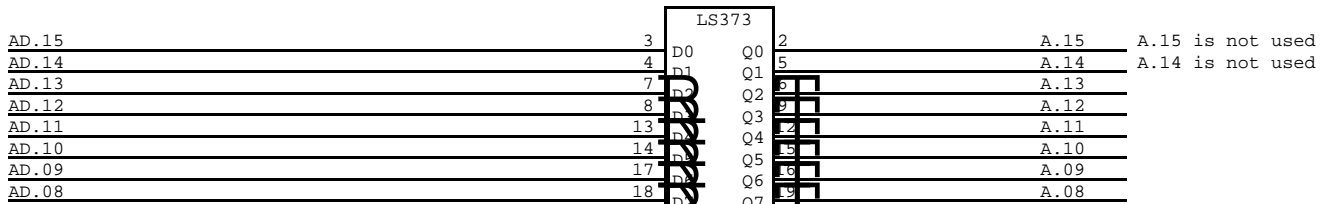
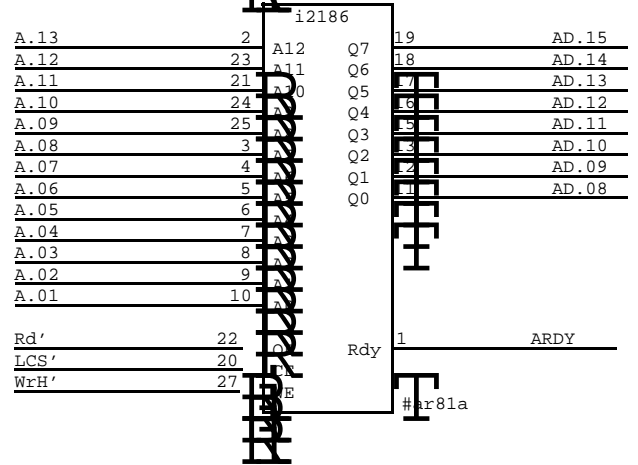
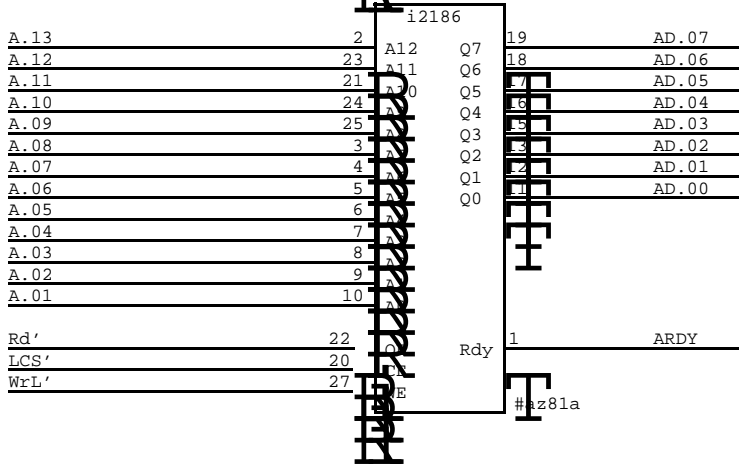
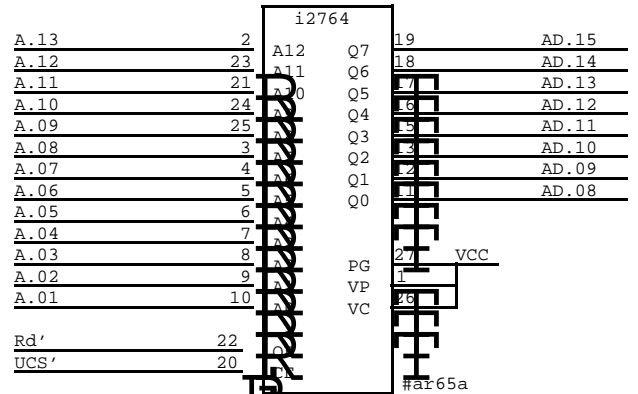
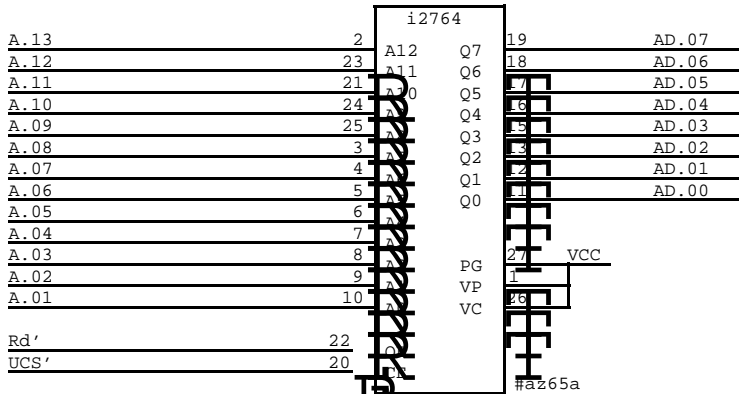
<u>TITLE</u>	<u>PAGE</u>
"A" Chip interface _____	1
80186 (logical) _____	2
Local Memory _____	3
Ethernet Controller _____	4
Keyboard/Mouse & RS232 _____	5
Floppy Disk Interface _____	6
80186 (real) _____	7
Power On Reset _____	8
Connectors & Route Stuff _____	9
Debug Ram _____	10
Timing _____	11
PLAT Layout _____	12

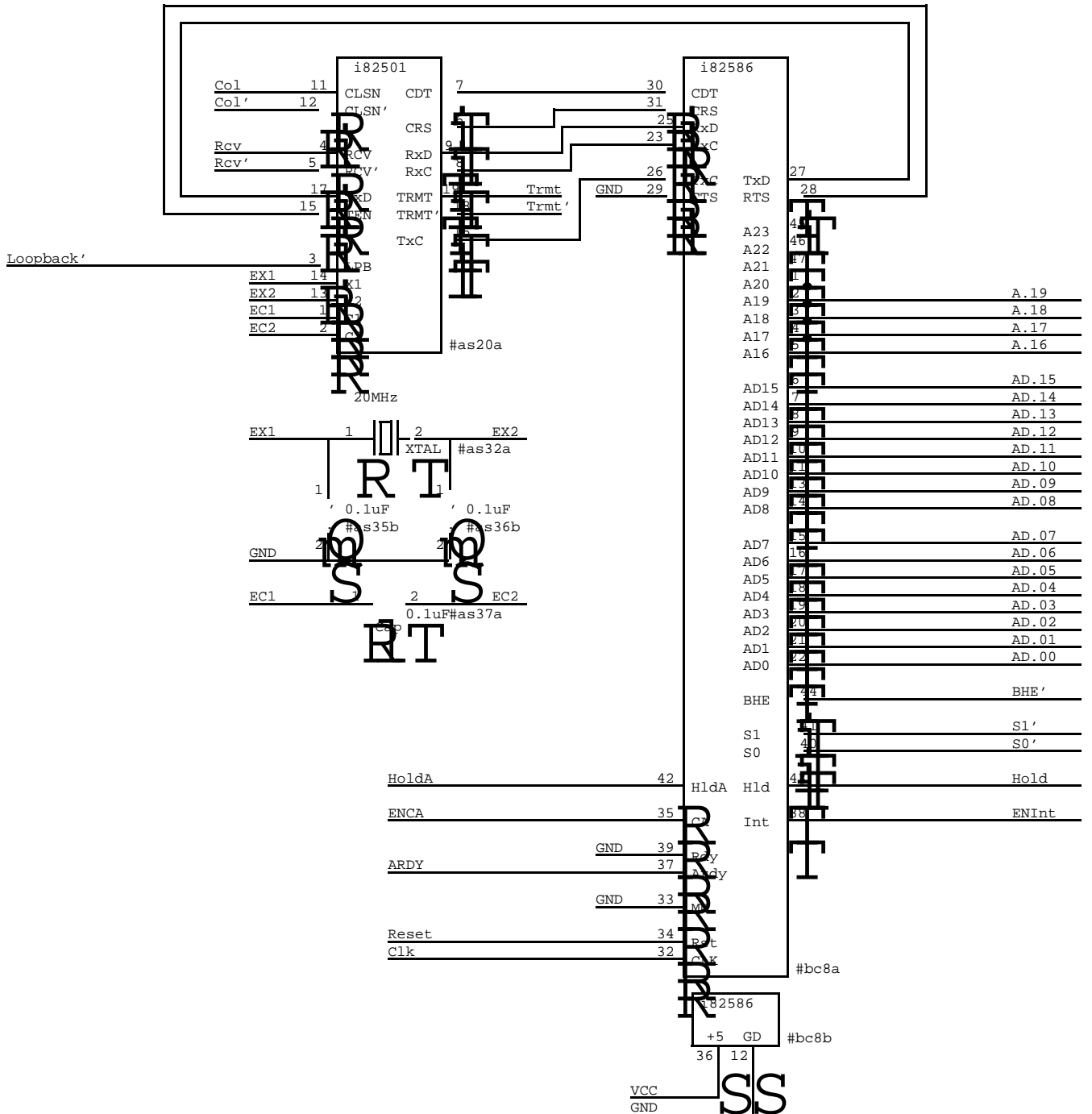
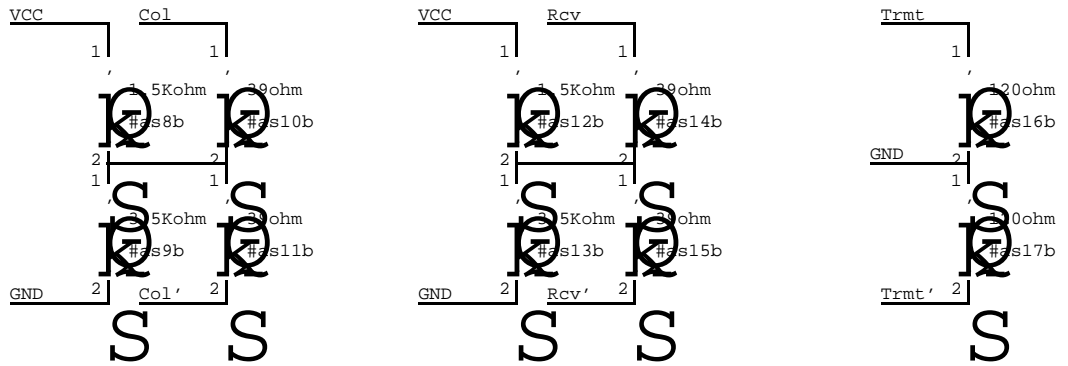
From IOP

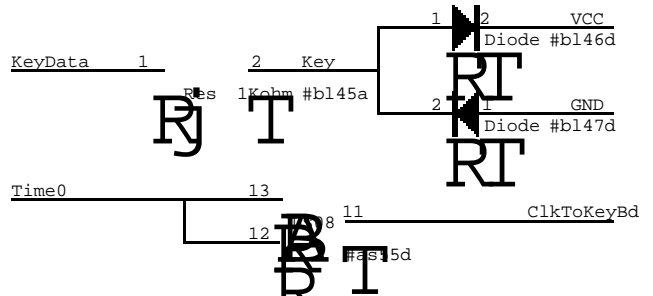
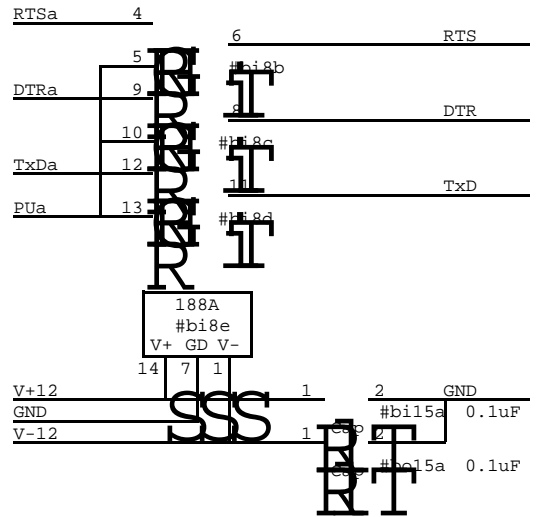
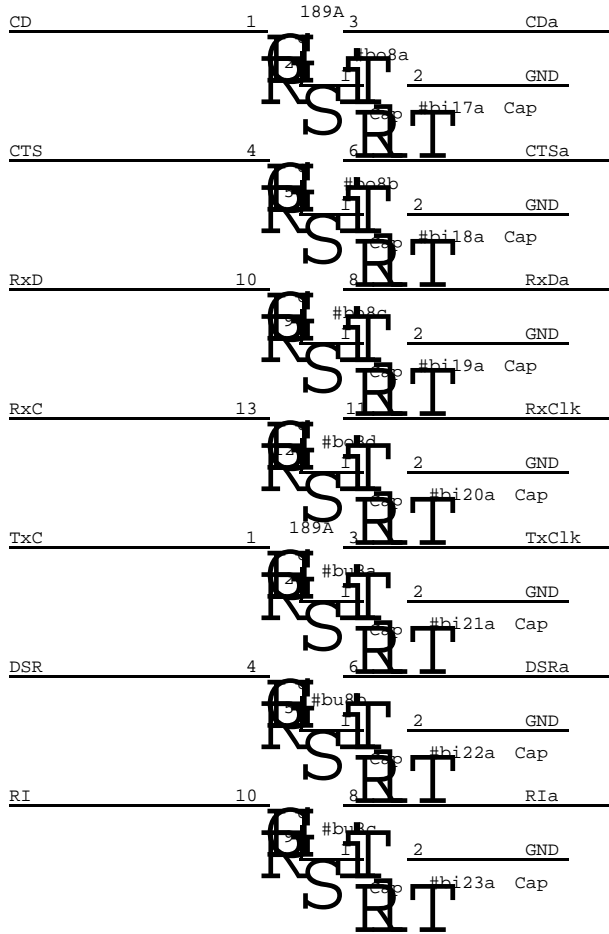
To IOP



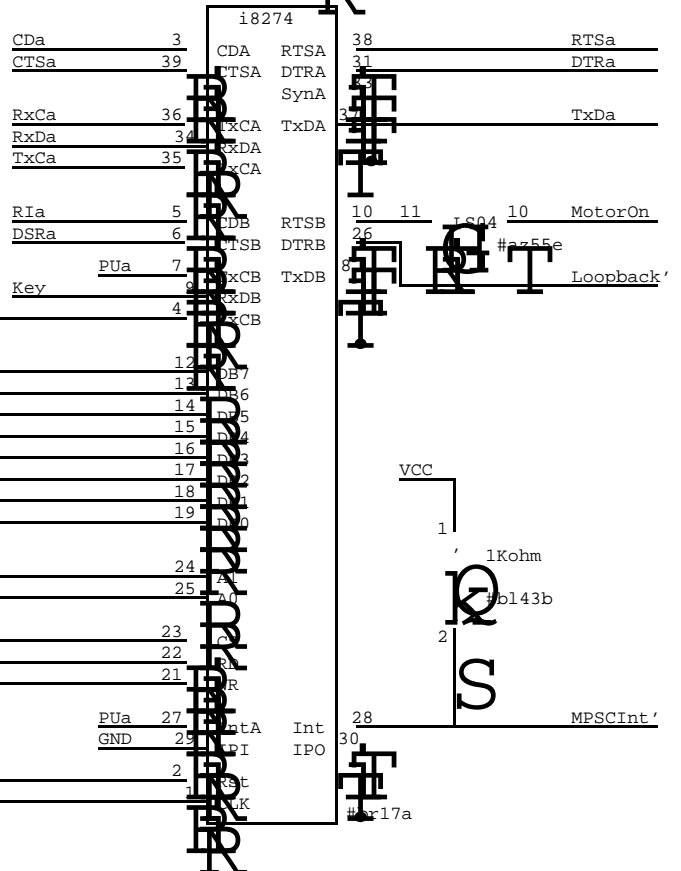
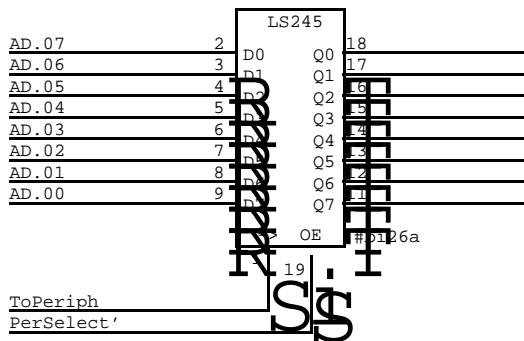
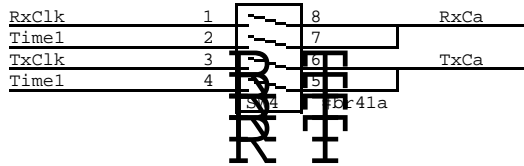


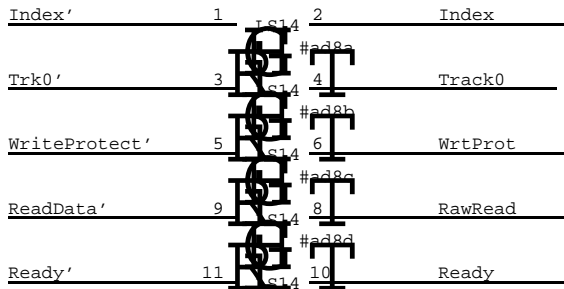




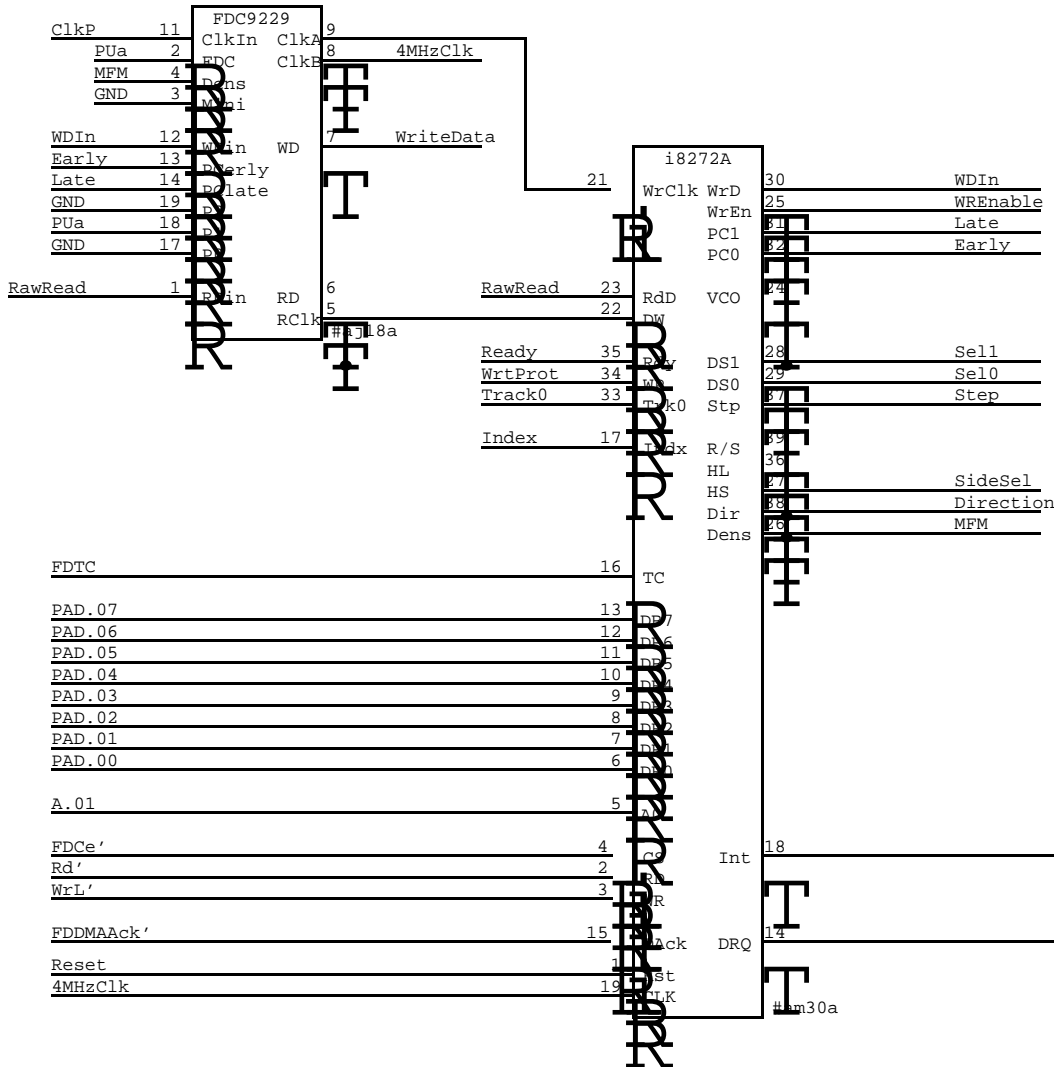
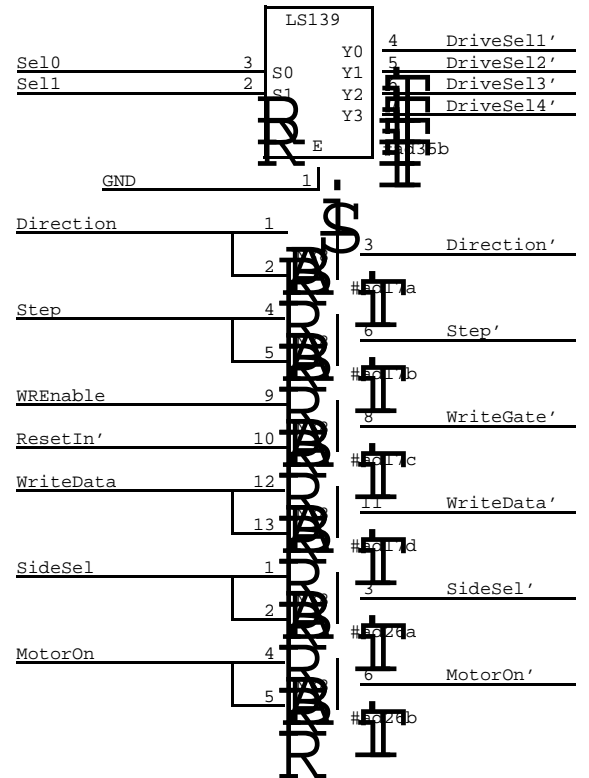
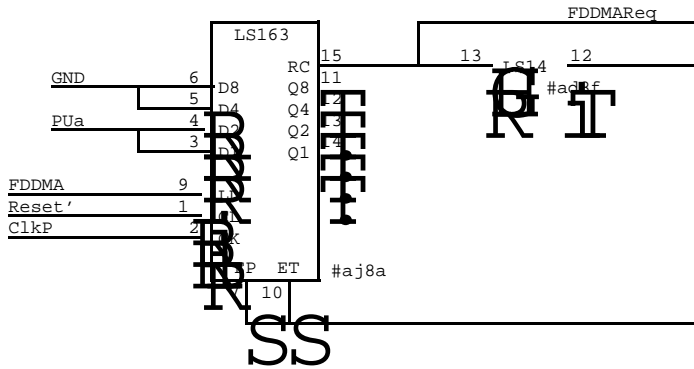


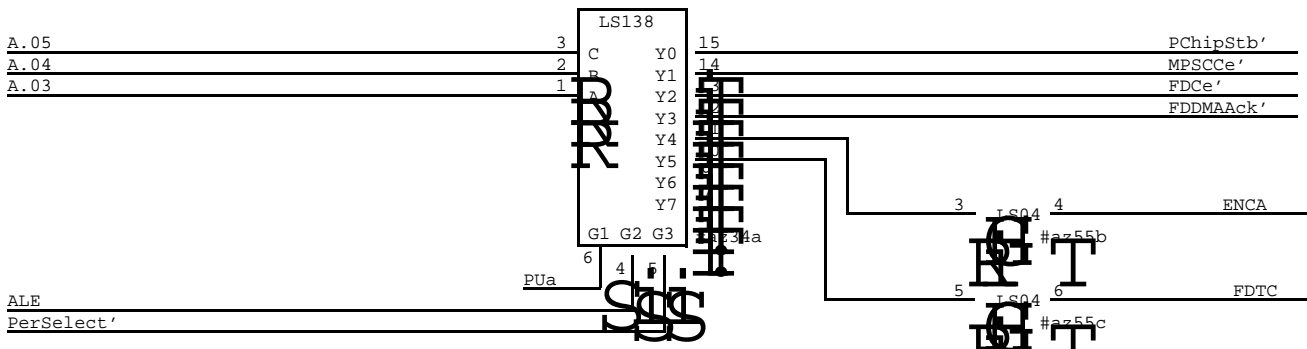
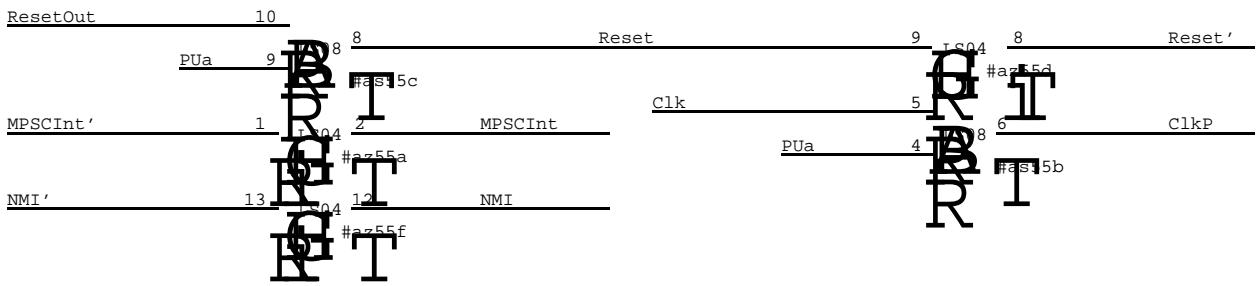
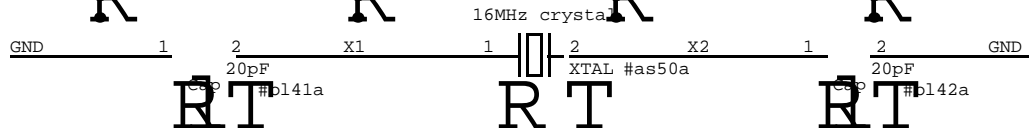
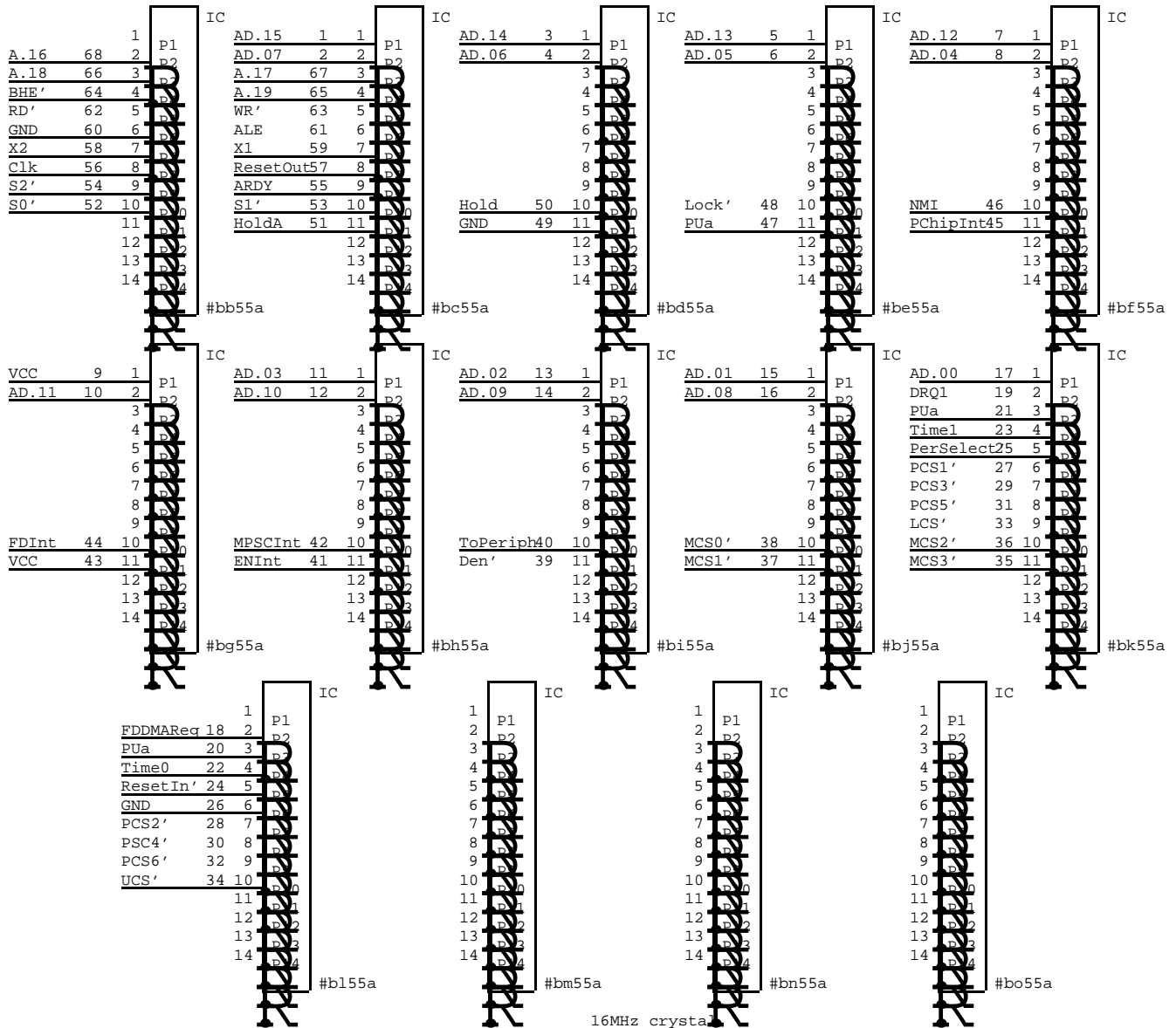
These are really jumpers shown as a switch



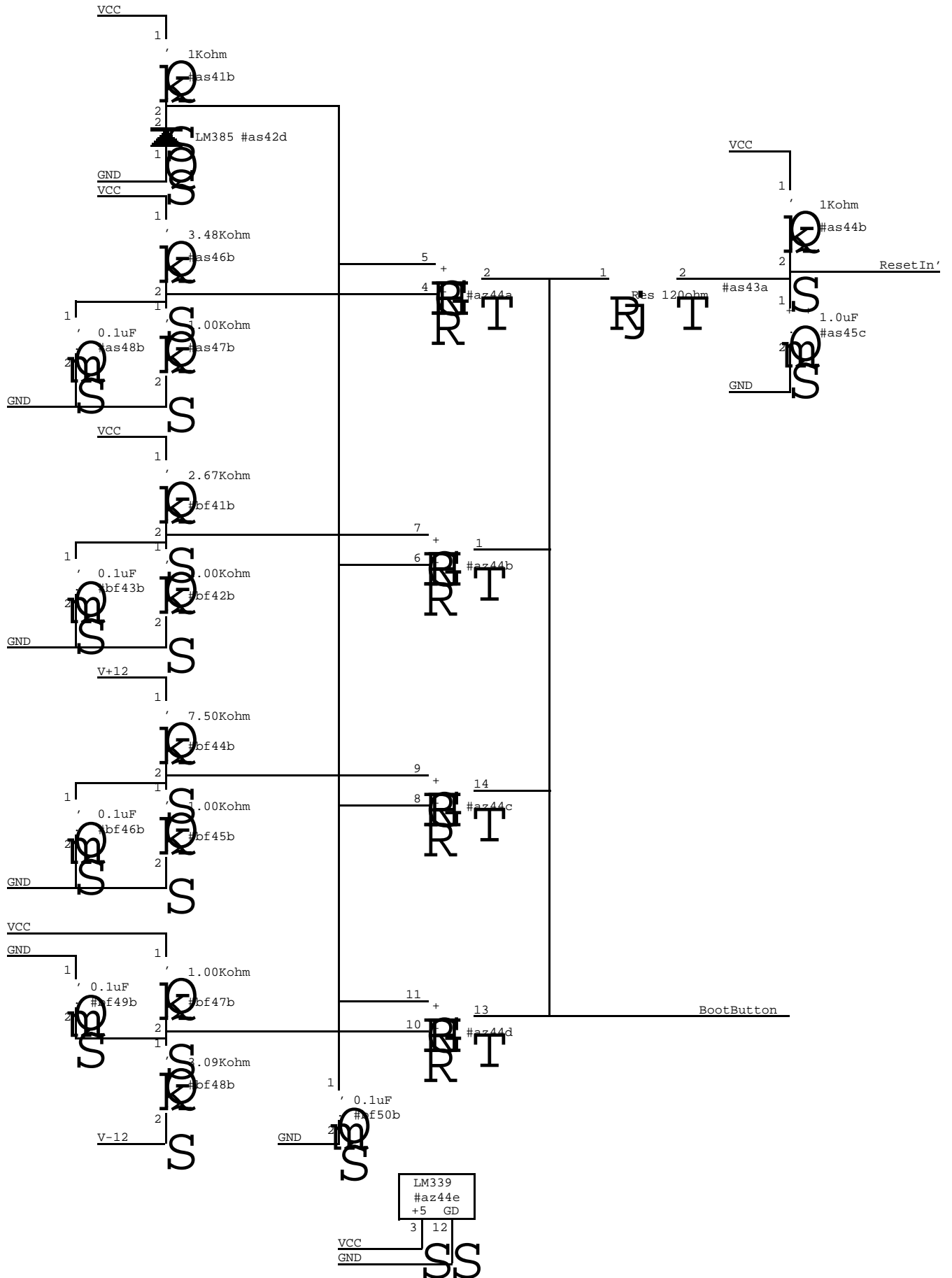


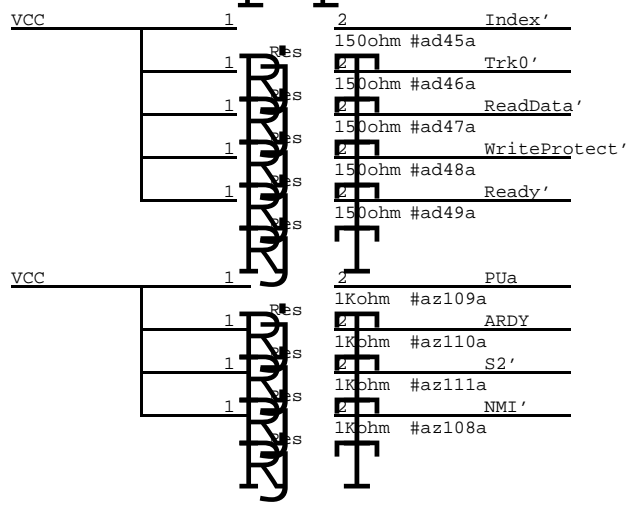
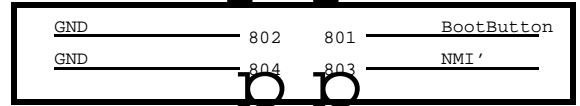
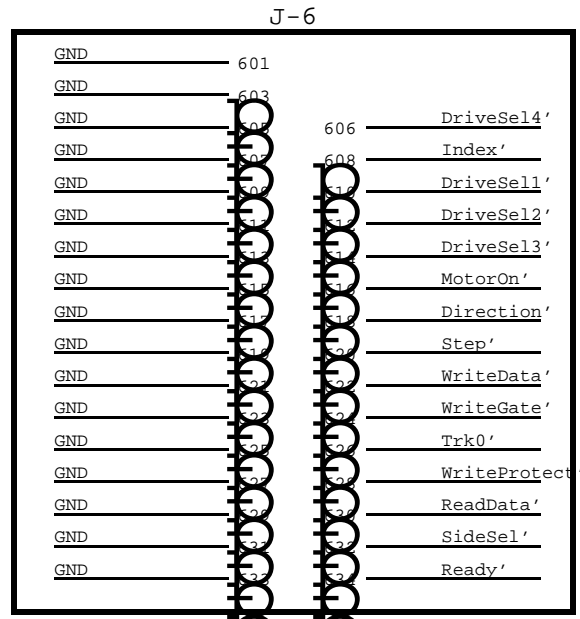
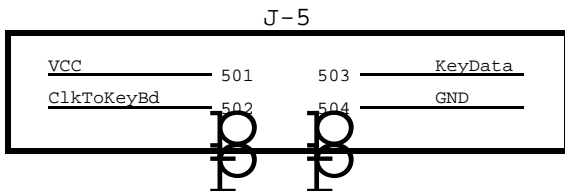
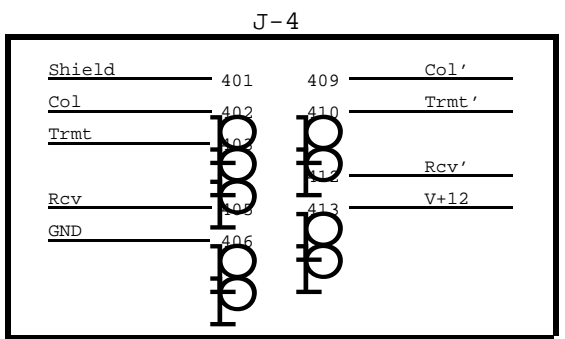
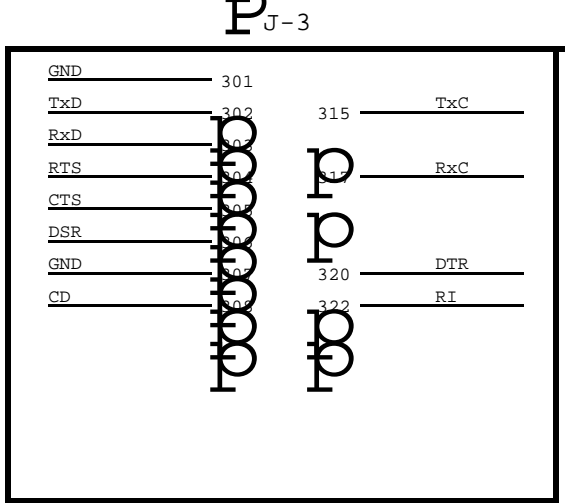
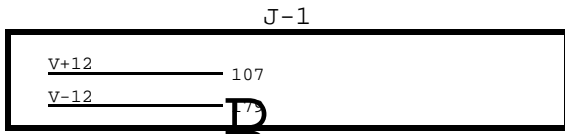
Terminators are on page 9

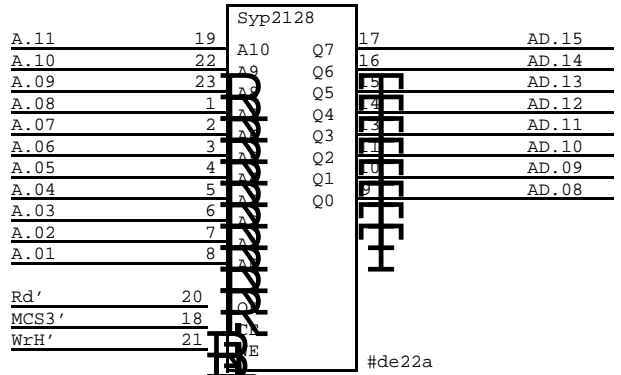
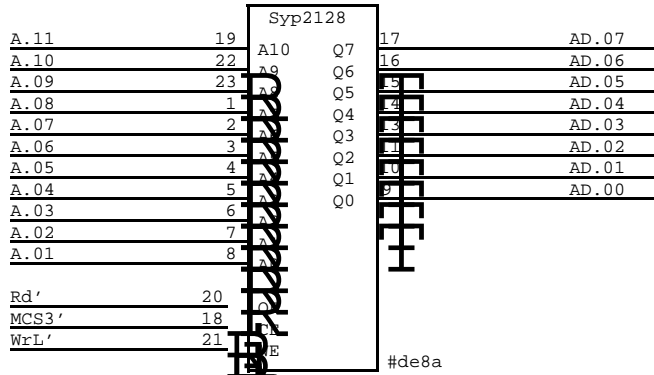
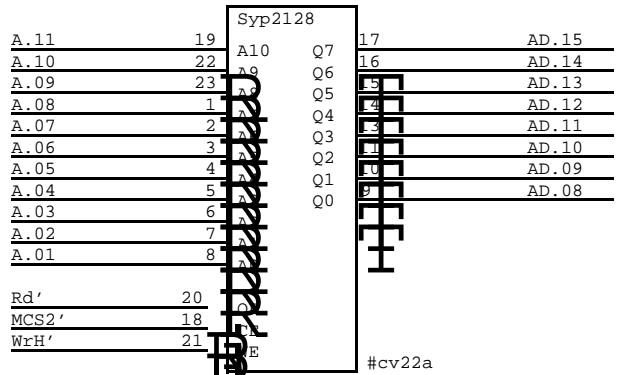
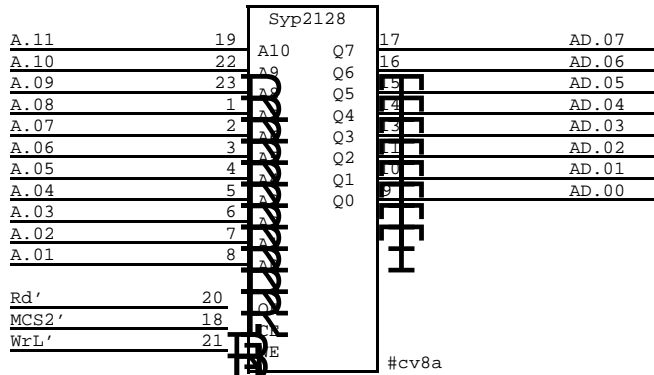
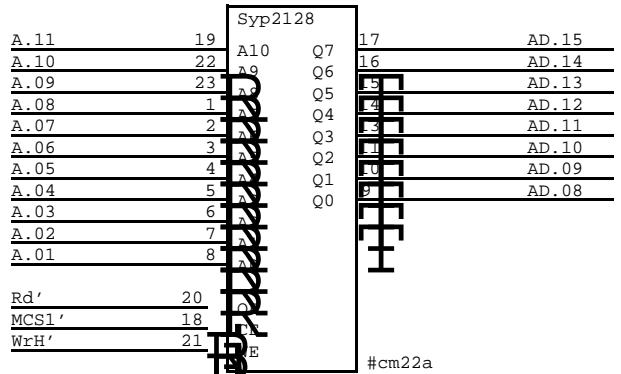
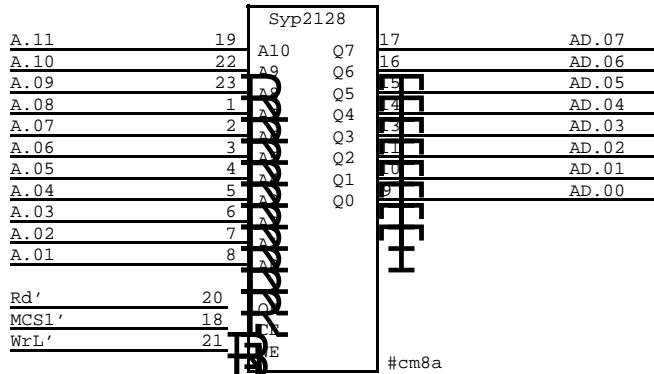
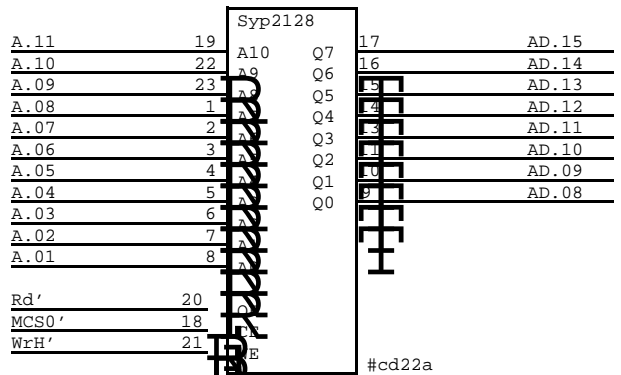
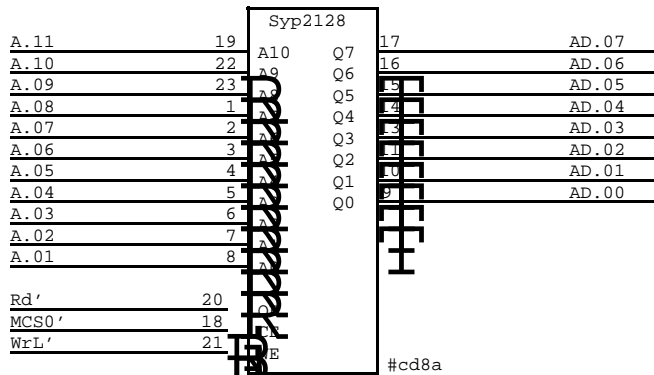


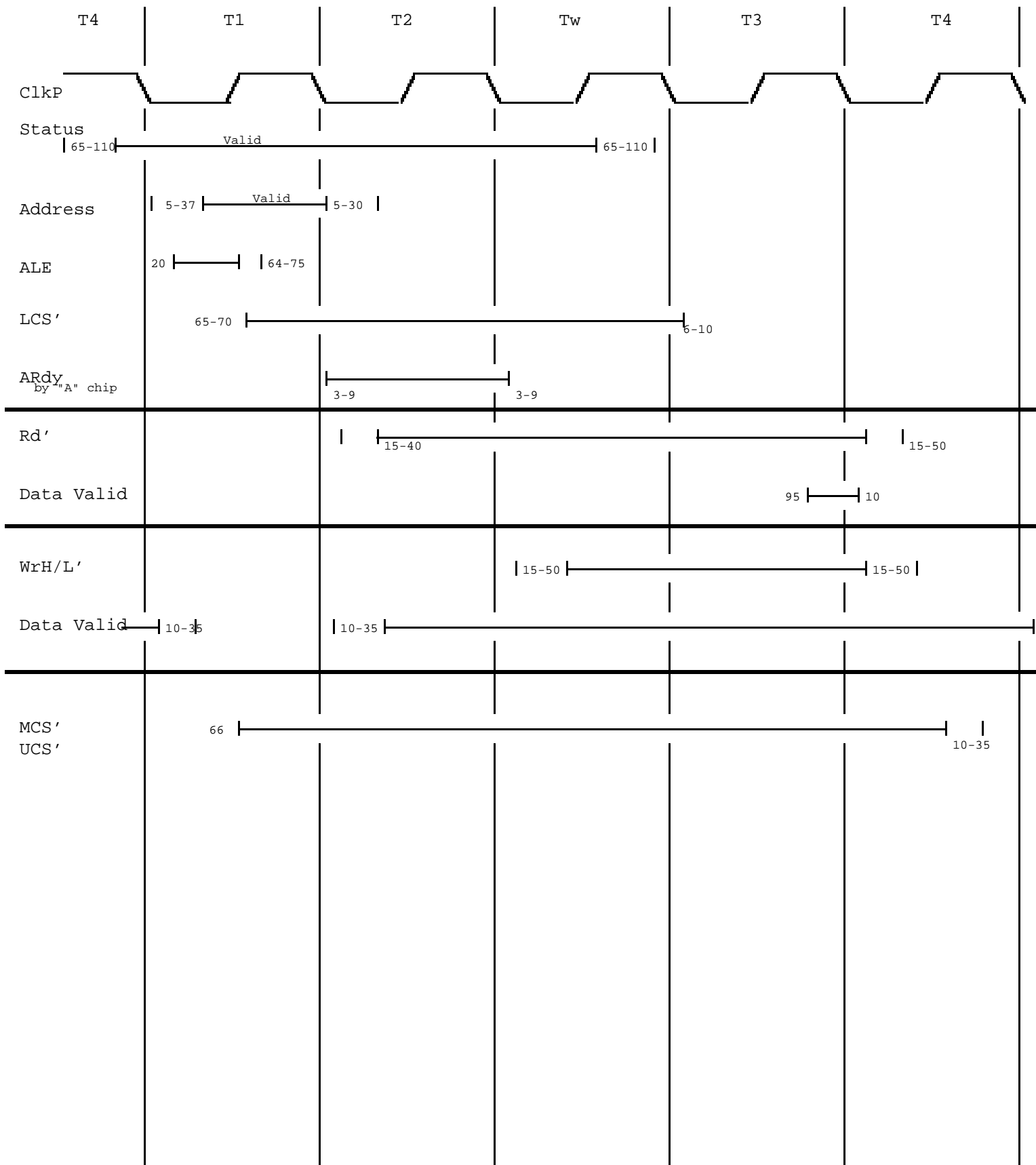










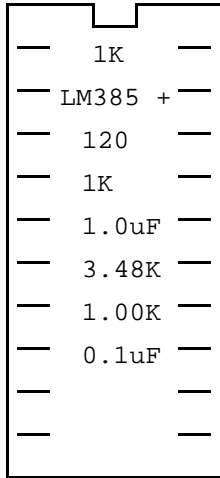


Clk is assumed to be 120ns

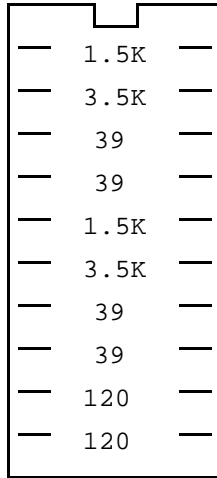
All timing is from falling edge of clk

Project	Reference	File	Designer	Rev	Date	Page
XEROX PARC	Daffodil Timing	Daff11.sil	Tim Diebert	F	6/02/83	11

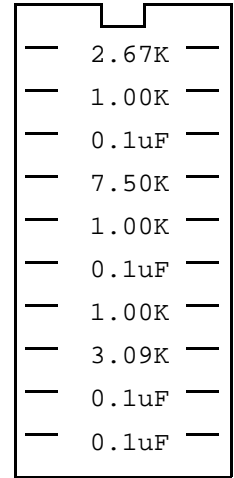
#as41



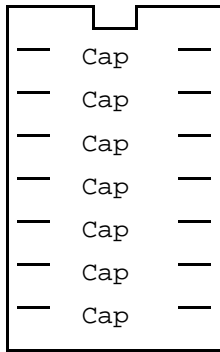
#as8



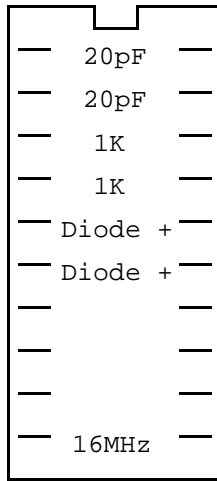
#bf41



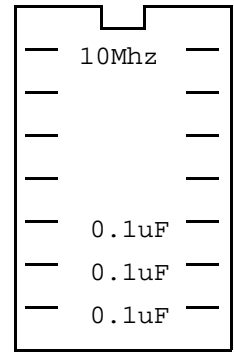
#bi17



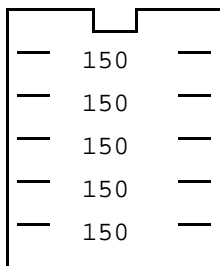
#bl41



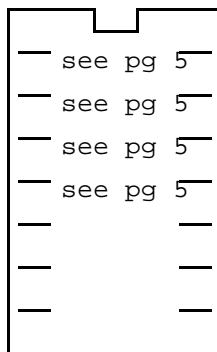
#as31



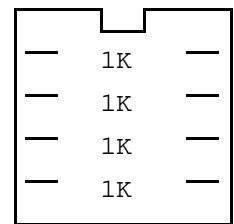
#ad45



#br41



#az108



Diskette

