



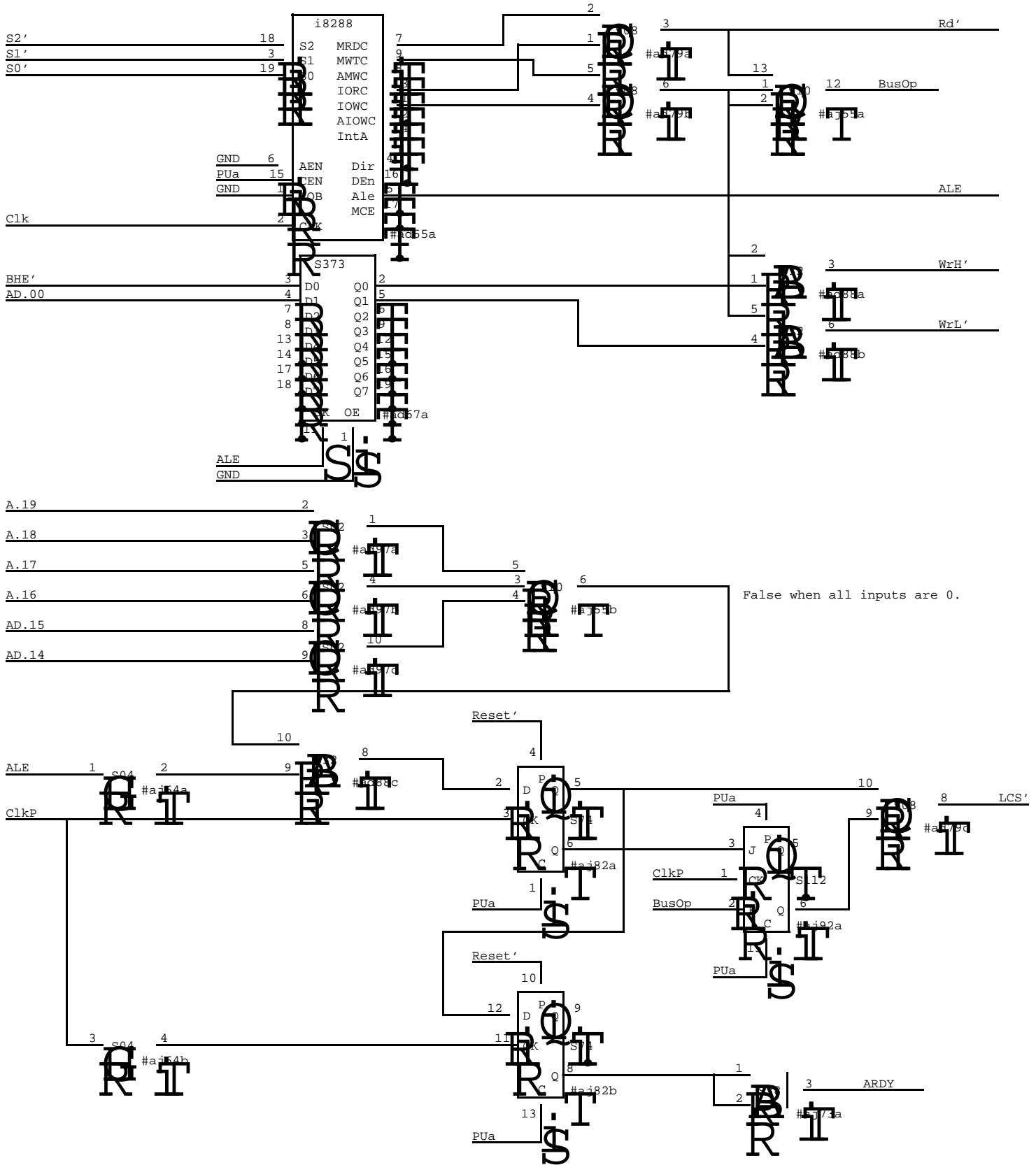
D a f f o d i l S c h e m a t i c s

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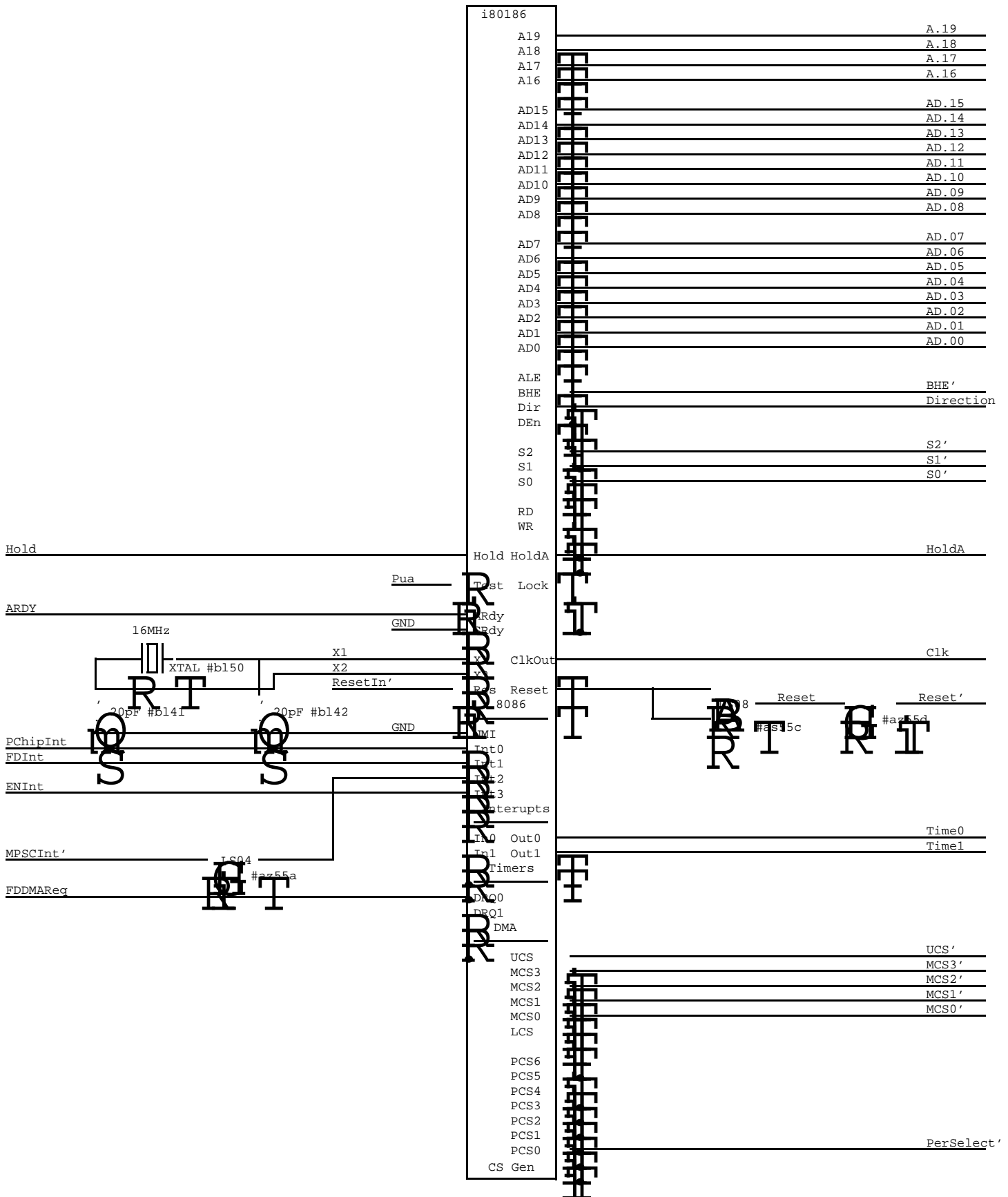
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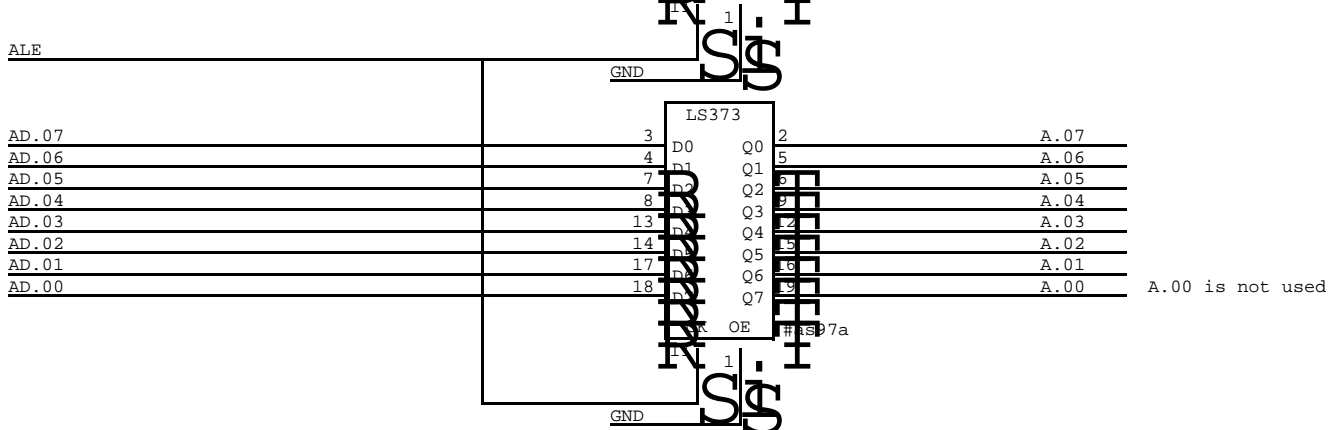
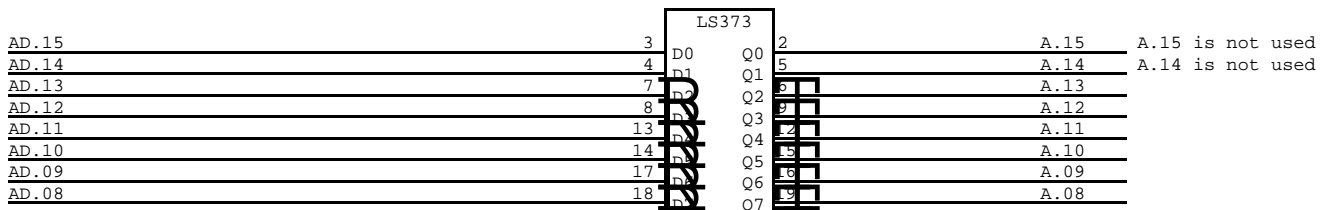
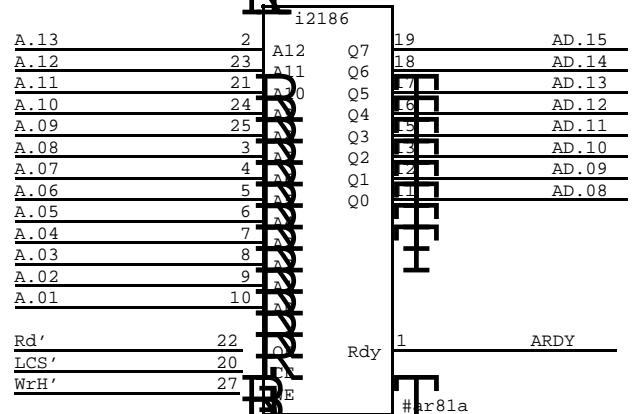
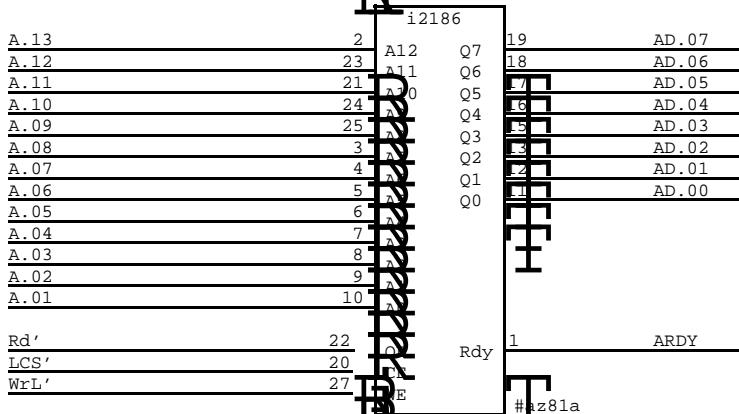
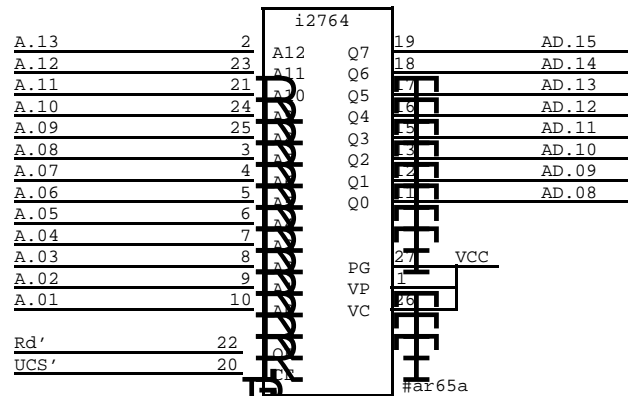
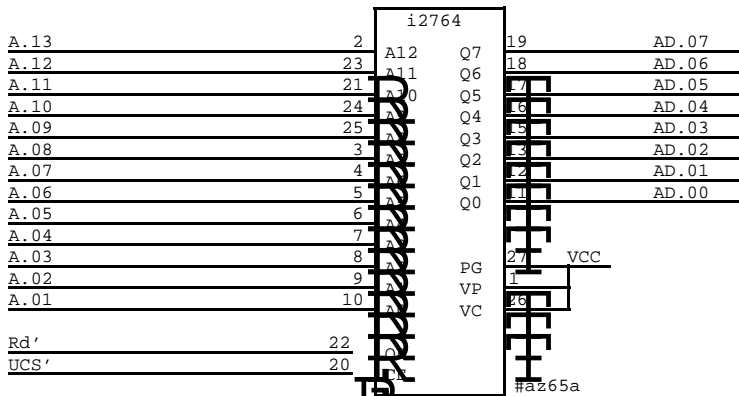
To IOP

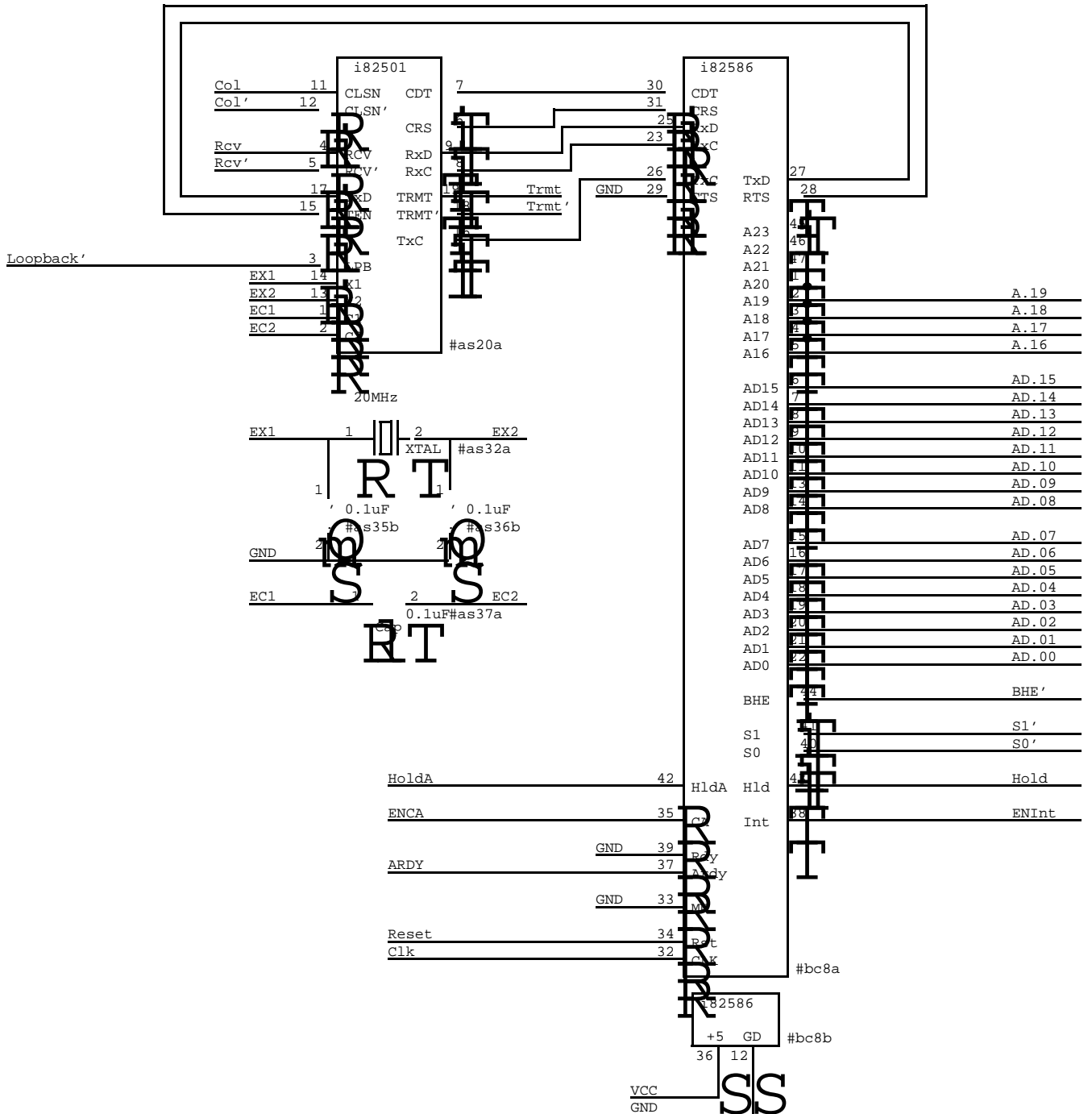
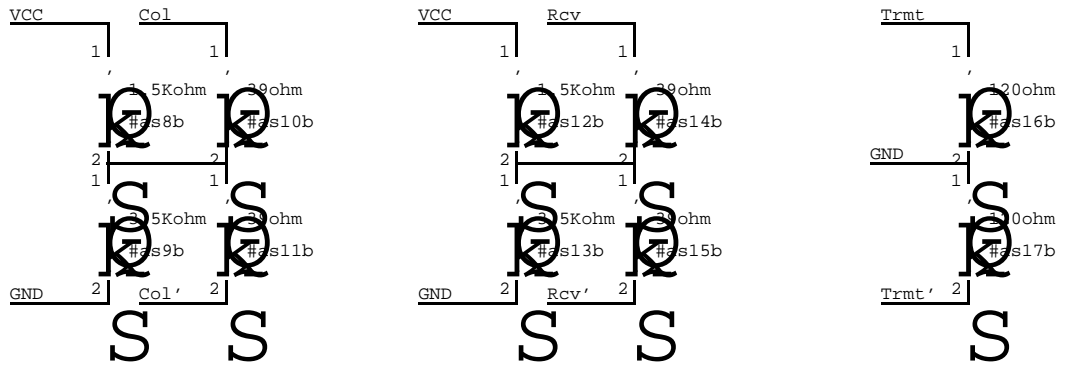


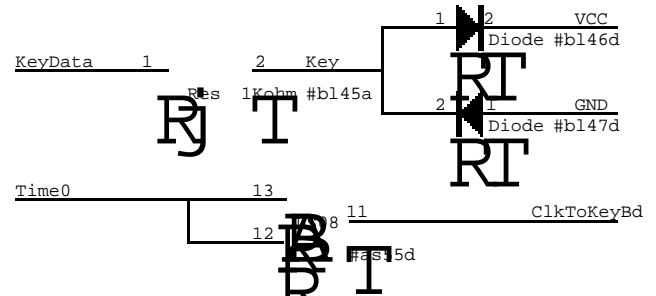
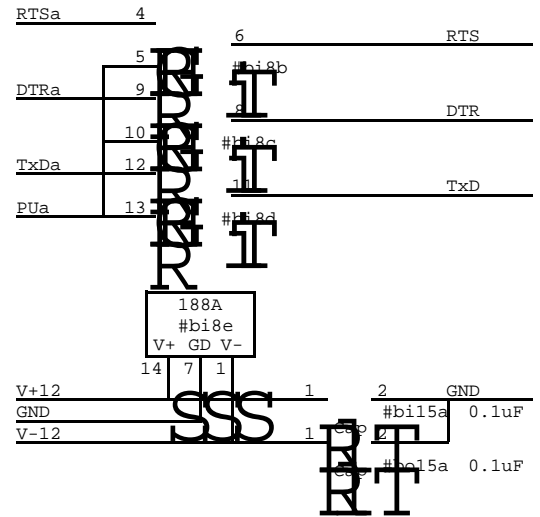
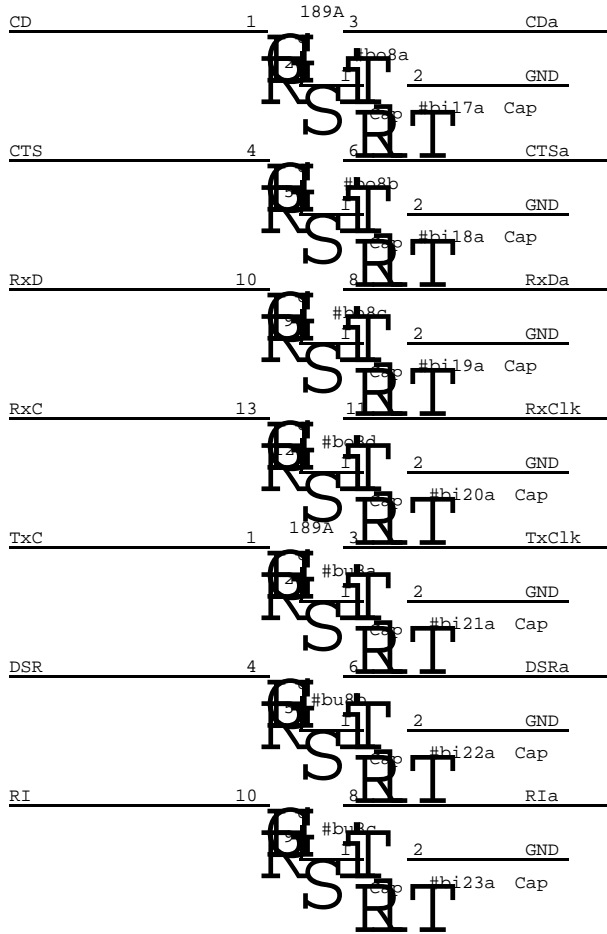
False when all inputs are 0.

XEROX PARC	Project Daffodil	Title "A" Chip Logic	File Daff01.sil	Designer Tim Diebert	Rev E	Date 9/26/83	Page 01
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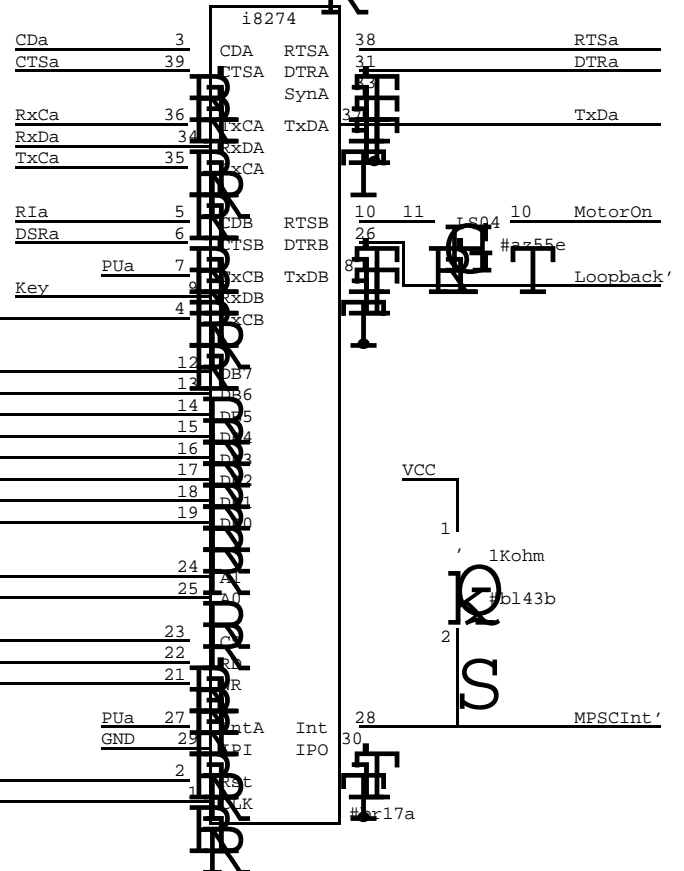
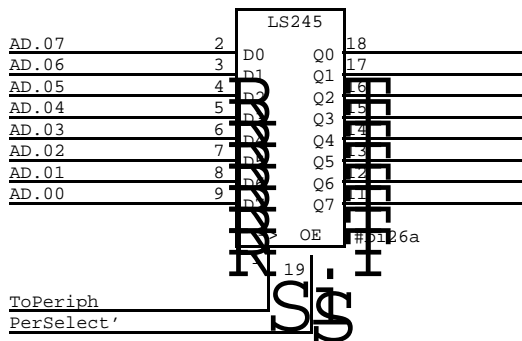
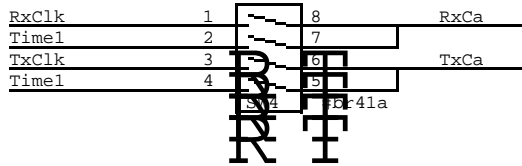


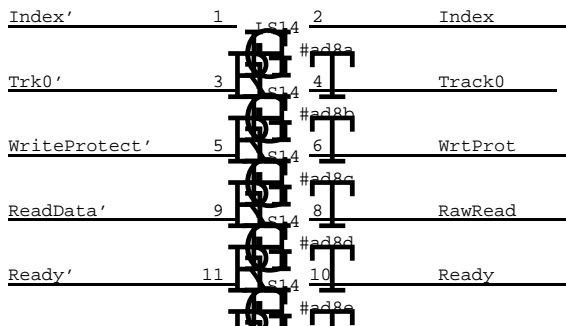




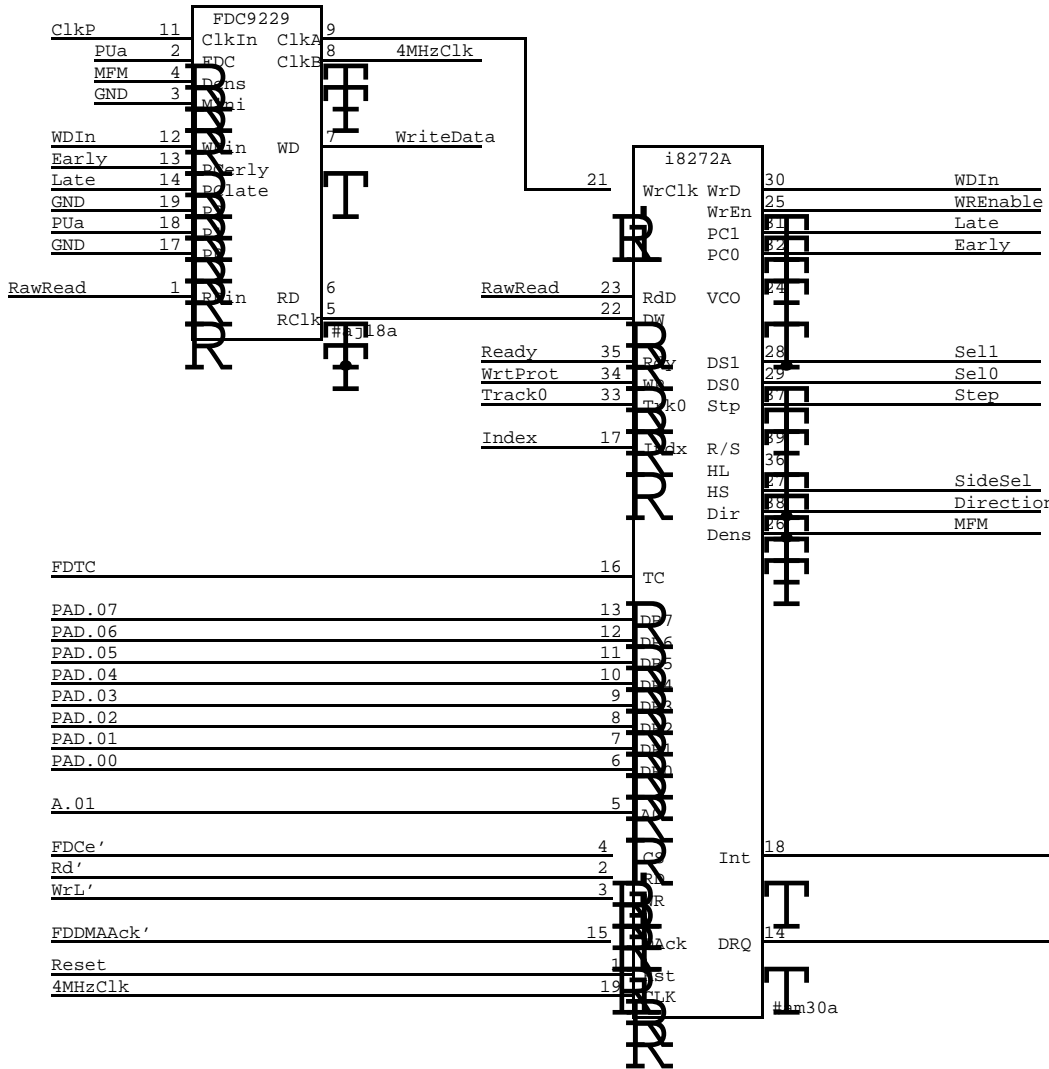
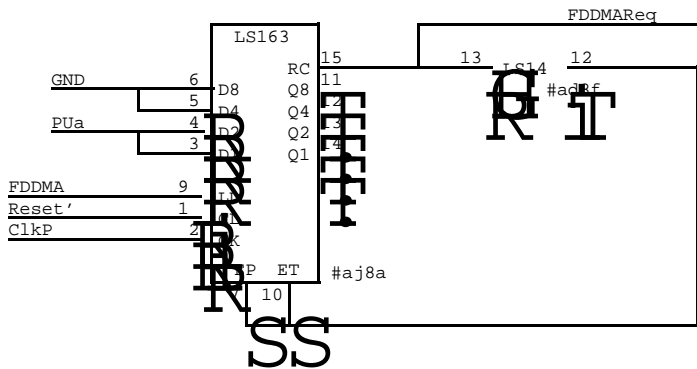
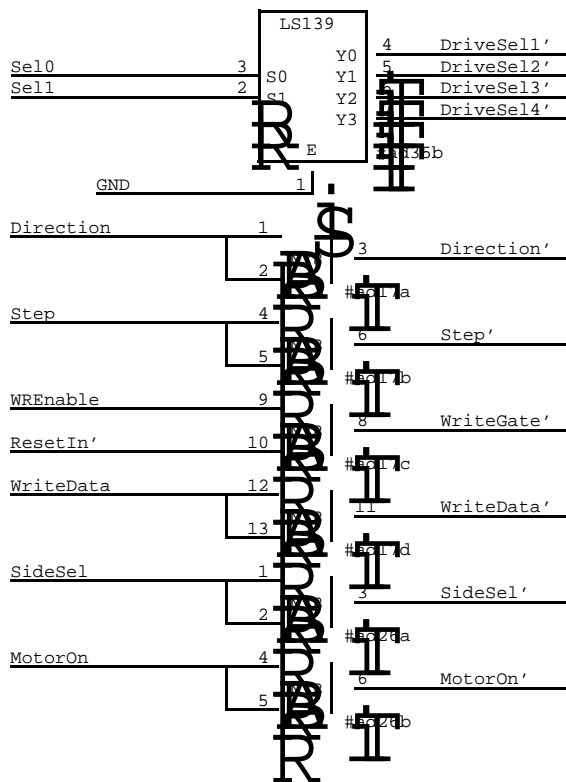


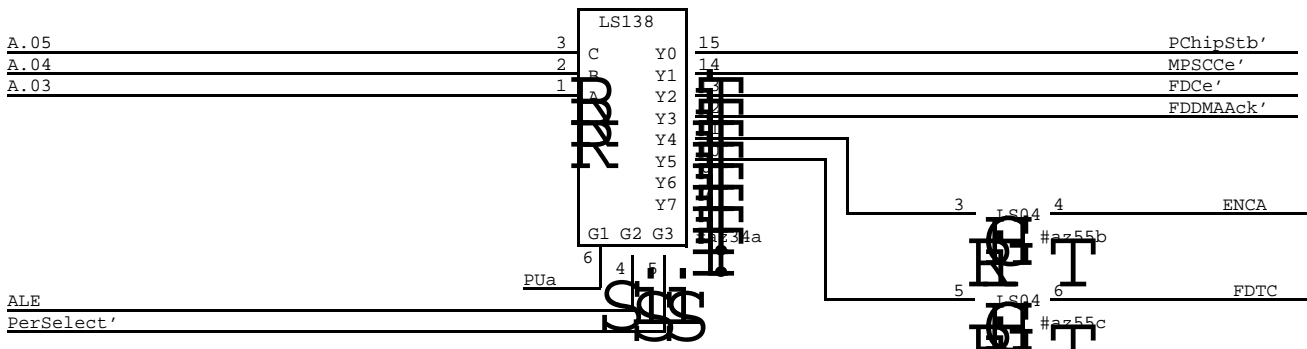
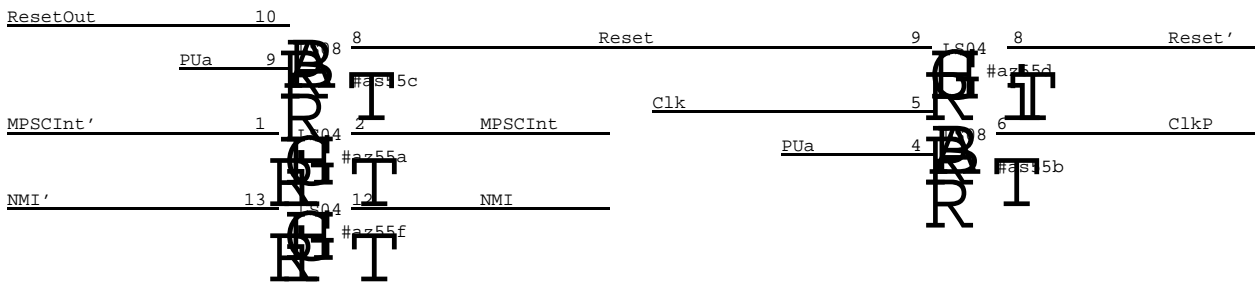
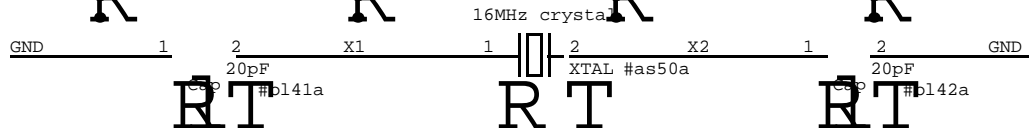
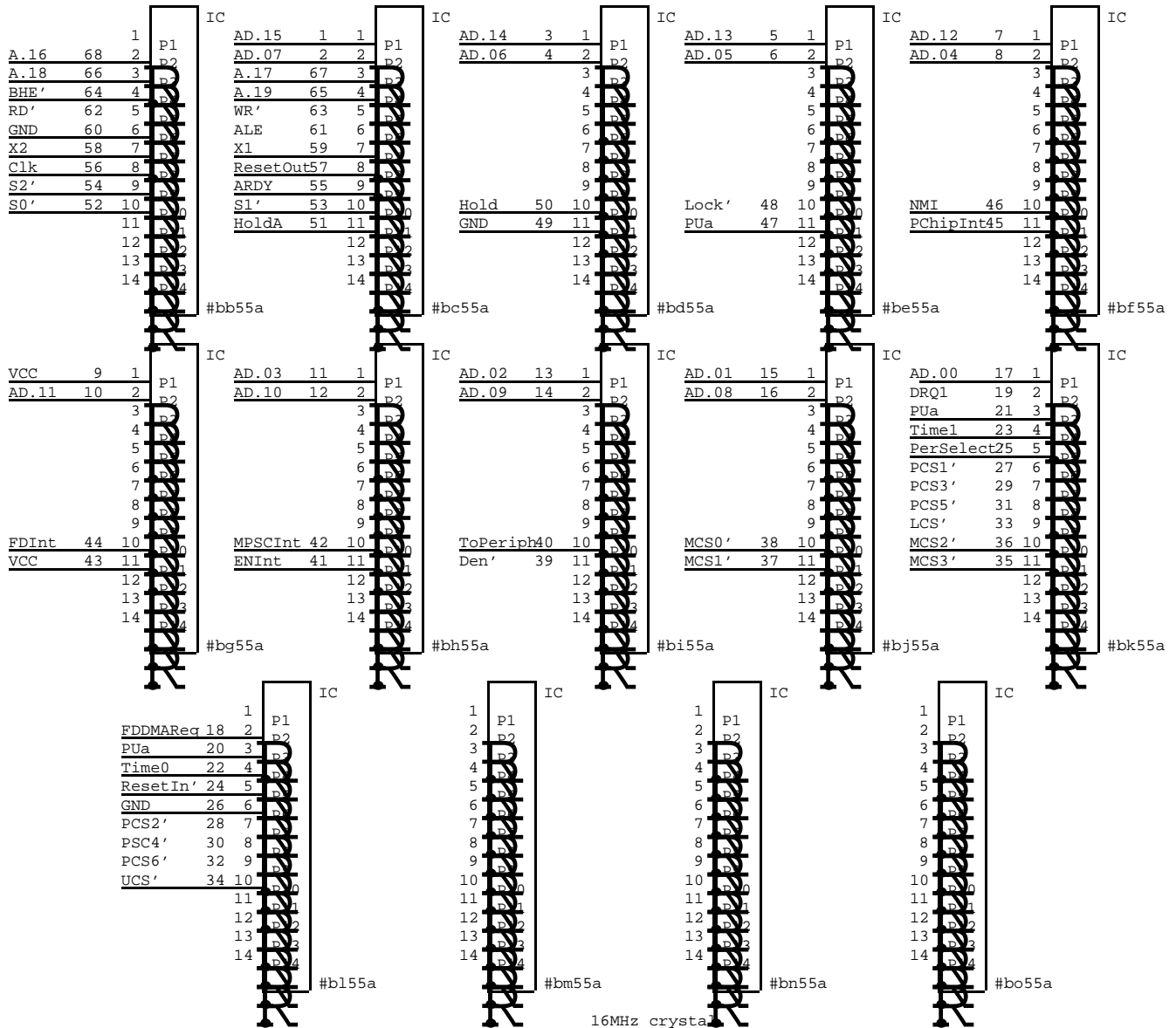
These are really jumpers shown as a switch

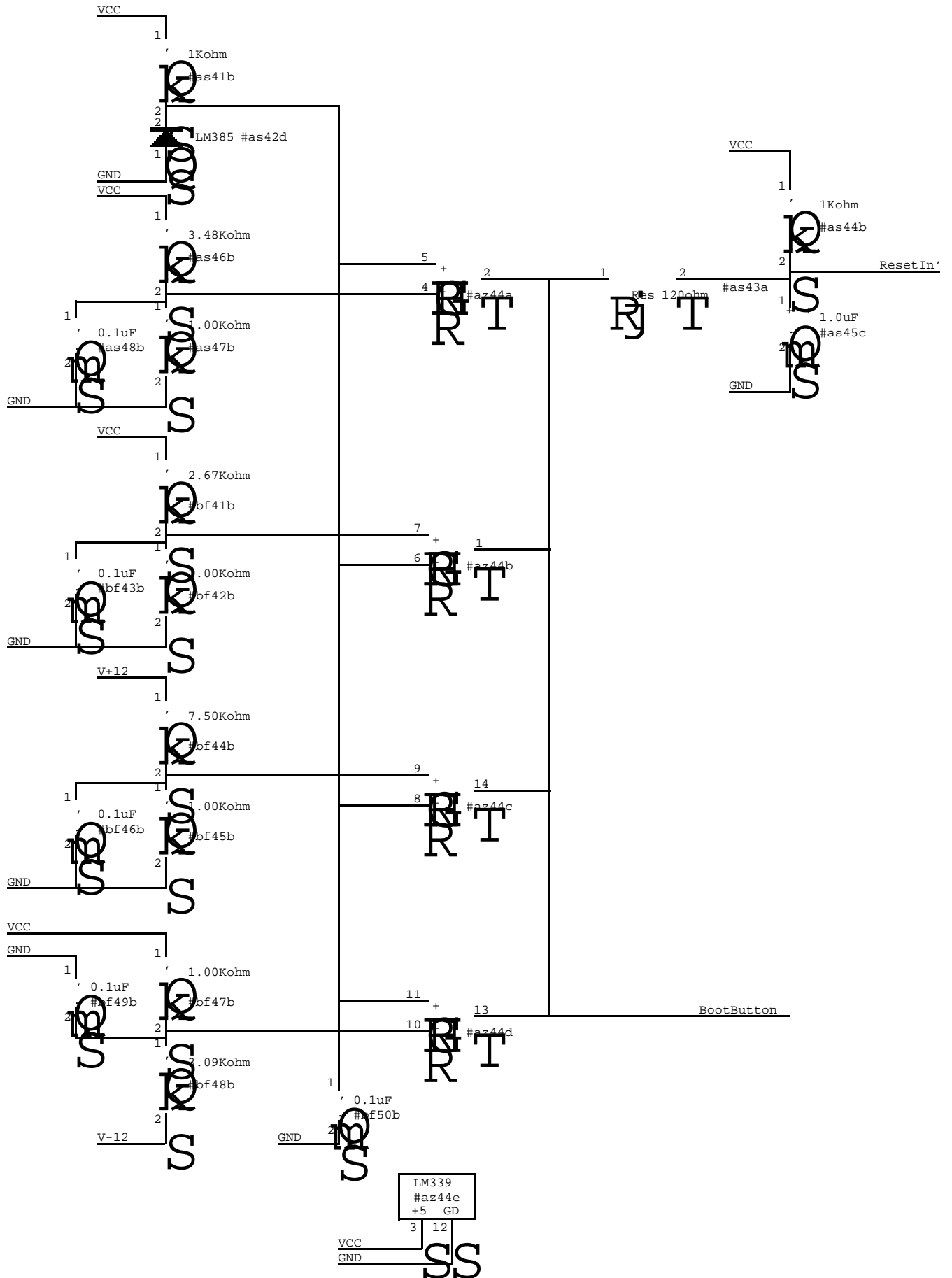


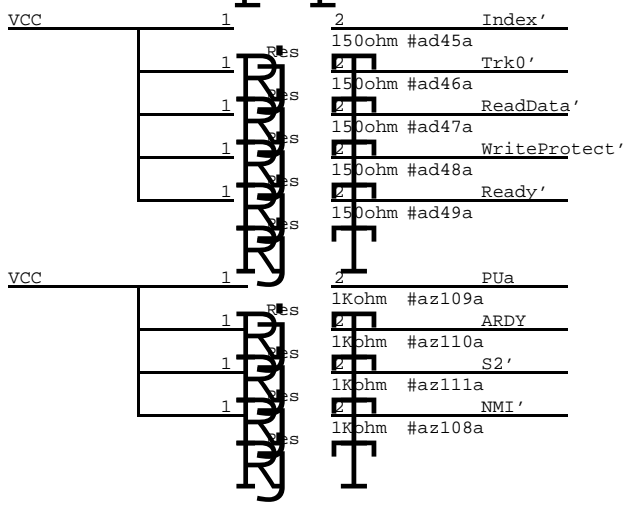
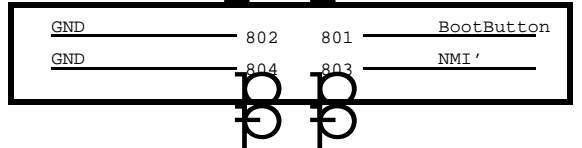
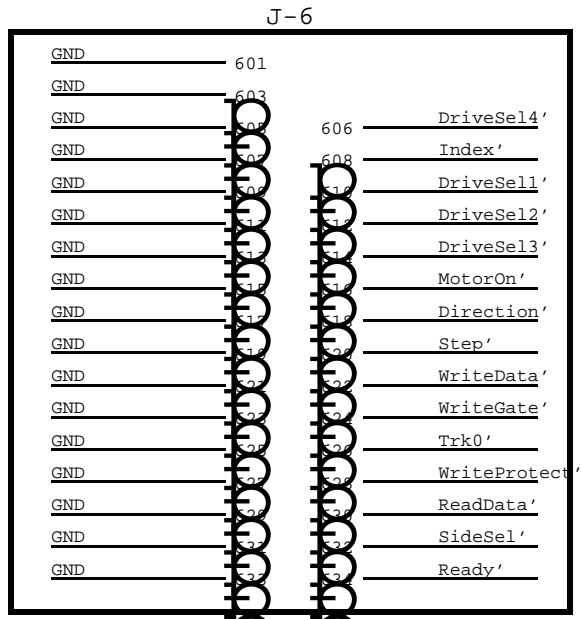
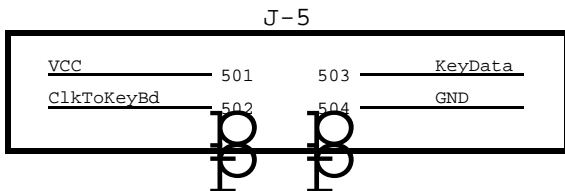
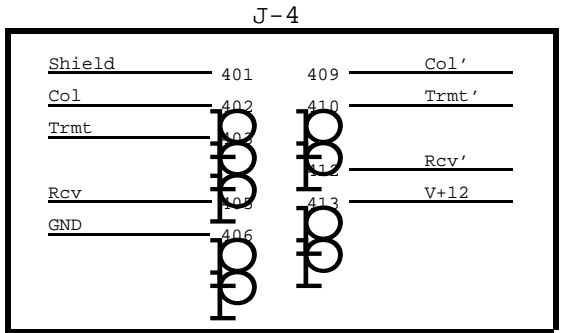
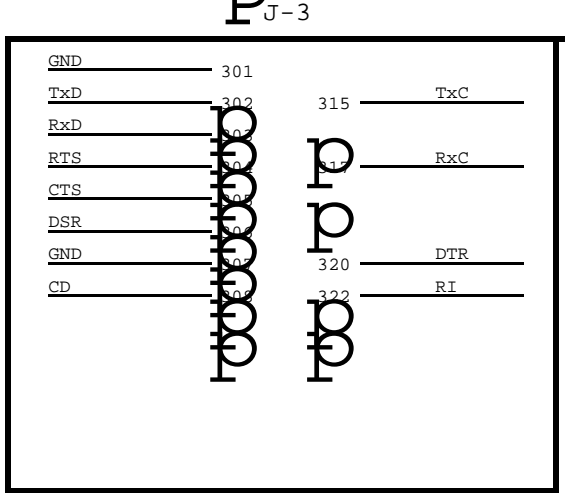
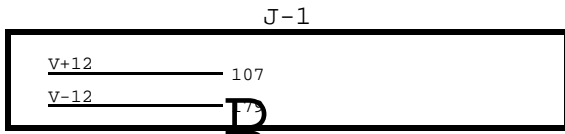


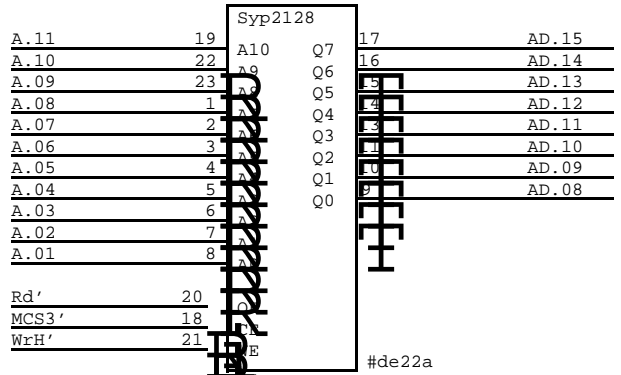
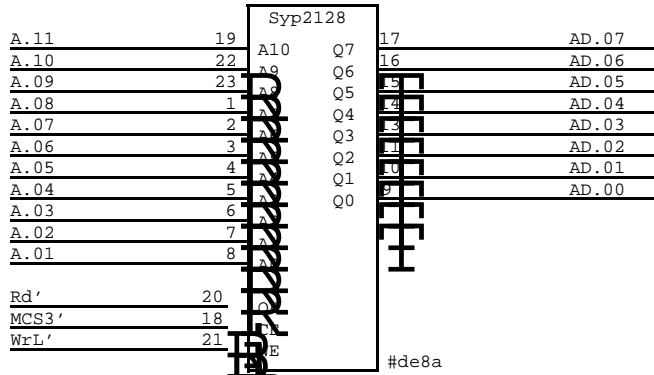
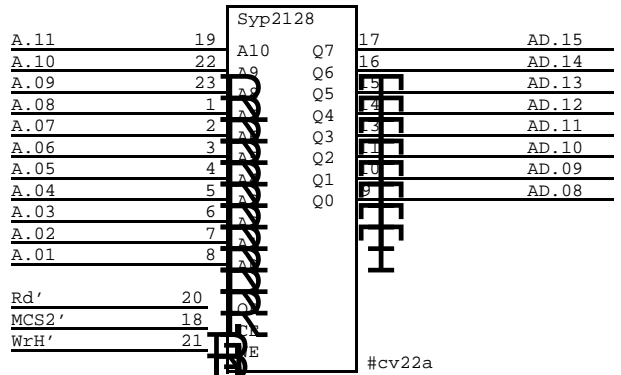
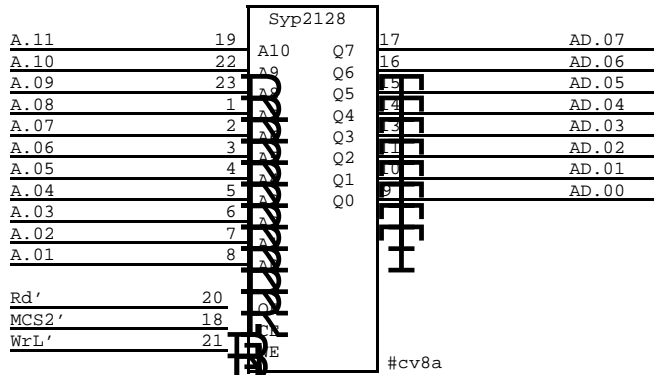
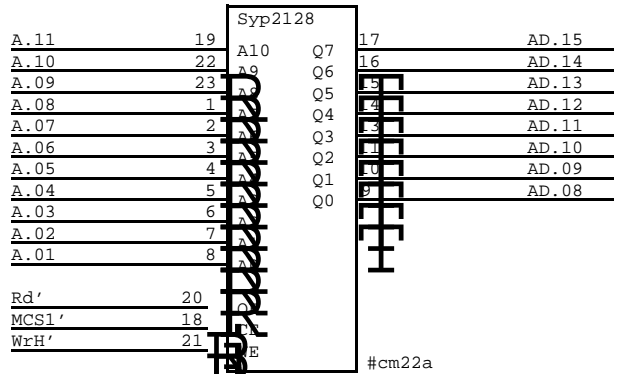
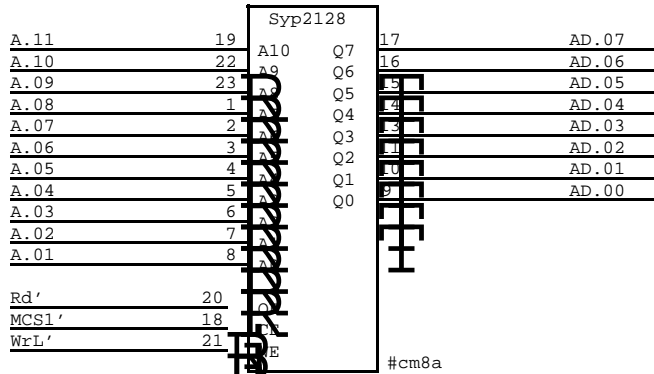
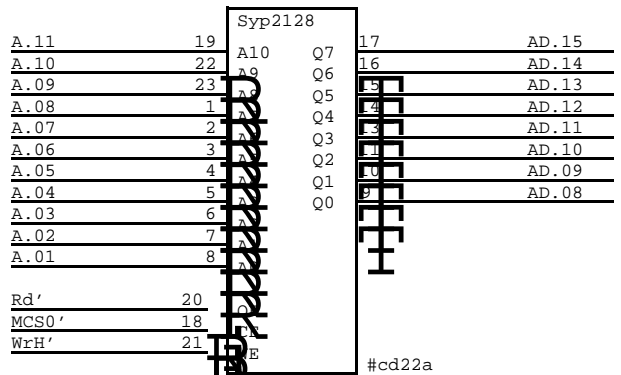
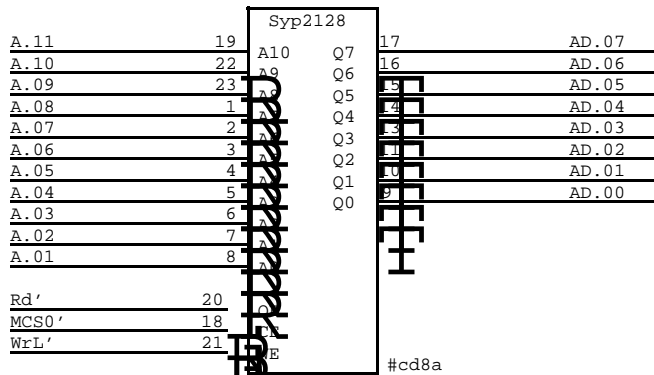
Terminators are on page 9

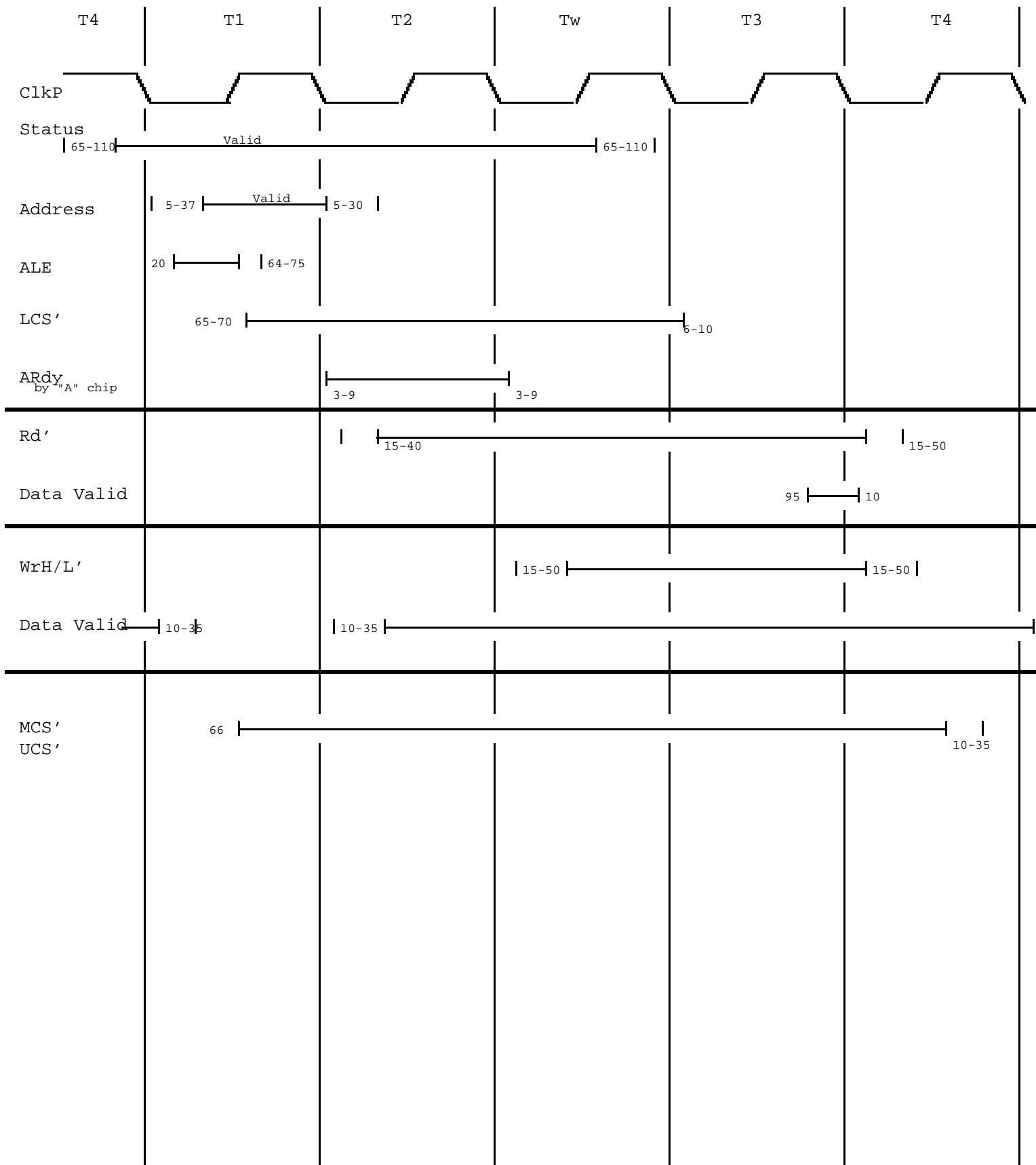










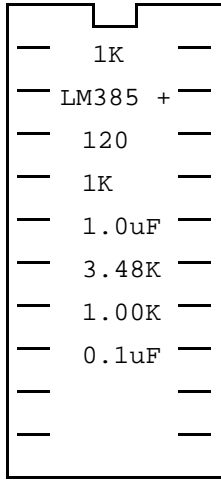


Clk is assumed to be 120ns

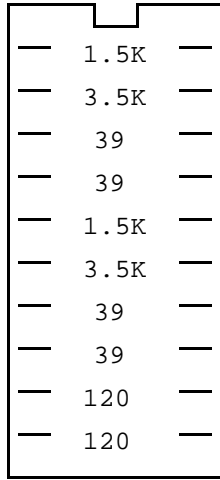
All timing is from falling edge of clk

XEROX PARC	Project Daffodil	Reference Timing	File Daff11.sil	Designer Tim Diebert	Rev E	Date 6/02/83	Page 11
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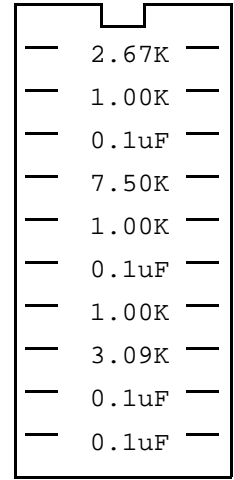
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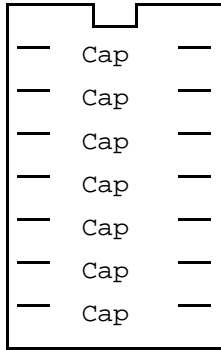
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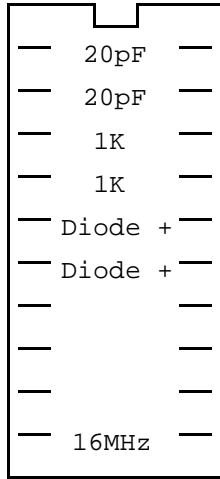
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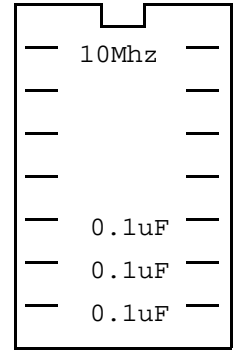
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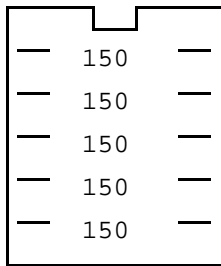
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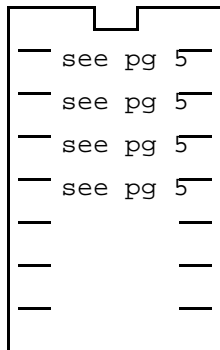
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#ad45



#br41



#az108

