

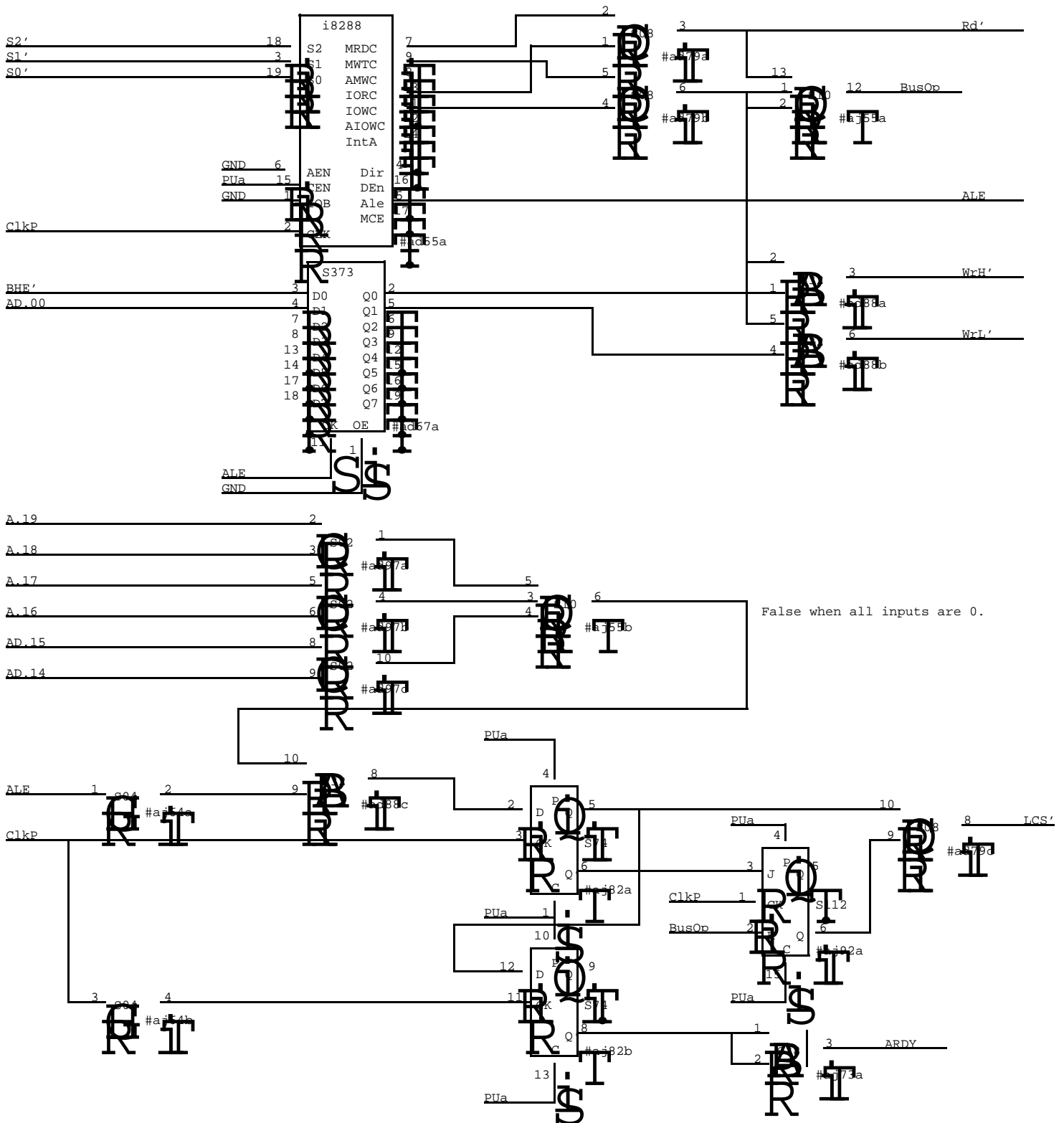
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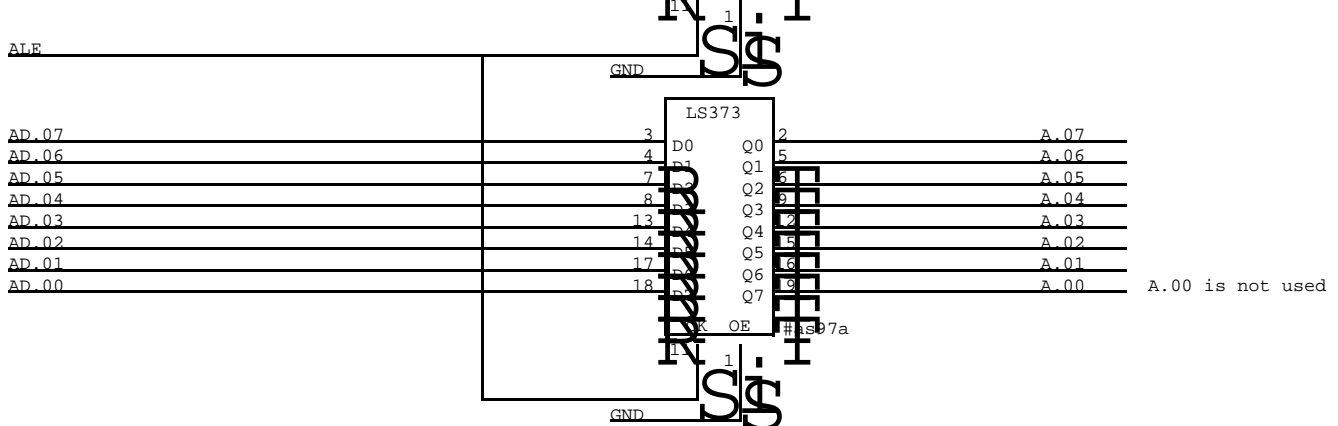
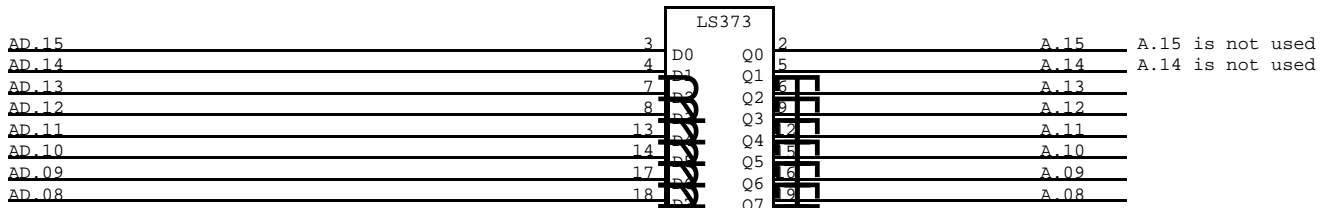
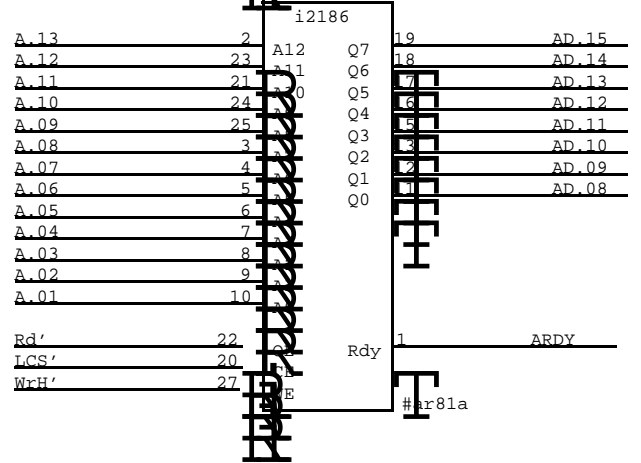
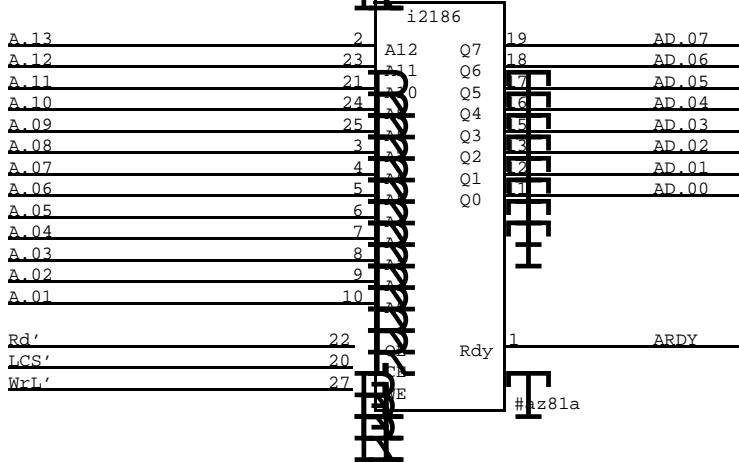
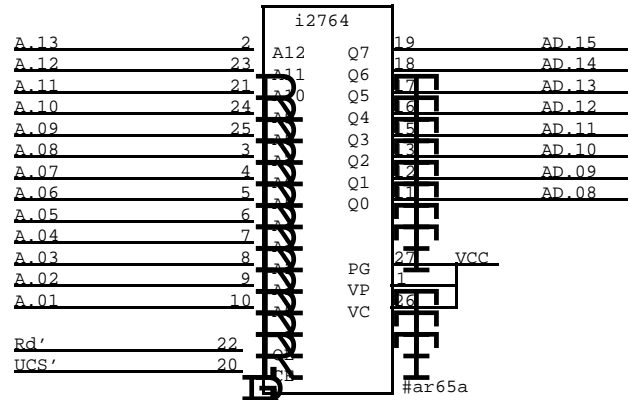
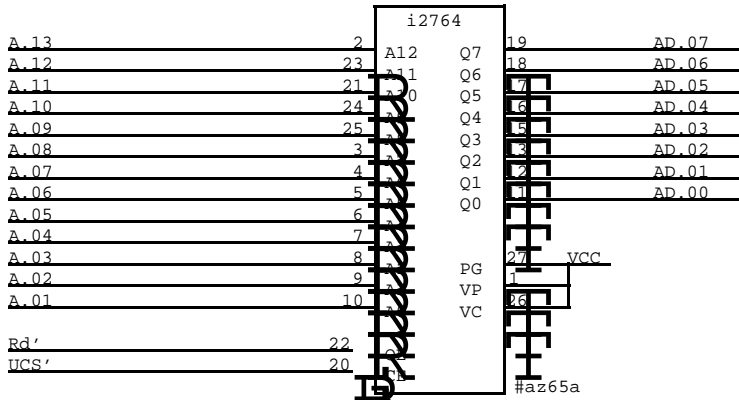
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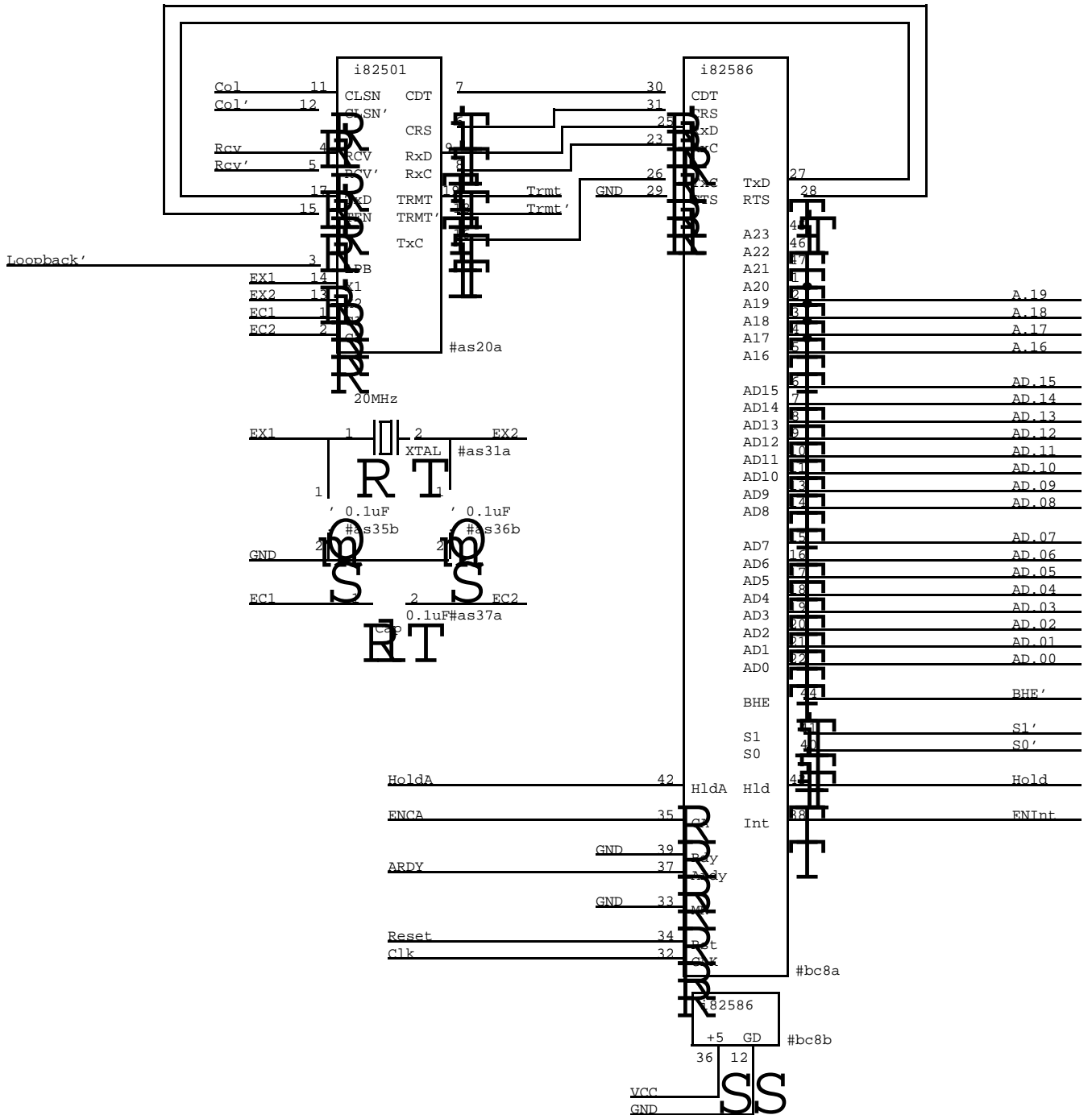
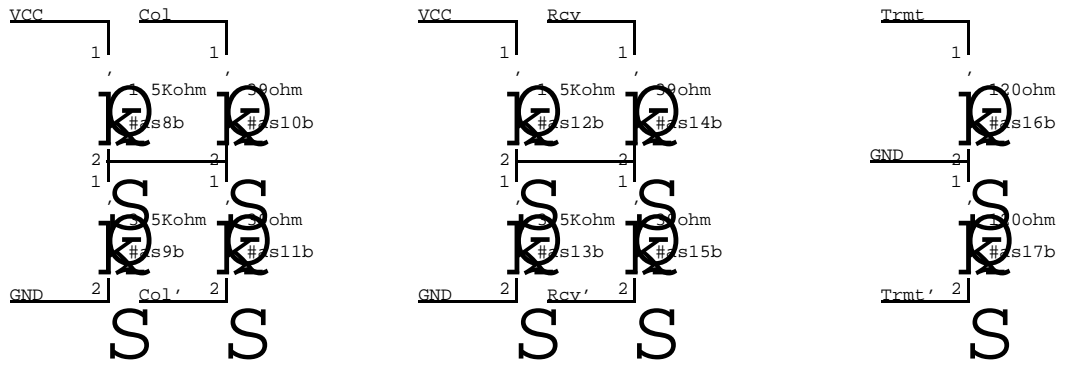
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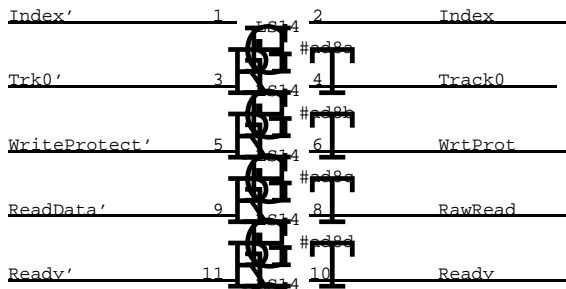
XEROX	Project	Title	File	Designer	Rev	Date	Page
PARC	Daffodil	"A" Chip Logic	Daff01.sil	Tim Diebert	A	8/09/83	01



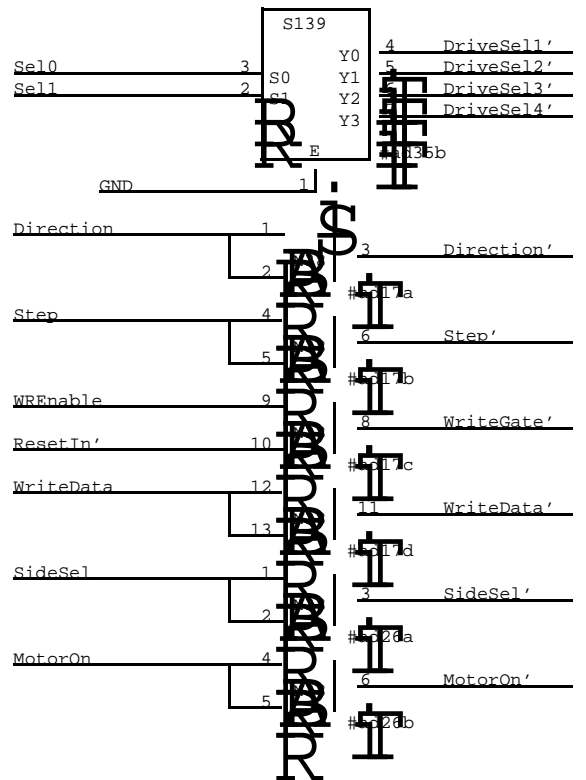
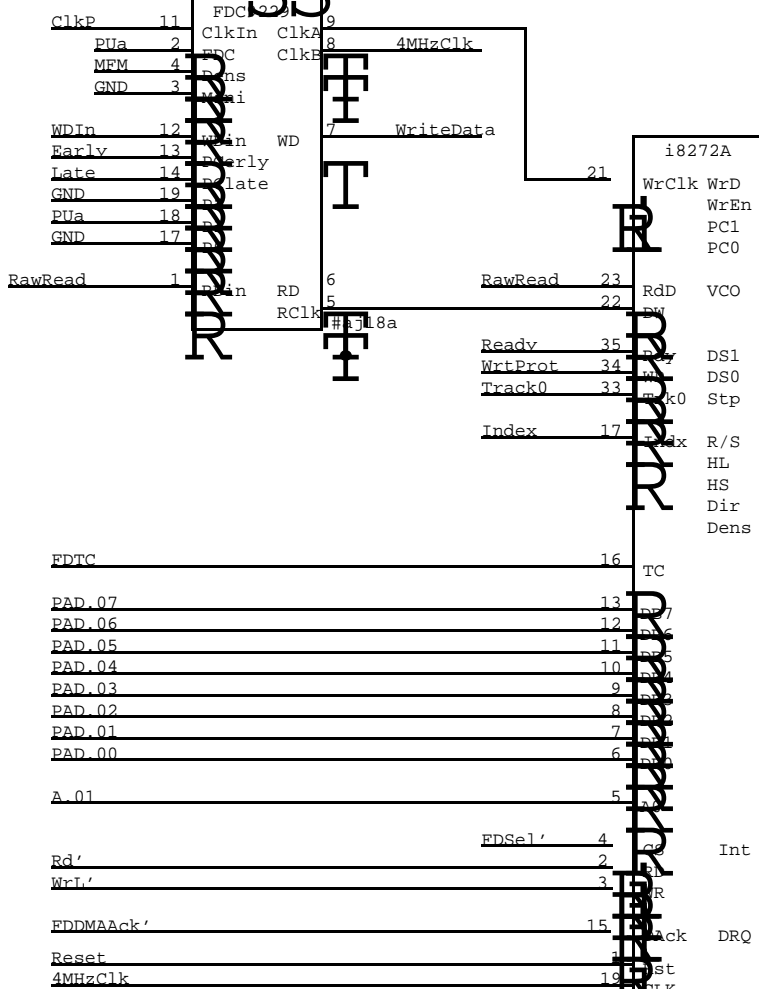
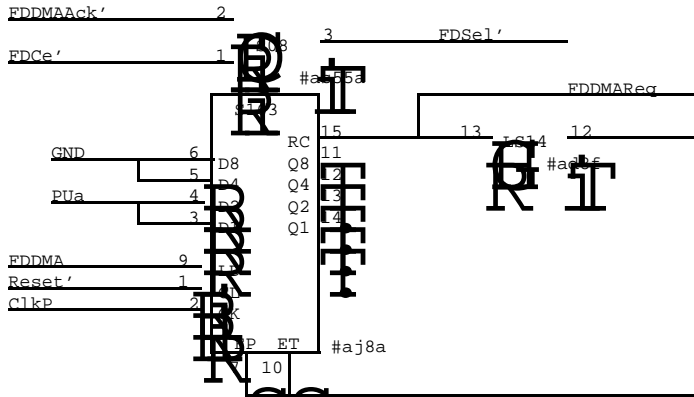


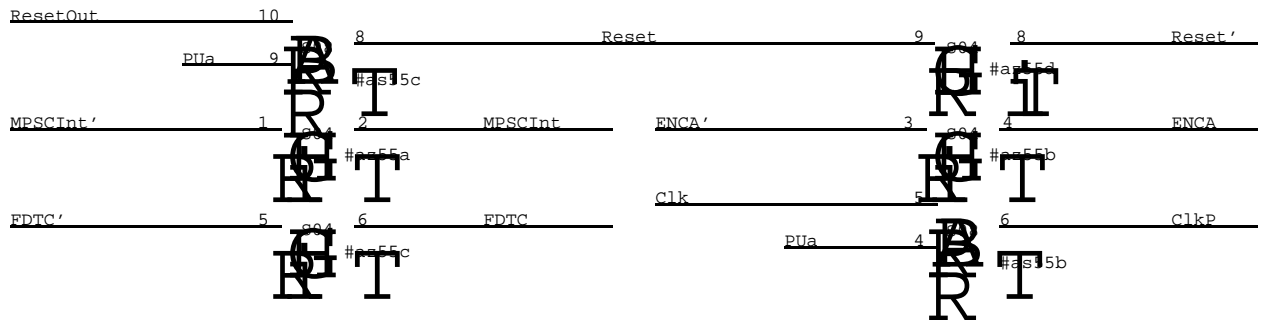
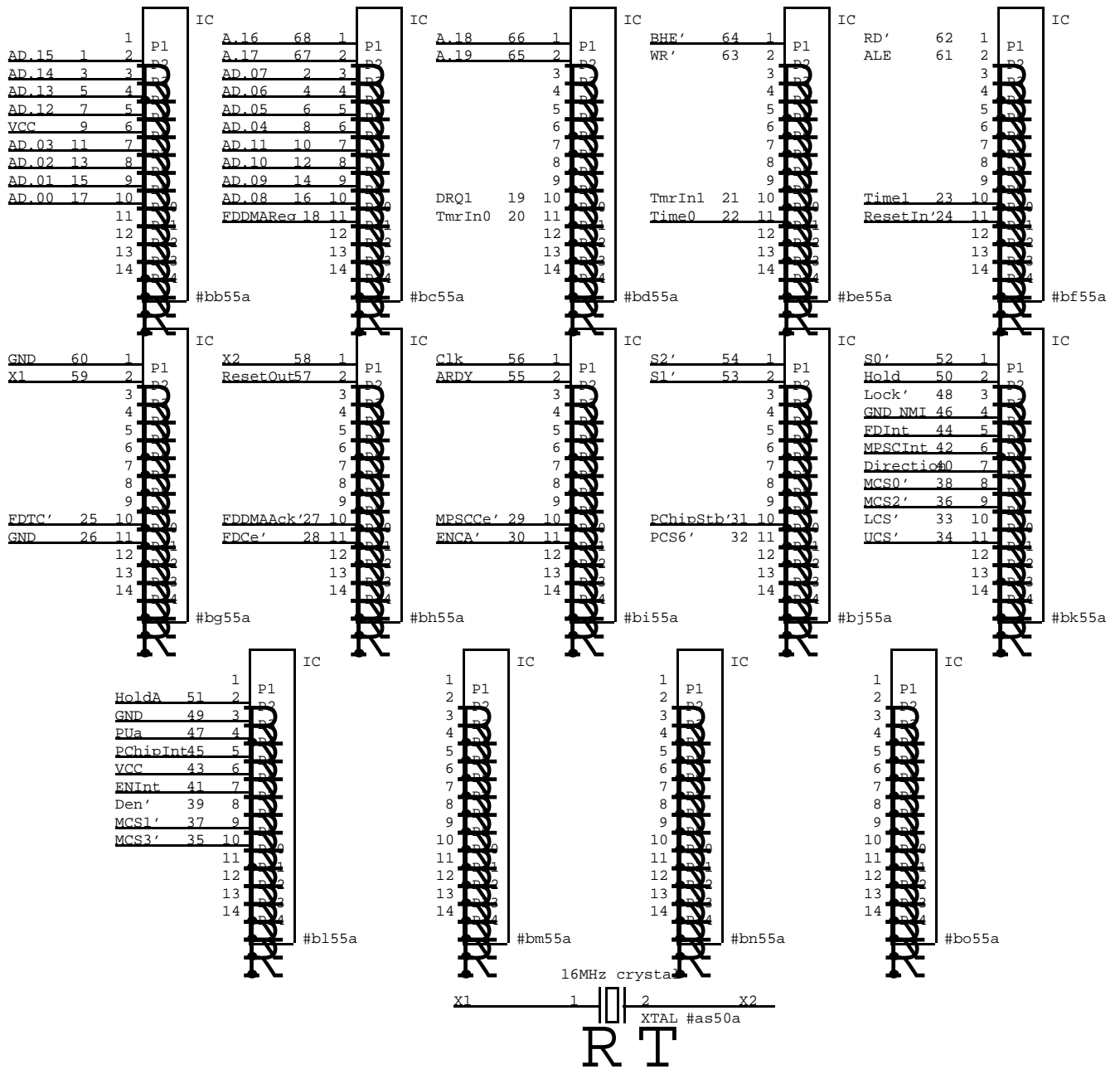




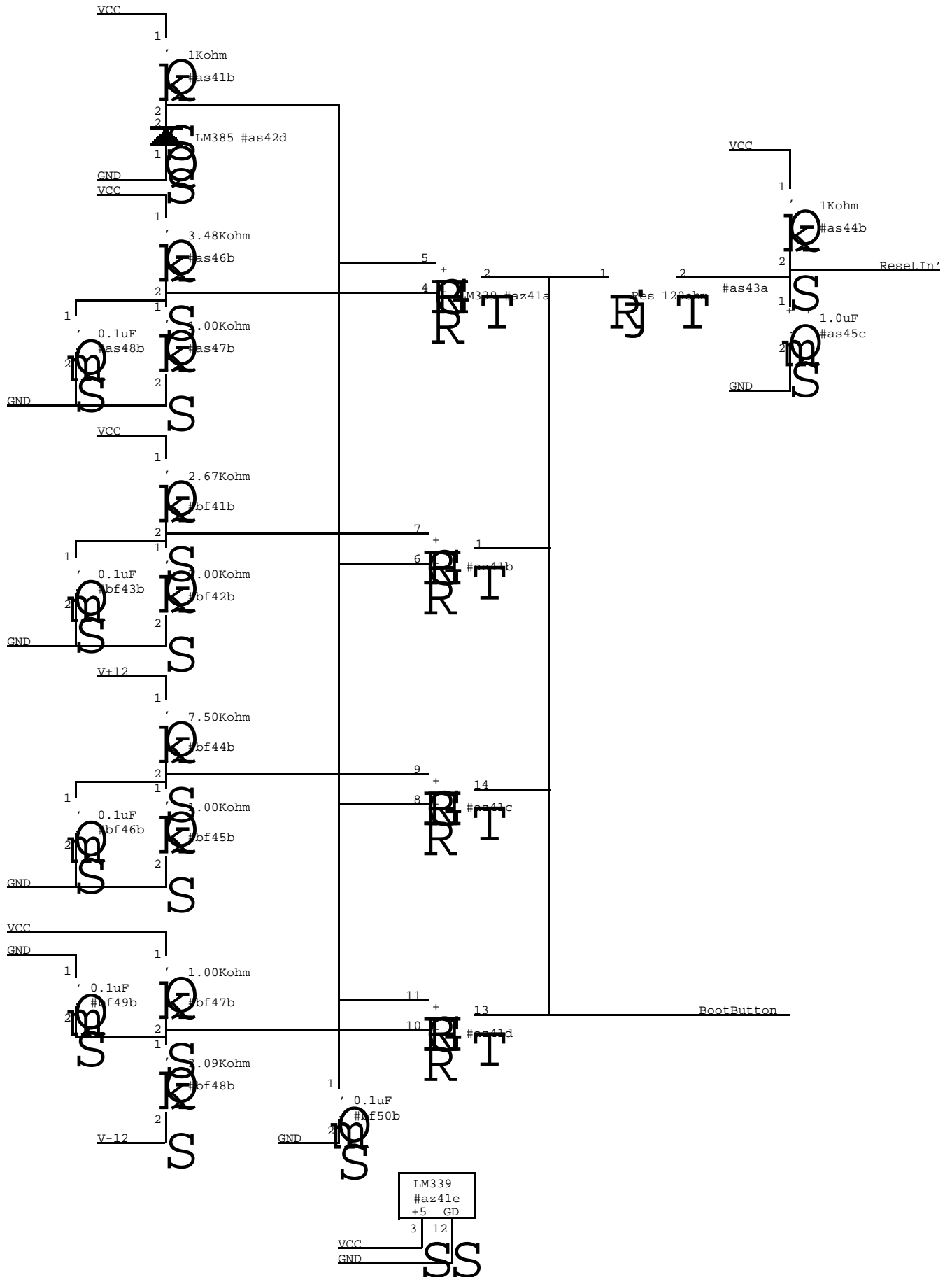


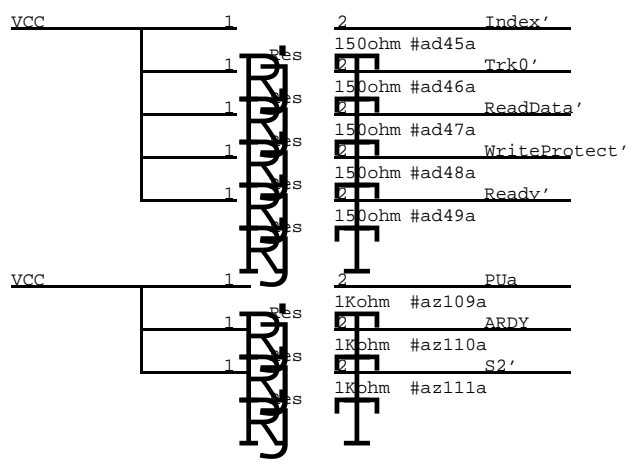
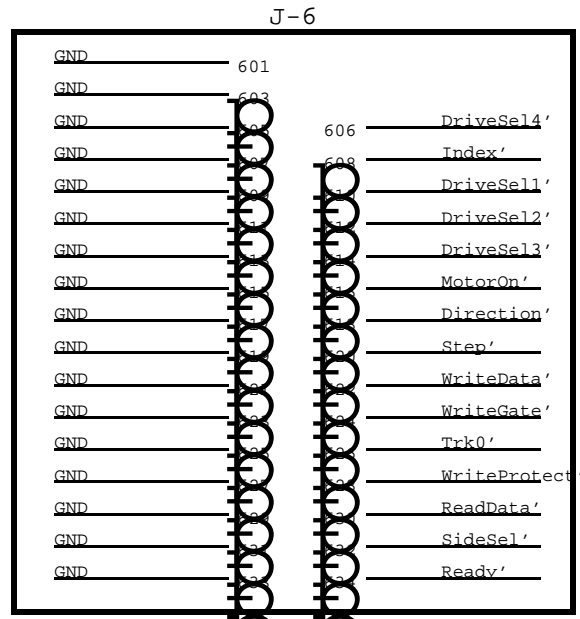
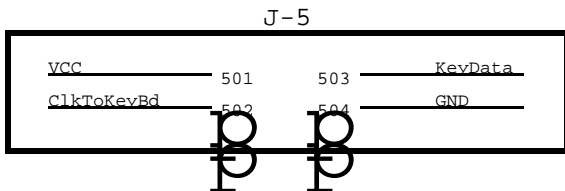
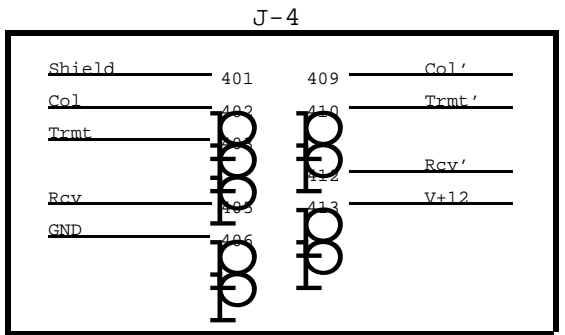
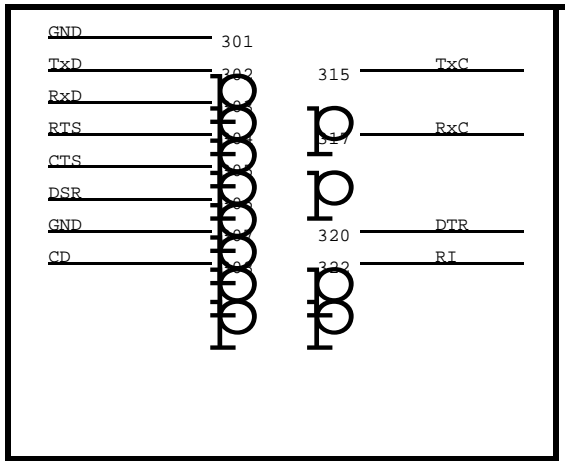
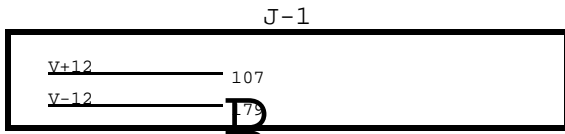
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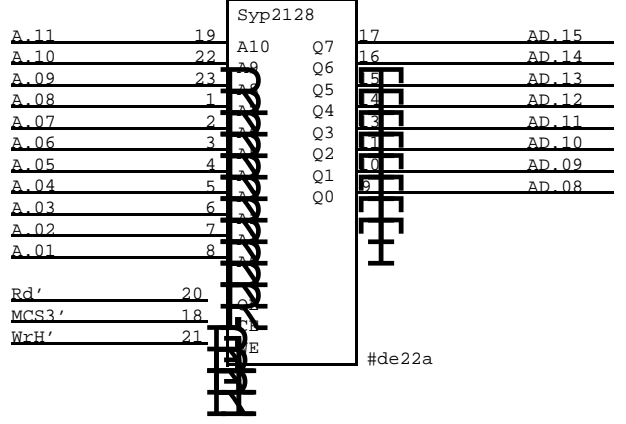
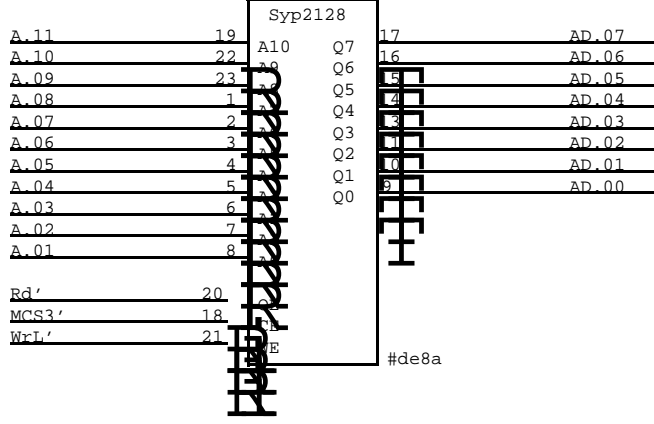
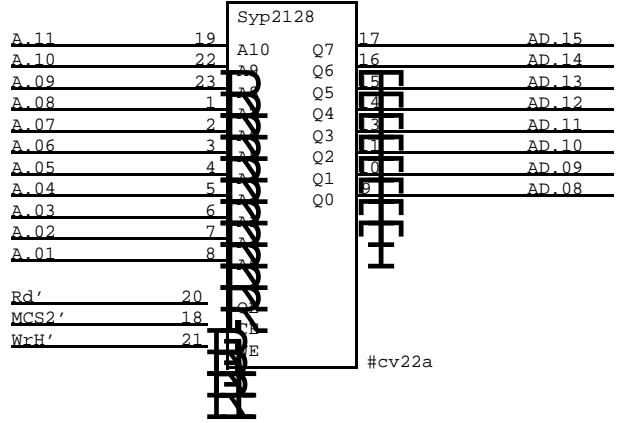
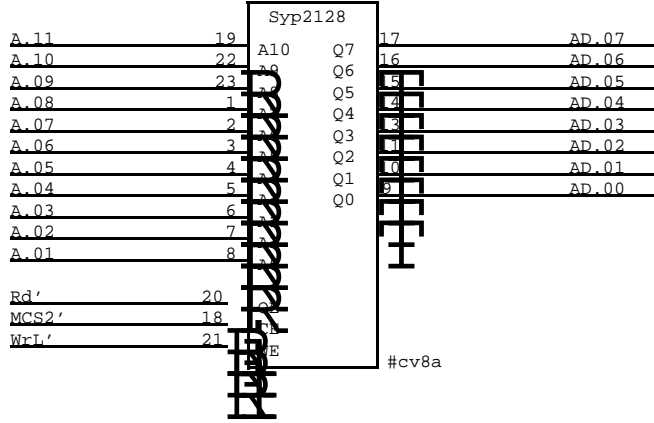
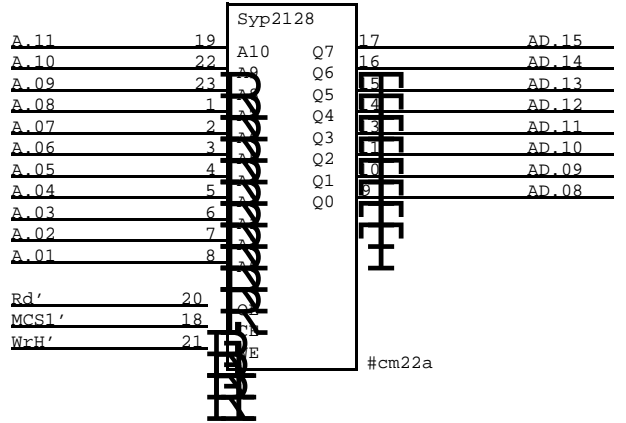
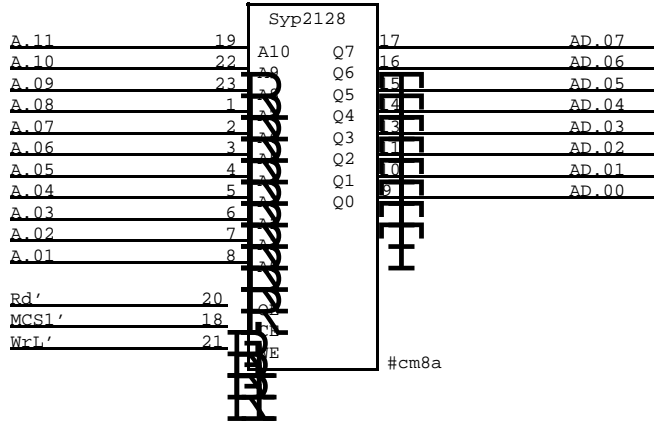
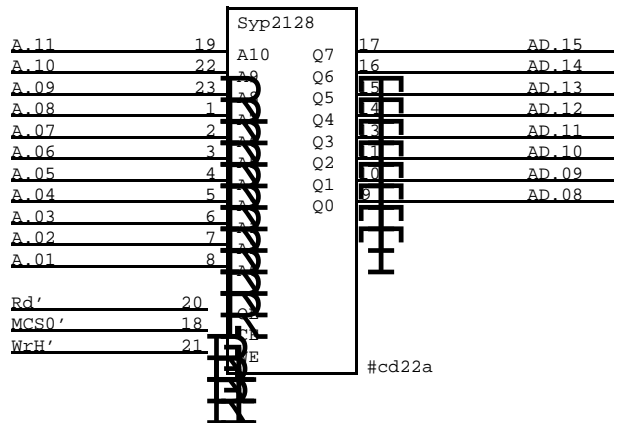
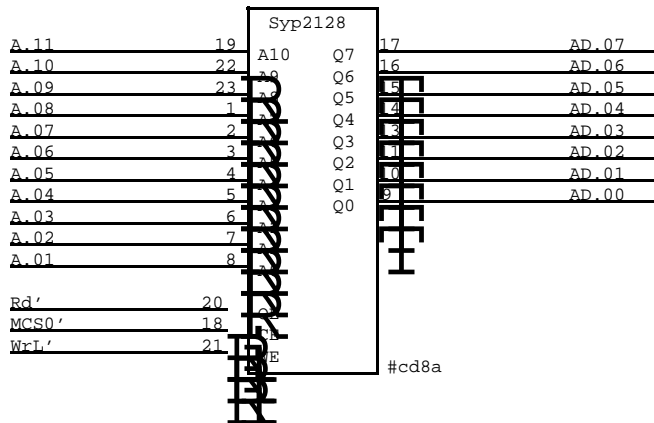


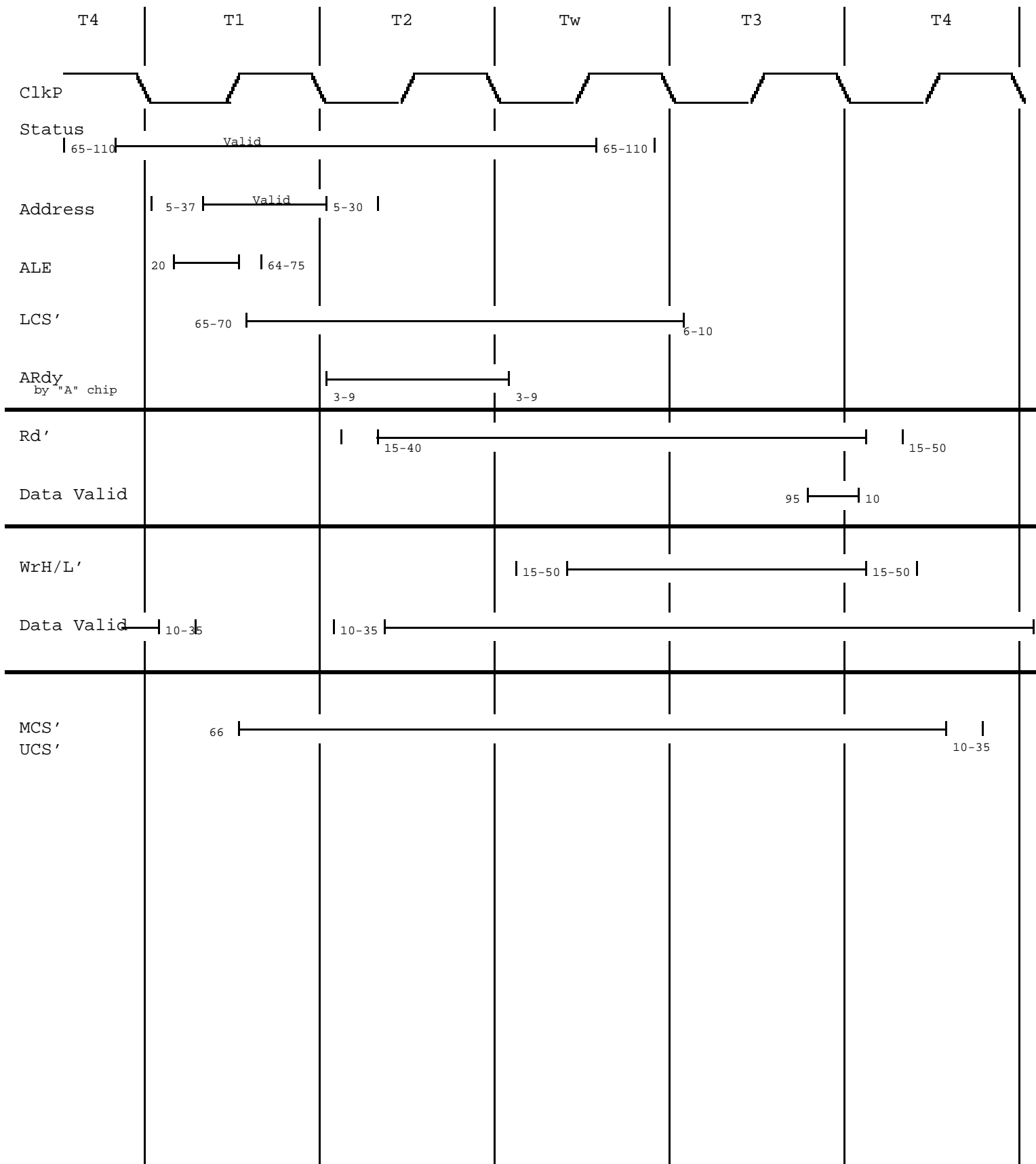












Clk is assumed to be 120ns

All timing is from falling edge of clk

XEROX PARC	Project Daffodil	Reference Timing	File Daff11.sil	Designer Tim Diebert	Rev A	Date 6/02/83	Page 11
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