Gate: a Chipmonk subroutine

The Chipmonk subroutine called GATE will layout a VLSI gate-array like layout from a text specification of the gates involved and their inputs. Inputs (and outputs) are specified by their signal (or node) names. A node name can be any identifier (a string of digits and/or letters, up to 100 characters). Case is ignored.

The circuit specification is read from a text file. In the text file, each gate is represented by one "line" (a line is terminated by <CR> or simicolon). The format of a gate-specifying line is:

<Output Node Name> <Param Spec> : <input Spec> <sep> <input Spec> ... <Line End>

<Output Node Name> is the identifier for the node connected to the Output of the gate. <Param Spec> is optional; if it is present it consists of a decimal number enclosed in parentheses, and specifies the gate parameters (pullup size) for this one gate. If there is no <Param Spec>, the default is used. See "Gate Parameters" below.

The gates which can be used are equivalent to "and-or-invert" gates with an arbitrary number of "NOR" inputs, each of which comes from an "AND" (which may have one or more inputs). Each "AND" may have arbitrarily many inputs (keep it within reason, or the gate widths will get out of hand).

<Input Spec> defines one "AND" and there are as many of them on the line as there are "NOR"s in the gate. The <Input Spec> consists of a single node name for a one-input "AND"; or a series of N node names, enclosed in square brackets, for an N-input "AND".

Node names and <Input Spec>s are seperated by a **<sep>**, which is any collection of spaces and commas. Naturally the collection must be non-null when two identifiers are being seperated.

<Line End> is exactly one carriage-return or semicolon.

Other types of lines:

A comment line is one whose first non-<sep> character is a minus (-). Everything from the minus to the <Line End> is ignored.

The default gate parameter index starts out as 1, but may be changed by a line consisting of a <Param Spec> alone. The default is unchanged by a gate line which specifies the <Param Spec> for that gate.

Examples:

An inverter:

Out1:in1

A two-input Nor:

Out2:in1,in2

A three-input Nand, using gate parameters # 3:

out(3):[in4 in5 in6]

A 2-2-3 and-or-invert:

out4 : [in10,in11][in20 in21] [in30 , in31 in32]

A comment:

- this is a comment

Two inverters and a comment:

o1:i1;o2:i2;-these inverters are silly

Setting a new <Gate Param> default:

(2)

Notes:

Blank lines are ignored. Extra spaces and commas are ignored. Comments must be first (non blank or comma) thing on a line, so if you wish to put a comment after a gate spec, without a carriage return

between, precede the - with a ;.

Parameter Spec Index:

This number specifies a set of parameters used in buiding the gate. The default is 1, which is a set of parameters with a 2-by-2 pullup, and Nor pull-downs which are 8-by-2. (AND pull-downs are wider by the number of AND inputs). Other indexes which are currently defined are: 2 has 4-by-2 pullups and 16-by-2 pull-downs. 3 has 6-by-2 pullups and 24-by-2 pull-downs. 4 has 2-by-4 pullups and 4-by-2 pull-downs. 5 is defined for test purposes but will not work correctly.

Running GATE:

To run GATE (as with any of the subroutines) you type "<CTRL><TAB>;" (semicolon). Chipmonk will prompt to ask for the subroutine name. You type "GATE". After a wait, GATE will ask for the file name. If it hits a problem with the input file, it will put up the message: "File Syntax Error". You respond with <CR> which will abort the GATE run and get you back to Chipmonk. If it has no problem with the file, it creates the circuit as a single cell (sith sub-cells) and puts it at the MARK. When it has finished, it will almost always put up the error message: "Problem running subroutine/ Pages left over". You can ignore this message (type <CR>); it is due to a bug in chipmonk which will be fixed in the next release.

Rather than asking a lot of questions, try it.