

ing IBM-PC or Multibus peripheral also an 1108 with Extended Processor Option (CPE) Initial

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Herring, Ed: 22 Oct 1984
IBM PC - Multi bus-com
patible peripheral

device(s) (not both at once!) can be attached to an 1108 which has the Extended Processor Option (CPE), using Xerox's BusMaster interface option. This document describes the functionality of the BusMaster hardware, and the BUSMASTER software package for controlling it. It is divided into sections: this introduction or sections in general by tetra

nsfers-the BUS functions
microcoded block transfers- the BUSBLT function
directions- overview of direct memory access dma-d
eta i led discussion of the dma process
dma - register model of the BusMaster dma con
trol dma-the BUSDMA functions dma-s summary of si
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accompanying BSMAS

TER software package is somewhat preliminary: While they have been used with IBM PC-compatible peripheral cards, the Multibus alternative has not been fully integrated at this writing. Thus some changes can be expected before the BusMaster interface option is released. In particular, more obscure data may change, the more technical documentation may become more exact, the documentation will be completed. Also, perhaps some peripheral cards will be better packaged, and the problems of access to existing memory will be properly addressed. Note in particular that the hardware documentation is written in a style which is not IBM peripheralware supported, which is false. IBM PC, IPBP C-XT, Intel 8237-5A, and Data Translation DT2801 are proprietary names. Additional hardware required be two

BusMaster and the peripheral devices: an IBM PC or PC-XT expansion chassis mount the peripheral cards, control cards in, and also a PC memory card, mounted in the expansion chassis. The BusMaster connects the PC expansion chassis (the "external bus") to the BusMaster high-speed parallel port of the 1108. The BUSMASTER library package makes use of the BUSMASTER software environment, PC peripheral

peripheral software to this augmented 1108 system just as they would in an IBM PC Master program. The peripheral cards are in the same way as they would be done in BASIC on an IBM PC: "peek and poke" - that is, explicitly programmed transfer of individual bytes from and to individual I/O and memory addresses. The rest of the software is a set of routines for programming techniques: 1) In interrupts: In interrupts are not as yet supported. More precisely, while the hardware does support interrupts, exactly as on an IBM PC, the 1108 microcoded software does not yet support interrupt service. 2) Direct memory access: PC peripherals can be accessed (dma) to the internal memory of the 1108. However, the peripheral can be accessed from PC memory mounted in the PC expansion chassis, and the 1108 can simultaneously access that memory, either with peeks & pokes or with microcoded high-speed block transfer instructions. Other examples of programs

In BASIC, not in volving interrupt service, can be translated immediately to Interrupt Disables. We have also implemented several applications on the same technique, with two different peripheral devices, the Data Translation DT2801 Analog & Digital I/O System and the Tecmar-like 640x400x4-bit color board. One of four applications has the data acquisition board sampling acoustic data

the data (including FFTs) and graphs their results, continuing in real time. This application uses quite sophisticated data acquisition techniques: hardware expansion chassis, while the program in the 1108 continuously reads & processes data from the circular buffer. This is possible because (1) the PC's microcontroller (which is functionally duplicated in the BUSMASTER) can be programmed to read data from the circular buffer continuously without intervention, (2) the data points can be read by the software program, and (3) data transfer from the PC memory to the 1108 does not interfere with the hardware device. This data transfer is done through the data bus using the BUSMASTER software. Our reference function is for the data transfer available as the LISPLibrary Package PCDA. This is one example of how to use the BUSMASTER package. Single-byte transfers to/from

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ions Notethat whenever you power-up or BUS RESET, you then have total

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initialization of memory refresh parameters, before returning memory on the external bus can be expected to hold data. (BUSRESET)--acts like a power-up: reset the BUSMASTER and assert the RESET signal along the external bus, the

causing every device there to reset itself as a power-up. BUSDMINIT will then have to be called again if the hardware control of memory refresh parameters is needed. (BUSINPUT/oa address) => 8-bit value - input byte from external bus; busi/oa address, returning it

as a small non-negative integer. (BUSOUTPUT/oa address 8-bit value)--output byte (the least significant 8 bits of the integer argument)

ent) to an external bus memory address (BUS.READ memory address) => 8-bit value--read a byte from external bus memory, returning it as a small non-negative integer.

negative integer. (BUS.READ HLMemory address) => 8-bit value--read a byte from external bus memory, returning it as a small non-negative integer.

small non-negative integer. memaddr is the less significant 16 bits of the memory address; memaddr is the more significant bits of the address. (BUS.WRITE memory address 8-bit value)--write a byte (the least significant 8 bits of the integer argument)

external bus memory (BUS.WRITE HLMemory address) --write a byte (the least significant 8 bits of the integer argument)

ent) to external bus memory. memaddr is the less significant 16 bits of the memory address; memaddr is the more significant bits of the address. Micro-coded block transfer to/from the external bus--the BUSBLT functions. These functions transfer data between

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an array in Interlisp-D virtual memory and a consecutive region in the memory

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on the external bus. Note that BUSDMA.NI has been called at least once, to initialize the memory refresh apparatus, before returning memory

the external bus can be expected to hold data. (BUS.BYTES array starting index bus address element to external memory)--transfer every byte of elements

elements of the array in Interlisp-D memory, starting with the starting index of the element, to or from consecutive byte addresses on the external bus, starting at bus address. array must be an array of integers, WORDS(=SMALLPOS) or FIXPs. If the array is of WORDS or FIXPs, then the more significant bits of each Interlisp-D word is transferred to the lower address of the external bus.

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troller. This view of the hardware controller is basic, and a simplified version of that in the specifications for the Intel 8237-5A, on which this system is based. DMA - direct memory access - is discussed in the

dma process Typical dma operation in the bus

The master is quite easy to program -- you are only dealing with one I/O device and in only one way. Even parallel bus systems are no exception. The device is not too bad if you're not going to be too picky. Unfortunately, I/O devices differ in major and minor ways, the bus master is designed to be flexible, and this is discussed in the next section. My hope is that a few of the examples in the Summary section below will help you understand some of the questions, which can only be answered by skimming a rough draft. (If you are planning exotic things, you may need to read the specifications for the Intel 8237-5A DMA controller chip, on which the bus master is based, and the Technical Notes section below.) The dma controller and memory refresh

the hardware has been initialized before any dma can take place and before the memory in the PC expansion chassis is initialized. This is done with the BUSMA.INIT function (though under some circumstances you may see the BUS.RESET function in the documentation). BUSDMA.INIT can be called a gain at any time, with the side effect of disabling (masking) all dma channels. The dma controller has a refresh rate

of 1/3 of the bus channels, numbered 1 to 3. (There is actually a fourth channel, numbered 0, dedicated to the memory refresh apparatus.) Each I/O device that does dma has to know where to find the dma channel number, as does the software controller. Usually a device's interface card has a jumper which determines which dma channel it will use. Only one device can be using any one

channel at a time. The hardware can be made to do dma at any time. The dma channel is a register in the dma controller. Within the dma operations

"A single dma operation" is: the program gets the I/O device address channels set up for the operation; many bytes are transferred at a time at the initiation of the I/O device but under the control of the channel; the transfer is done in a few cycles, either the channel, the I/O device, and/or the program; finally the program transfers the I/O device and the channel. Also, during the time when individual bytes are transferred by the I/O device and the channel, the program might intervene temporarily to suspend and then resume the operation. It is important to note that the dma controller itself does not actually distinguish between "suspended" and "terminated": if the program resumes the operation then it was "suspended"; if it sets up a new operation then the "old news" terminated! These two operations depend on

the device. Setting up the dma channel involves setting up address, transfer count, and mode registers. It would be premature to discuss the setup further here, as we have not yet motivated the issues. Rather we will discuss everything else, including the function of the channel registers, then discuss setup in the Summary section. During the execution of dma operation

"individual bytes transferred" are required by the I/O device involved. If more than one device requests dma at the same time, the dma controller services the lower-numbered channel first. The direction of the transfer (to or from memory) has to have been set up before the I/O device and the dma channel. The memory address to/from which the

transfer will take place is determined by the dma channel. Normally it uses successive memory addresses, and in "Auto-initialization Mode", the channel will wrap the addresses around a circular buffer (wrapping in either direction). For exactly how addresses are generated, see the discussion in the next page, current address, and as a address registers below in the Register Model section. DMA on a particular channel can be

suspended and resumed by "masking" and "unmasking" the channel. A masked channel refuses to honor any dma transfer requests. If there is a dma transfer request still pending when the channel becomes masked, the channel will service the request when. Obviously, data can be lost by keeping the dma channel masked too long while the I/O device is requesting transfers. It remains to be discussed how dma operates

terminates. This is potentially rather complicated.

itself because use its transfer counter; or the channel mask is used by the program. In either case, the channel is

self does not distinguish between "suspended" and "terminated". I will try to say why it does so: At a given point, a channel is either in a state where it is not masked, or it is masked. If it is not masked, it will accept requests for transfer, and the transfer counter will be incremented. If it is masked, it will not accept requests for transfer, and the transfer counter will not be incremented. If the transfer counter reaches zero, then the channel is unmasked. If the transfer counter reaches a value greater than zero, then the channel is masked. The channel is masked if the transfer counter is greater than zero, or if the channel is in a state where it is masked. The channel is unmasked if the transfer counter is zero, or if the channel is in a state where it is not masked. The channel is masked if the transfer counter is greater than zero, or if the channel is in a state where it is masked. The channel is unmasked if the transfer counter is zero, or if the channel is in a state where it is not masked.

est dmtransfer for any of the reasons, including: it is slow transfer counter, which is not; it has detected an error condition; it has detected the TC signal from the channel on the external bus; it has detected some other termination condition; or it has been disabled by the program. Any particular device may allow support for these conditions. The channel can not directly be disabled by the device; it has ceased requesting transfers; it simply responds to them if and as they arise. Typically the program determines that the device considers the transfer operation done. The program might mask the channel.

temporarily, for some kind of housekeeping reason, or it may do so as part of the termination operation. It can have any of the reasons for doing this. The channel does not care if the program chooses to mask it or not. The channel is masked, that's fine; otherwise, when the channel becomes unmasked, it will keep on from where it was. Changing a channel's parameters while it is unmasked is risky and should be avoided. Direct memory access -- register

model of the Bus Master DMA controller in our model of the mac controller,

the real global registers, and each channel has a set of seven registers: Page register - S upplier esthemores

ignificant bits

of the external bus memory addresses generated by the channel. The contents of this register are concatenated to the left of the current address register when an address is generated. Unfortunately, incrementing the address register does not affect its page registers. (This simplifies that any operation must take place entirely within one (64KB-aligned) 64KB page since the current address register is 16 bits wide. Further, a buffer that has a 64KB page boundary will really wrap around within the 64KB page it starts in. The page registers are set up by the program, but cannot be read by it. Current address register -- Holds

the less significant bits

the external bus memory addresses generated by the channel, that is, the 16-bit address within a page. The channel generates addresses by concatenating its page register on the left of the current address register.

annel increments or decrements the current address register by one. The direction depends on the channel's mode register. Unfortunately, this increment or decrement does not affect the program register (as discussed above). The current address register is

set up by the program, incremented or decremented by the channel, and, in "Autoinitialization Mode", reloads by the channel from its base address register when it runs down. The current address register can be read by the program, so that the program can keep track of the external bus memory synchronization with the external bus. Base address register--In Auto

initialization Mode, hold

is the starting address of the circular buffer. That is, in Autoinitialization Mode, when a channel's current transfer count register runs down, the channel reinitializes its current address register. The base address register is loaded

automatically whenever the program sets up the current address register. There is no BUS DMA function for loading the base address register. Current transfer count register

er--Control the length of the dma operation

ration (of the Autoinitialization Mode, the length of the circular buffer). That is, after each data transfer, the channel decrements its current transfer count register, and if it goes to zero, then a TCS signal is asserted to the external bus and the channel is masked (if not Autoinitialization Mode) or the current address and transfer count registers are reinitialized from the base address (if Autoinitialization Mode). Note that the current transfer

count register contains the number of bytes transferred since it was last done, a 16-bit number. Not only that, when the current transfer count register's value is zero, viewed as after a data transfer, means "done", the same zero value is viewed as before a data transfer, means 64 K. Thus the maximum transfer (of circular buffers) is 64 Kbytes. (You may also know that the

hardware registers always use the same address, that is, we've described the module 64 K. The BUS DMA functions maintain the translation.) The current transfer count register

is set up by the program, decremented by the channel, and, in Autoinitialization Mode, reloads by the channel from its base transfer count register when it runs down. The current transfer count register can be read by the program, so that the program can synchronize it with the external bus memory access switch the external bus dma. Base transfer count register--

-In Autoinitialization Mode, hold

is the initial value of the current transfer count register. That is, in Autoinitialization Mode, when a channel's current transfer count register runs down, the channel reinitializes it from its base transfer count register. The base transfer count register

is loaded automatically whenever the program sets up the current transfer count register. There is no BUS DMA function for loading the base transfer count register. Mode register--Contains some

intro bits. The

mode register is set up by the program, but cannot be read by it. write memory?--det er mine sw het her dma transfer sare from the i/odevice to memory or vice versa. autoinit?--gover ns Autoinitialization Mode. If false, the current transfer count register should be set up with the length of the transfer, and when it runs down the channel mask itself. If true, the current transfer count register should be set up with the length of the circular buffer in external bus memory, and, when it runs down, the channel reloads the current address and current transfer count registers from the base address and base transfer count registers, thus wrapping around the circular buffer. deca ddr?-- det er mine sw het

current address register is incremented or decremented as it reaches the transfered. Mask kbit--When the channel's mask

bits set

the channel is set to "masked", dma on the channel is suspended in that the channel will ignore requests for dma transfer from the i/odevice. No that if a i/odevice request

is made while the channel is masked, and is still asserting that request, then the channel becomes unmasked, the channel will service the request at that time. Thus data can be lost while a channel is masked or will be lost if the channel is masked for a significant time. The speed of the i/odevice.

hence the dma controller is (re)initialized, including a power-up. They can be forced by the program. A channel sets its mask bit when the current transfer count runs down, except in autoinitialization mode. The program cannot read the mask bits. TCbit - Whether the channel's

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transfer -count register has run down since the last time either the dma controller was (re)initialized, including a power-up or **BUS DMA TC BIT** explicitly used to reset this bit. Direct memory access-- the **BUS DMA**

Functions See the Register Models section above

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 of operation is not heard from the functions and of the register reference to bytes. These functions do not check the

argument except as specified. **(BUS DMA INT)**--(re)initialized

dma controller and memory refresh circuitry. Mask channels 1, 2 and 3, and clear their TC bits. **(BUS DMA A.S ETMOE channel write memory**

autoinit? **decade** (dr?)--set the mode register for the channel. **(BUS DMA SET PAGE channel** bits of address

address)--write to the page register for the channel. Check that channels 1-3. **(BUS DMA A.S ETMOE channel write 16 bits of**

address)--write to the base & current address register for the channel. The channel must be masked when this function is called-- this is the caller's responsibility. **(BUS DMA READ ADDRESS channel)=>low 16 bits**

of address--read the current address register for the channel. The channel must be masked when this function is called-- this is the caller's responsibility. **(BUS DMA SET ONT channel n bytes)--write**

both the base & current transfer count registers for the channel. Check that n bytes is in the range 1-65536. The channel must be masked when this function is called-- this is the caller's responsibility. **(BUS DMA READ ONT channel)=>n bytes--read**

current transfer-count register for the channel. Note that the value 65536 is returned as the function will only be evaluated when the channel must be masked when this function is called-- this is the caller's responsibility. **(BUS DMA MASK channel)--set the mask bit for the channel**

channel, disabling dma on the channel. **(BUS DMA MASK channel)--clear the mask bit for the channel**

channel, enabling dma on the channel. **(BUS DMA READ TC BIT channel clear the bit ?)** => the channel

TC bit, as **TOR NIL**. A socket is the bit if requested. Direct memory access -- summary of simple use. Generally yes

channel can be dealt with separately. Plans

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ce will use. Determine what conditions will terminate the operation, and how the device, the program, and the hardware will find out about them. Determine whether the software will be, to the extent that they are not dynamically allocated. If you are using circular buffers, you will know by the time you get to Global initialization. Call BU

S.RESET whenever you want

to simulate a power-down, power-up cycle for the Bus Master, the expansion chassis, and the device on the expansion bus. Call BUSDMA.INIT. This has the effect of doing a hardware reset of the memory on the external bus to keep data intact, but has the effect of masking channels 1-3. Since either is now a read mask bit, if you have a multiplexed device using DMA on the system, you will have to read in the BUSDMA initialization in your own software. This may be a matter of administration. If the channel

is not masked (which

is after BUSDMA.INIT), call BUSDMA.MASK, then call BUSDMA.MODE, BUSDMA.SETPAGE, BUSDMA.SETADDRESS, and BUSDMA.SETCOUNTER in any order. (If your mode settings or program number for the channel are constant, you don't have to change them. When the channel is masked, it is a fatal error to set up the device. Now call BUSDMA.NMASK, then, when ready, start the device. (It could be started while the channel is masked if data would be lost, but this way always works.) The data operation is now successful. You will need to set things during the time, especially since you don't have interrupts. If you are going to use BUSDMA.READ or BUSDMA.READCOUNTER, or other with the need to suspend the channel temporarily for some reason, call BUSDMA.MASK. At the end, the call BUSDMA.UNMASK to resume. To stop the channel, call BUSDMA.A.MASK. It records memory access--technical

Notes (1) The current -and base transfer

counter register is kept in the hardware as the number of transfers remaining less one, and the channel checks after each byte transfer for the current transfer counter having been decremented from zero. BUSDMA.SETCOUNTER and BUSDMA.READCOUNTER perform the translation to the mode described above. (2) The address of the device

described herein are the same as on the IBM PC. They can be described by inspecting the Inter-lisp-D source code in this BUSMASTER library package. (3) The main point of this section is

to tell technical advanced readers how the BUSDMA mode is implemented. The truth about the Bus Master and the Intel 8237-5 DMA controller chip. This is for those who have read the specification for the Intel 8237-5 DMA controller chip or look at the Bus Master on IBM PCs. As it benefits, perhaps, to give hints to those who are thinking about using an exotic device through the Bus Master. This section is not intended to be a

tell a little about the read of the Bus Master functionality. That is

done by the BUSDMA function of the Interrupt Mask bits, Parity Error, and general the Bus Master status and control registers (except Reset via BUS.RESET). Note that interrupt from the external

bus device of the 1108 are supported by the Bus Master, but the 1108 microcode will present a low-priority interrupt. See also Technical Note (1) above. Intel 8237-5 A functionality that

does not apply to the hardware content of the Bus Master Channel. It is dedicated to memory refresh. And therefore block memory-to-memory transfer and block memory initialization are possible. If the device cannot assert the TC signal to the DMA controller. Command registers: the timing variations may not be physically possible. I don't know; DREQ & DACK are of course fixed. Mode register: "cascade" mode is of course not possible. Note that the page registers are not on the 8237-5 A.

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