BUSEXTENDER -- Bus Extension Port for 1108 with Extended Processor Option (CPE)

Initially released: 17 Sept 1984
Michael Herring

A user-designed device can be attached to an 1108 with Extended Processor Option (CPE) through the same connector that Xerox's PC-bus and Multibus adapters use. This document describes the protocol for this connector, and basic Interlisp-D functions for accessing it.

The Bus Extender (BX) connector allows the DandyTiger to read &/or write 16-bit words at any of 32 register-addresses on the external device. Four 1-bit status lines can also be read. An interrupt line is reserved for use with future microcode.

The maximum data transfer rate when the device is accessed from the Interlisp-D functons below is 150K words/second. Burst transfer rates of 2M words/second can be achieved with specialized microcode.

The BX connector is the DandyTiger CPE board's lower D-37 connector J1 (female). It is not cabled to the outside of the 1108.

Description of signals on connector

BX.0-15	Data. Bidirectional. BX.15 least significant.
SUA.4-7	Address (with fY.1). SUA.7 least significant.
fY.0	Direction. 1= from device to processor.
fY.1	Address (with SUA.4-7).
fY.2-3	Device select (with SelFP').
SelFP'	Device select (with fY.2-3). Active low.
FPCLK	Clock. Normally high (98ms min), 39 ns low, rising edge active. Always high when SelFP'=1.
FPI.0-3	Status lines. Asynchronous input to processor.
Interrupt'	Interrupt. Asynchronous input to processor. Active low. The current microcode version does not support this external interrupt, so Interrupt' *must not* be asserted (pulled down).

Signals are TTL active high except as stated. Since these are high-speed intra-processor bus signals, the cable must be short, e.g. 2 feet.

The external BX device is selected when fY.2=fY.3=SelFP'=0.

Writing to the register with address SUA.4-7=fY.1=0 must not have any significant effect. Such writes are generated by the central processor as a side effect of other operations.

With special cabling, the user device could share the BX connector with Xerox's PC-bus or Multibus adapters. Then the register-addresses with SUA.4-7 = 2 and 3 are reserved for the Xerox bus adapters, as is the status line FPI.1.

Timing requirements on the BX device will be included in later versions of this documentation. The write-to-device cycle is straightforward. The DandyTiger microcode assumes that reads from the BX device are pipelined over two BX cycles; that is, that the datum returned from the BX device during a read cycle is that addressed in the previous BX cycle.

Pin List -- for the CPE board's lower D-37 connector J1 (female).

1	SUA.7	11	FPI.2	21	BX.14	31	BX.5
2	SUA.6	12	FPI.1	22	BX.13	32	BX.4
3	SUA.5	13	FPI.0	23	BX.12	33	BX.3
4	SUA.4	14	5volt (1 amp)	24	BX.11	34	BX.2
5	fY.3	15	5volt (1 amp)	25	BX.10	35	BX.1
6	fY.2	16	FPCLK	26	BX.9	36	BX.0
7	fY.1	17	GND	27	BX.8	37	GND
8	fY.0	18	GND	28	SelFP'		
9	Interrupt'	19	GND	29	BX.7		
10	FPI.3	20	BX.15	30	BX.6		

(The pin numbers on page 38 of the CPE-FP schematic of 12/16/83 are mistakenly reversed.)

Interlisp-D access

An *address* here is an integer, taken as the five bits SUA.4,..,SUA.7,fY.1 (least significant).

(BX.INPUT *address*) reads a 16-bit datum from the *address*, returning it as an integer.
(BX.OUTPUT *datum address*) writes the least significant 16 bits of *datum* to the *address*.
(BX.READSTATUS) returns the four status bits FPI.0,..,FPI.3 (least significant) as an integer. Note that BX.READSTATUS accesses the Parallel Port.