

Extension Port for 108 with Extended Processor Option (CPE) Initial Release

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A user
-design ed device

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an be attached to a 108 with Extended Processor Option (CPE) through the same connector that Xerox's PC-bus and Multi-bus adapters use. This document describes the protocol for this connector, and basic Interlist-Dfunction for accessing it. The Bus Extender (BX) connector

allows the Dandy Tiger to read &/or write 16-bit words at any of 32 registers - addresses on the external device. Four 1-bit status lines can be read. An interrupt line is reserved for use with future microcode. The maximum data transfer

rate when the device is accessed from the Interlist-D functions is about 150K words/second. But transfer rates of 2M words/second can be achieved with special microcode. The BX connector is the Dandy Tiger CPE board's slower D-37 connector (female). It is not cable to the outside of the e1108.

Description of signal lines

connector BX-15 Data Bi direction

a

1. BX.15	least significant. SUA.4-7 Address (with FY.1)
.SUA.71	most significant. FY.0 Dir.ction.1=from device
ceto	processor. FY.1 Address (with SUA.4-7)
.FY.	2-3 Device select (with S
elFP')	.SelFP' Device select (with
Y.2-3)	.Active low. PCLK Clock. Normally high (
98msm	in), 39 ns low, rising edge active. AllowayshighwhaSelFP'=1. FPI.0-3 Stat usli
hronous	input processor. Interrupt' In te rrupt. Asyn
chronous in	put to processor. Active low. The current microcode version does not support this external
	interrupt, so Interrupt must not be asserted (pulled <u>down</u>). Signal is active high

Except as stated. Since these are high-speed internal processor bus signals, the cable must be shielded, e.g. 2 feet. The external BX device is

selected when FY.2 = FY.3 = SelFP' = 0. Writing to the register with address SUA.4-7 = FY.1-0 must not have any significant effect. Successive registers are generated by the central processor as side effect of other operations. With special cabling, the user device could share the BX connector with Xerox's PC-bus or Multi-bus adapters. Then the register - address switch SUA.4-7 = 2 and 3 are reserved for the external bus adapters, as is the status line FPI.1. Timing requirements on the B

X device will be included in the literature so that this documentation. The write-to-device cycle is straightforward. The Dandy Tiger microcode assumes that read from the BX device are pipelined over two BX cycles; that is, that the return from the BX device during a cycle is that address in the previous BX cycle.

w
erD37 conneto rJ1 (fe male).1 SUA.7I1FP I.221BX.1 43BX.52SUA.6
2

F	PI.12	2B	X.133	2B	X.43S	UA	.513
F	PI.02	3B	X.123	3B	X.34S	UA	.414
5	volt(1a	mp)24	BX	.1134	BX	.25f
Y	.3155	vo	lt(1a mp)25B	X.	1035B	X.	16fY
.	216F	PC	LK26X.936B	X.	07fY.	11	7GND
2	7BX.	83	7GND8	fY	.018	GN	D28S
e	IFP'	9I	n te	rr	upt'	19	GND
2	9BX.	71	0FP	I.	320BX.		
1	530BX.6(Th	ep	inn	um	bers		
on	page3	8o	ftheC	PE	-FPs		

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integer,takenasthe

f

iv *ebits*SUA.4, .. ,S UA.7,fY1(lea st sig nifi cant).(BX.INPUTaddress) readsa16-bitdatumfr

omtheaddre ss,retur ningit a sanint eger. (BX. OUPUTdatmaddress)w ri te st heleasts
ignificant1 *bitso fdatum*totheaddre s.(BXREADSTA)FUSur ns *thefo* ur sta *tusbits* F

H.0,...,FPI.3(1 *estsigni fic ant*) asaninteger.NotthatBX.READSTAAccessesite PallelPo

rt.