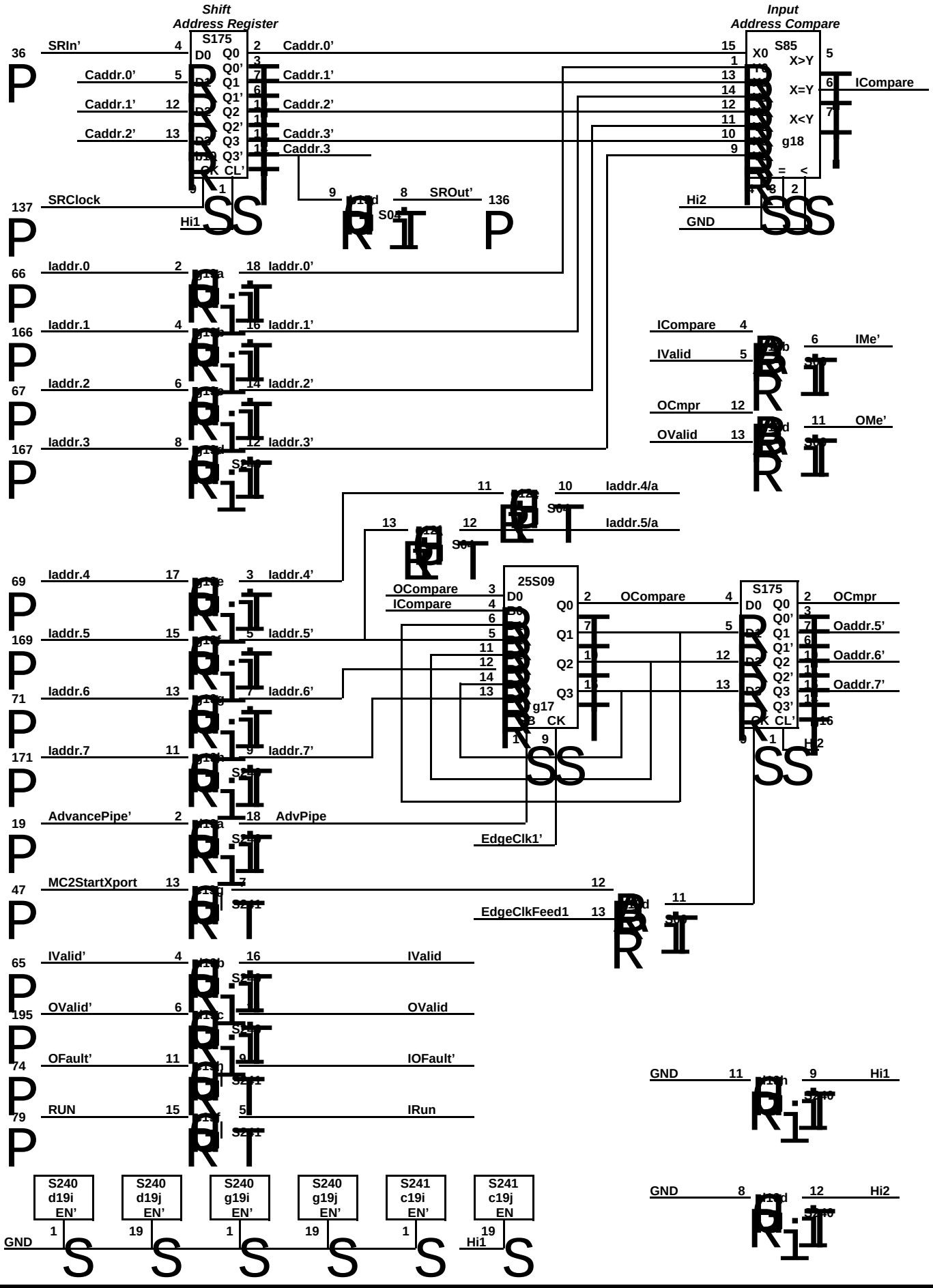
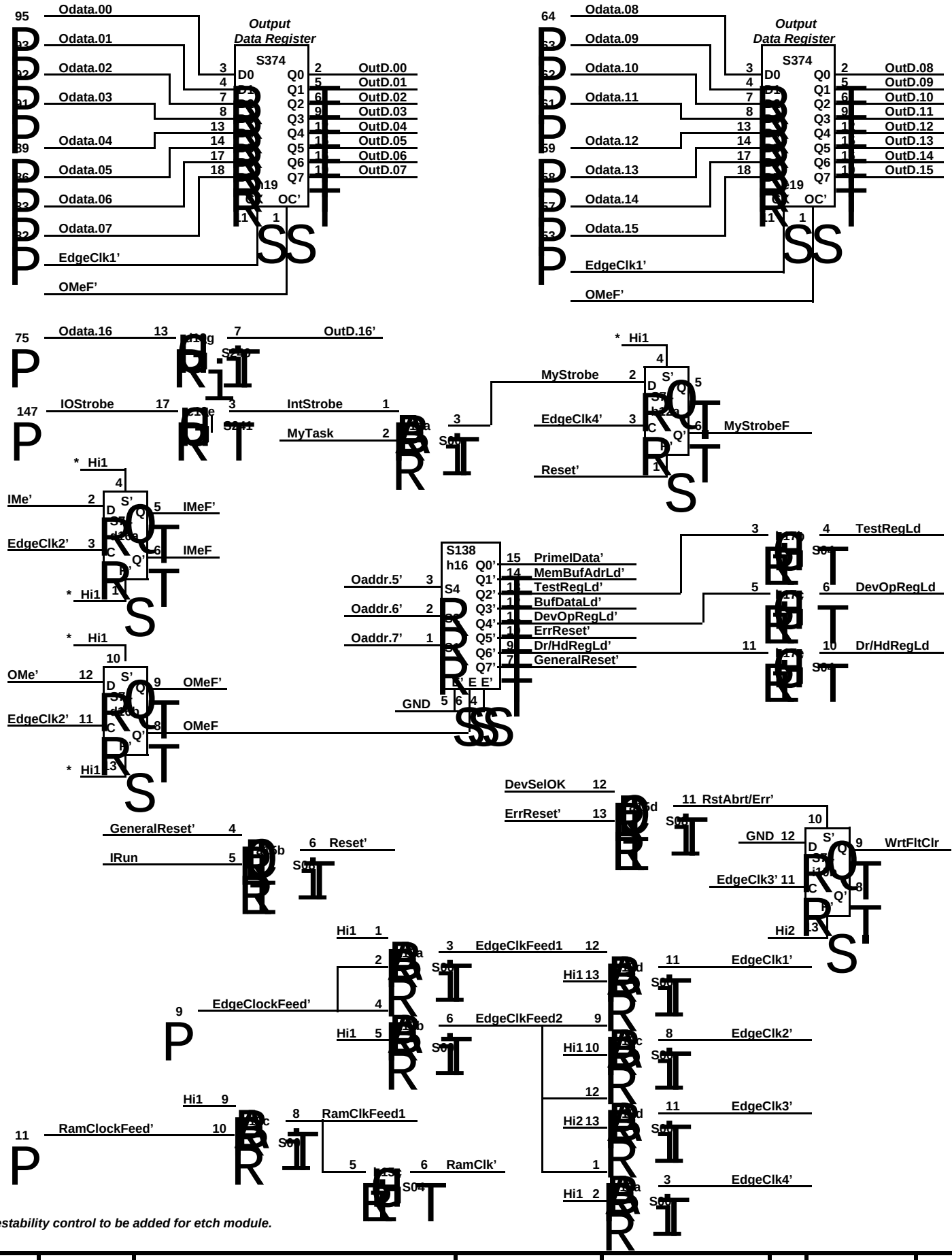
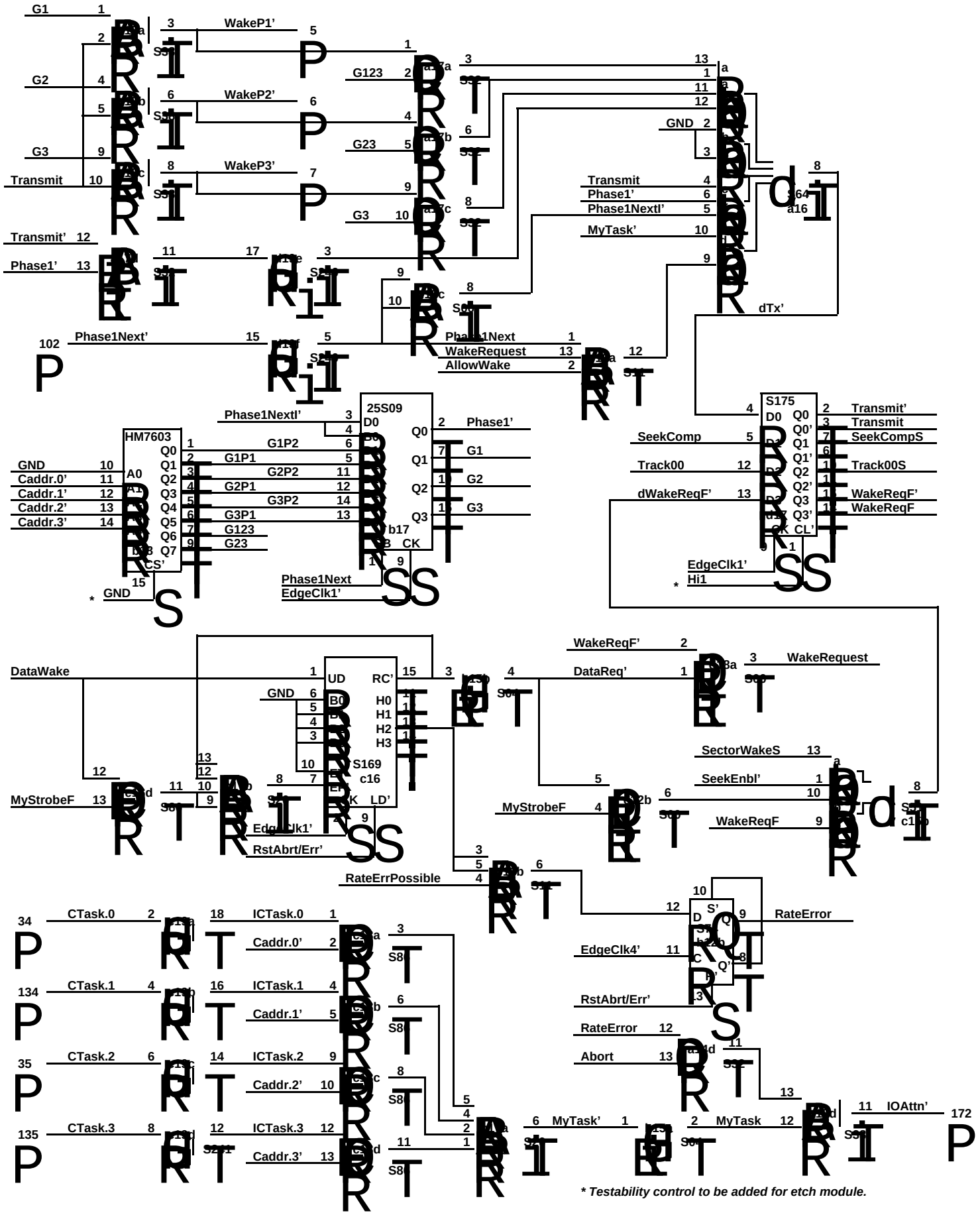


XEROX EOD	Project D0	IO INTERFACE Address	File RDC01.sil	Designer J. F. Cameron	Rev Gc	Date 7/28/78	Page 01

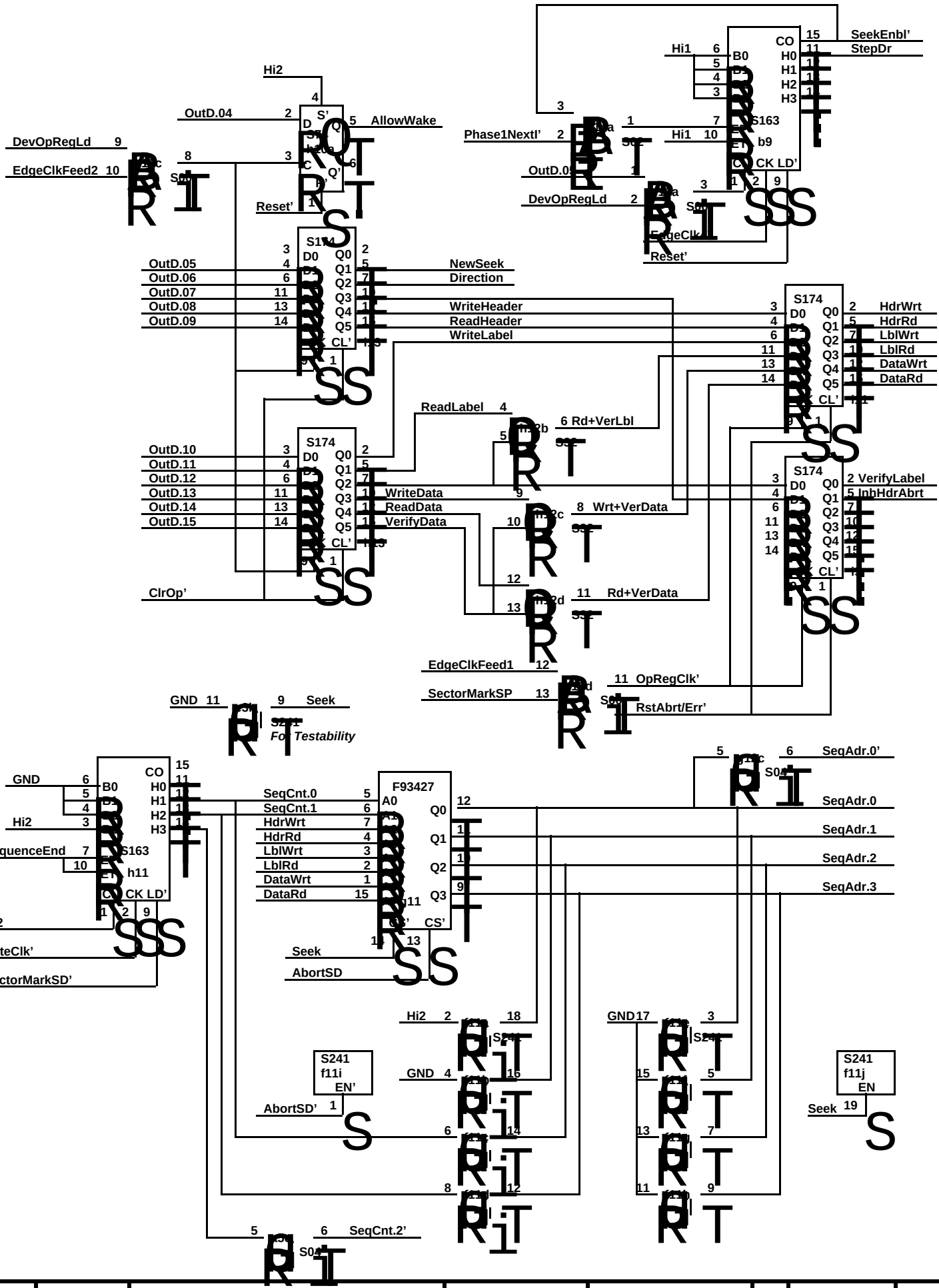


** Testability control to be added for etch module.*

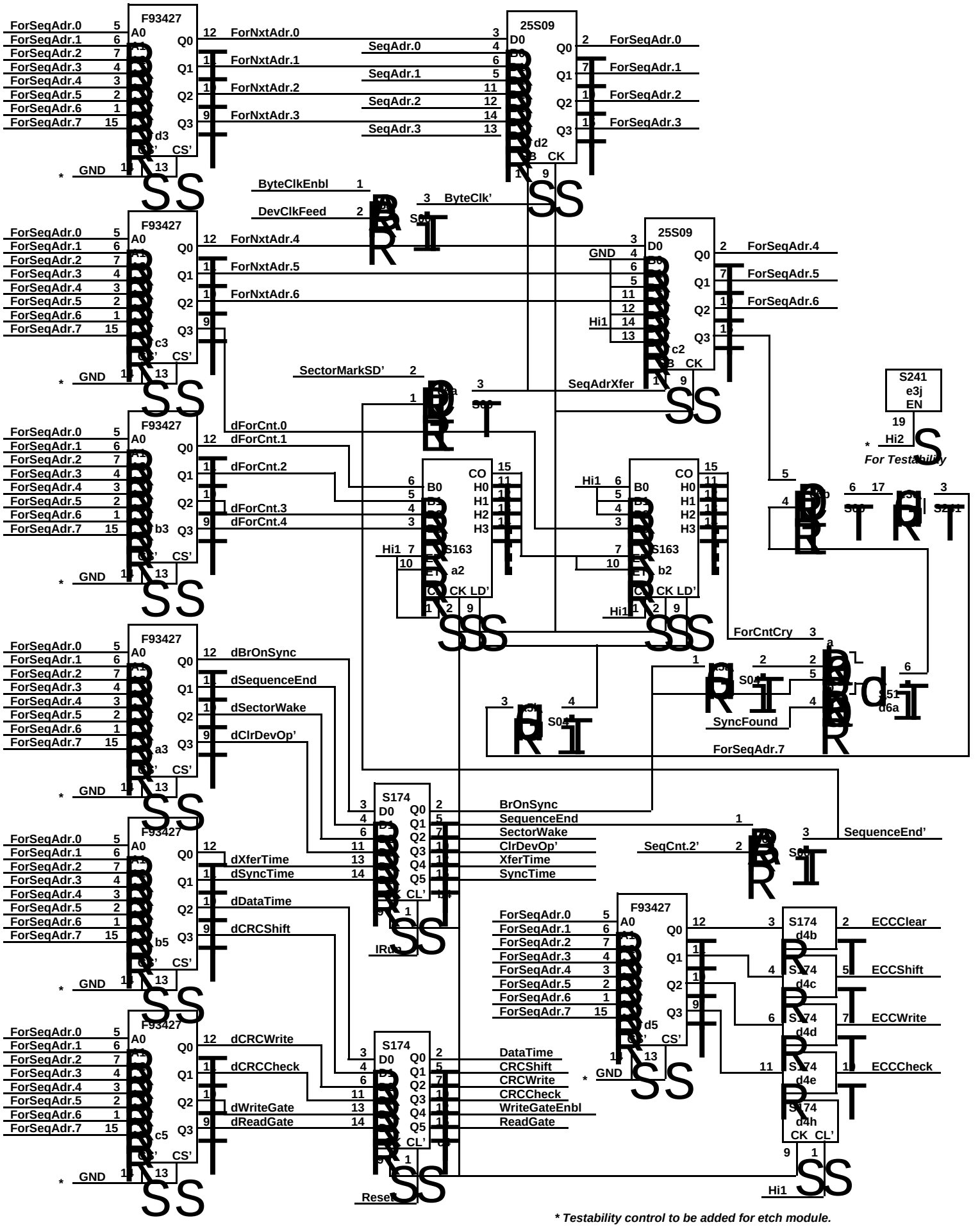
XEROX EOD	Project D0	IO INTERFACE OData/Clocks	File RDC02.sil	Designer J. F. Cameron	Rev Gc	Date 7/20/80	Page 02



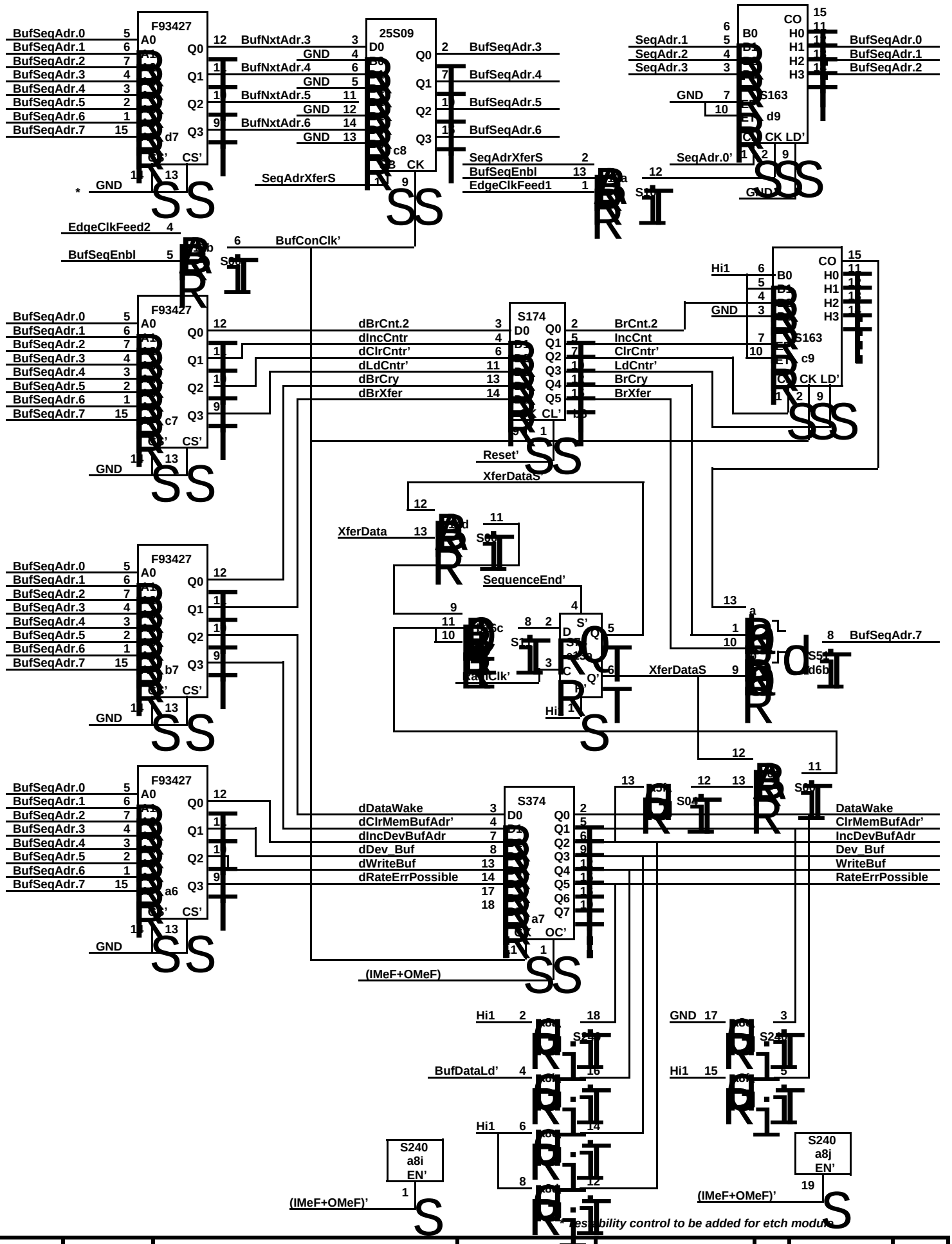
XEROX EOD	Project D0	IO INTERFACE WakeUp/CTask	File RDC03.sil	Designer J. F. Cameron	Rev Gc	Date 9/3/79	Page 03



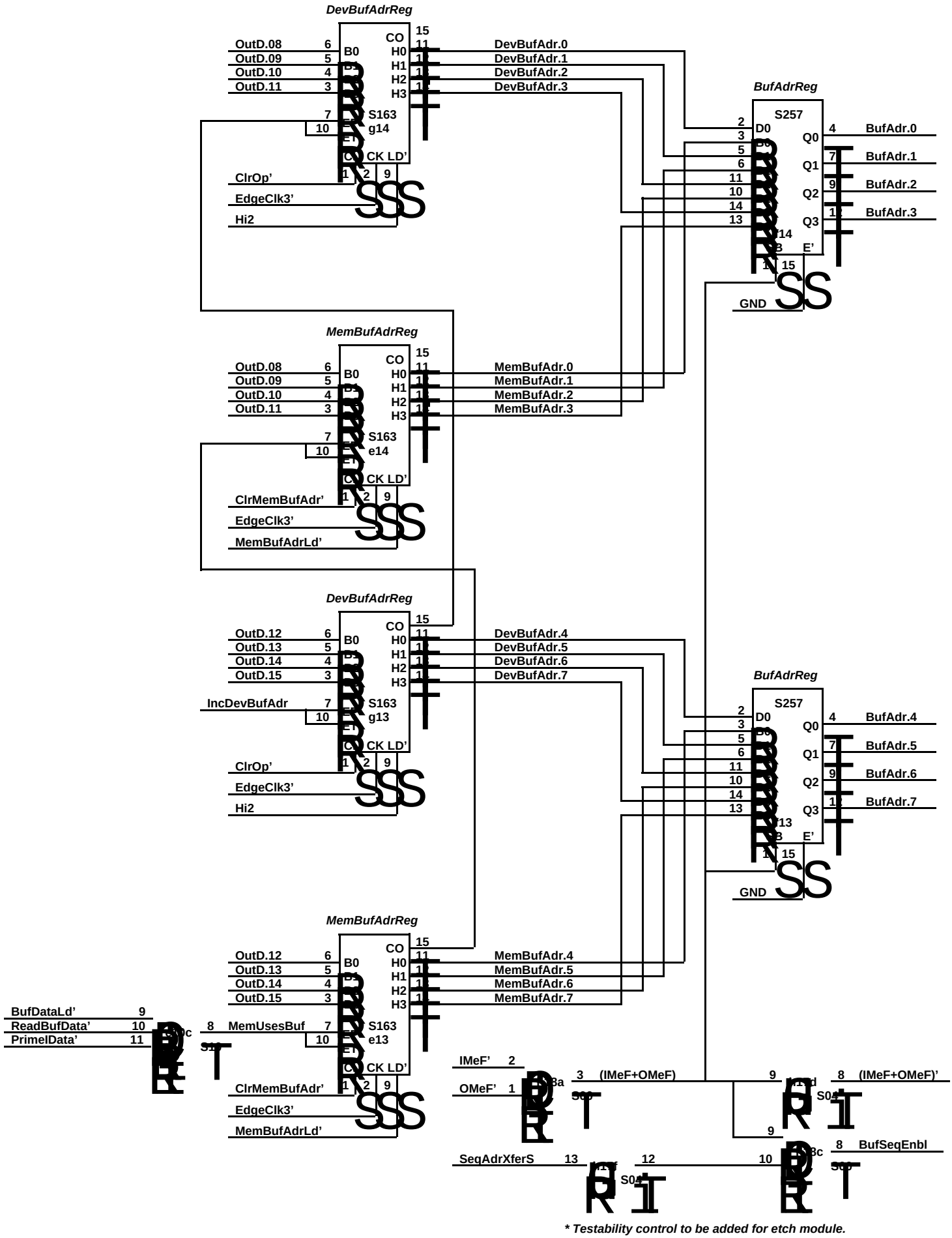
XEROX EOD	Project D0	Sequence Address Generator	File RDC04.sil	Designer J. F. Cameron	Rev Gc	Date 7/20/80	Page 04



XEROX EOD	Project D0	Device Format Sequencer	File RDC05.sil	Designer J. F. Cameron	Rev Gc	Date 7/20/80	Page 05

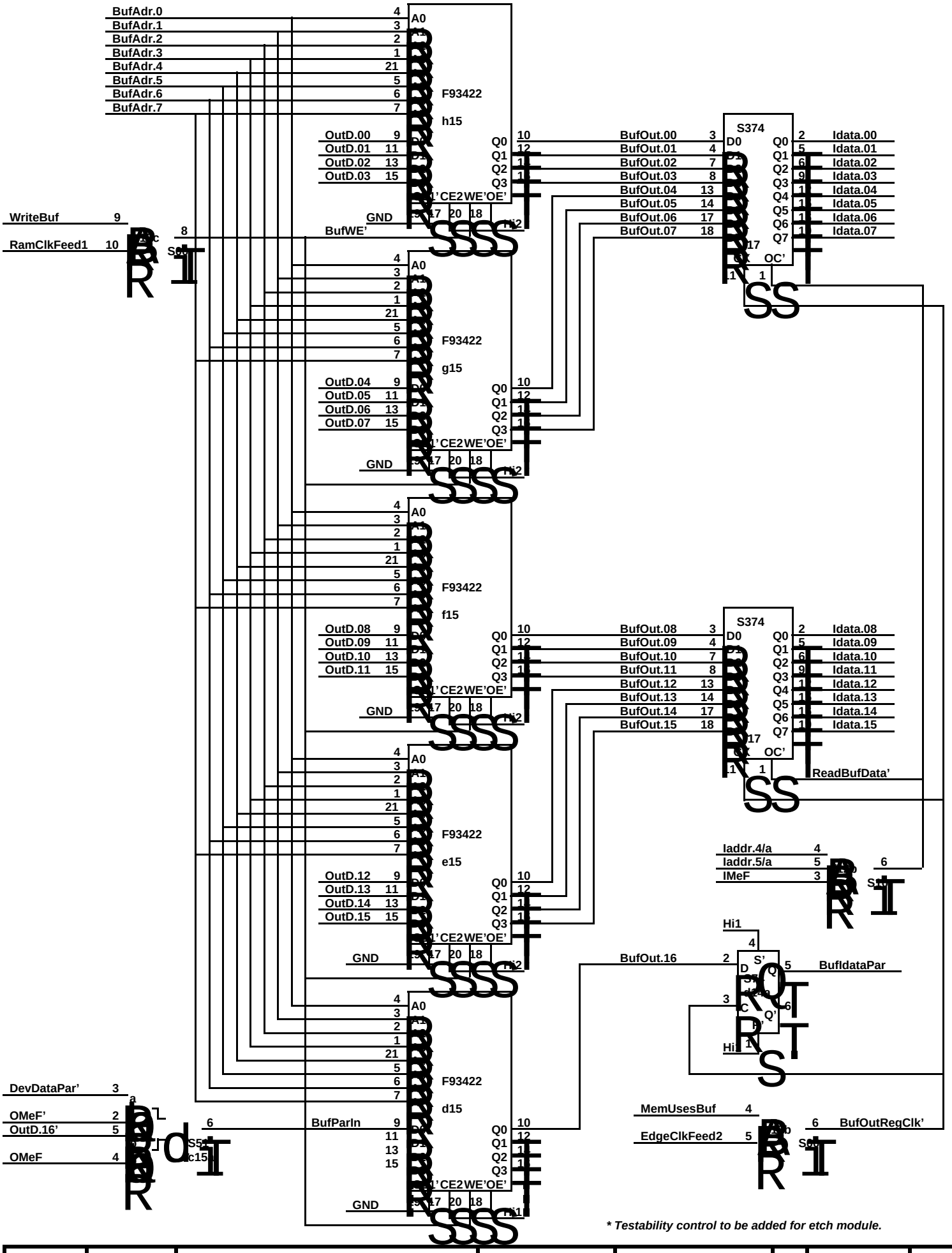


XEROX EOD	Project D0	Buffer Control Sequencer	File RDC06.sil	Designer J. F. Cameron	Rev Go	Date 1/24/79	Page 06

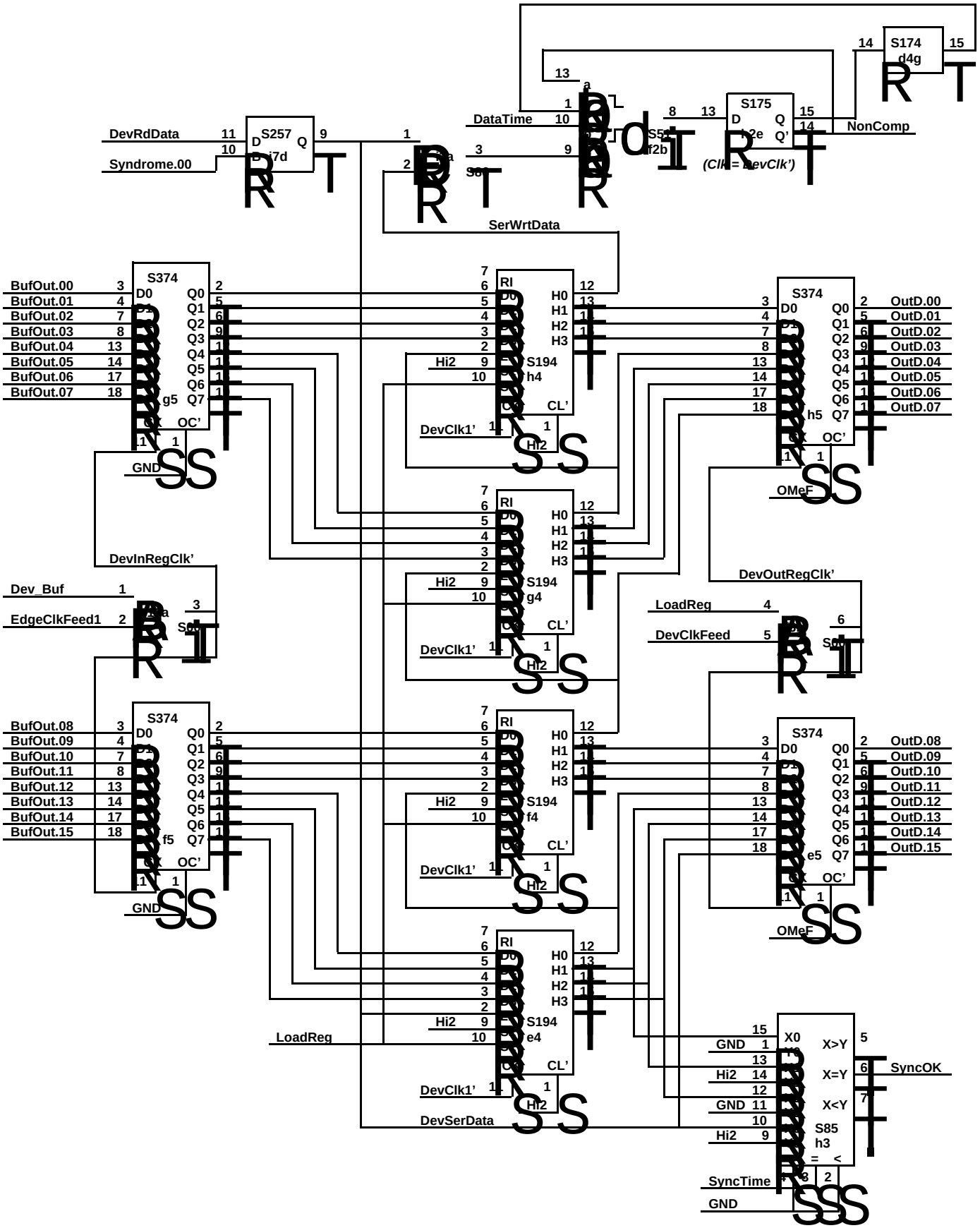


** Testability control to be added for etch module.*

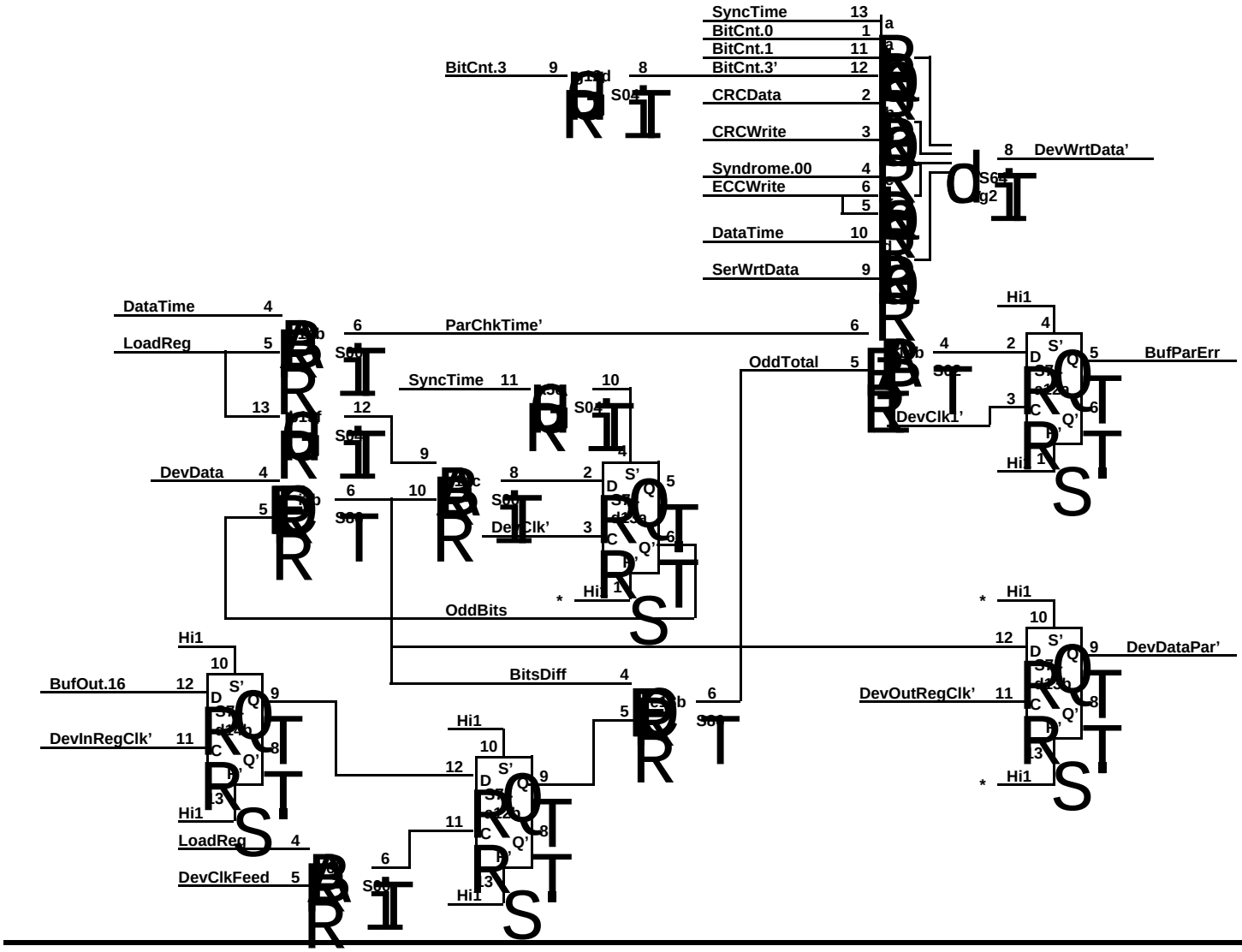
XEROX EOD	Project D0	Data Buffer Address Register	File RDC07.sil	Designer J. F. Cameron	Rev Gc	Date 9/3/79	Page 07

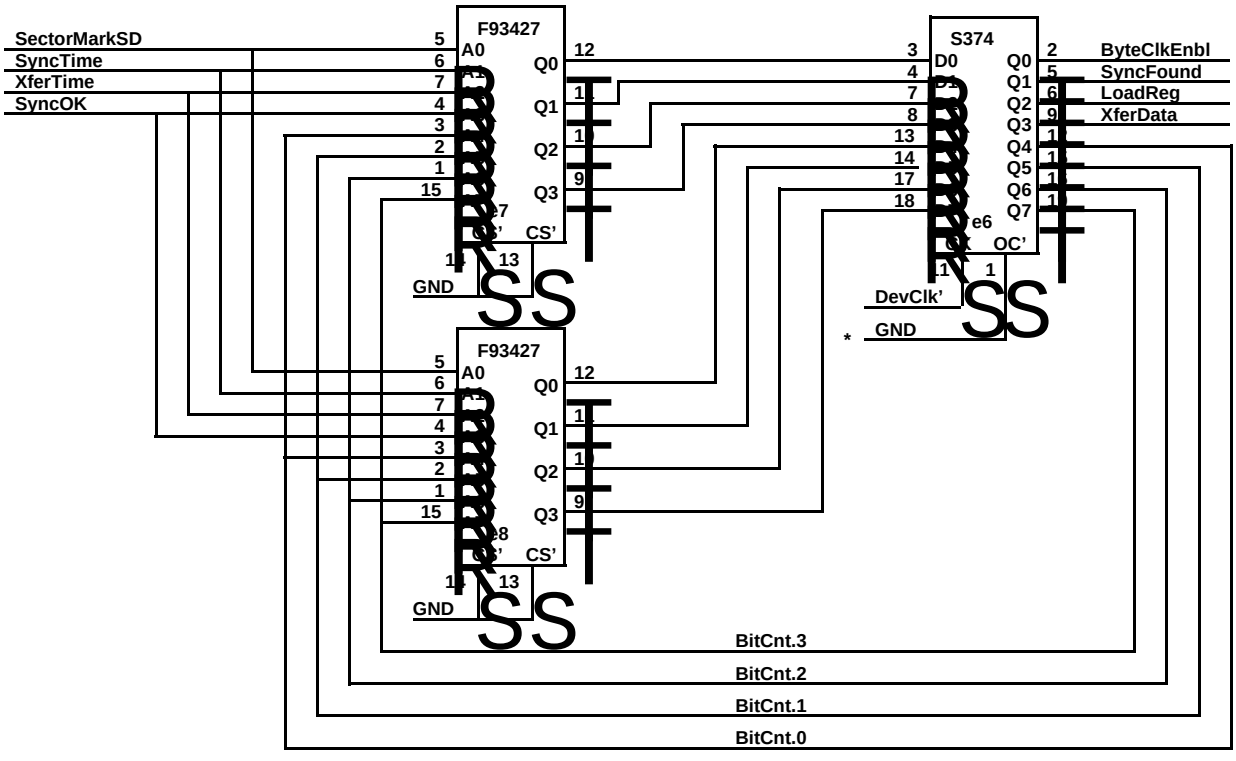


XEROX EOD	Project D0	Data Buffer	File RDC08.sil	Designer J. F. Cameron	Rev Gc	Date 9/4/79	Page 08



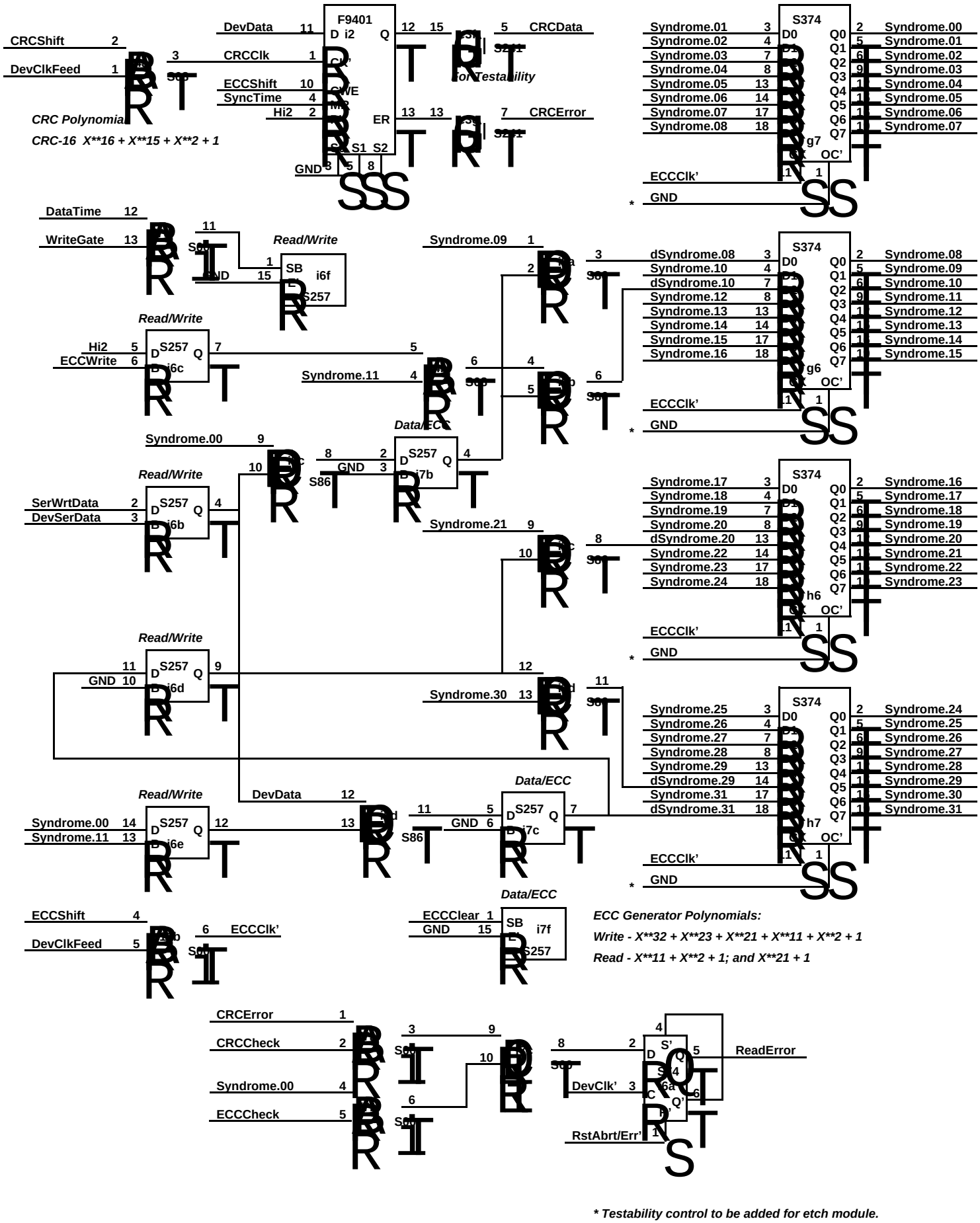
XEROX EOD	Project D0	Data Serializer/Deserializer	File RDC09.sil	Designer J. F. Cameron	Rev Gc	Date 7/20/80	Page 09



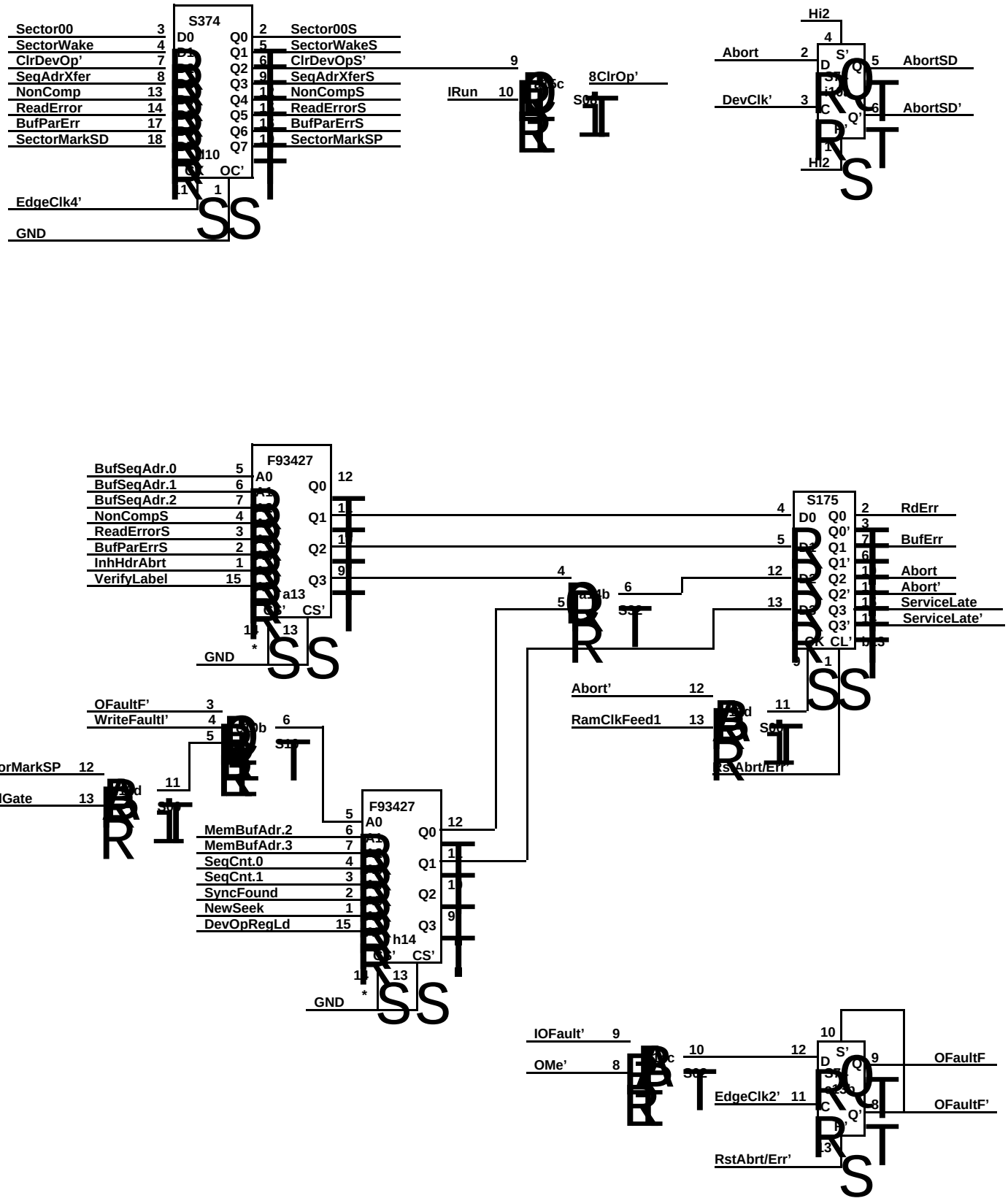


** Testability control to be added for etch module.*

XEROX EOD	Project D0	Device Write Data; Parity Check Data Timing Generator	File RDC10.sil	Designer J. F. Cameron	Rev Go	Date 10/16/78	Page 10

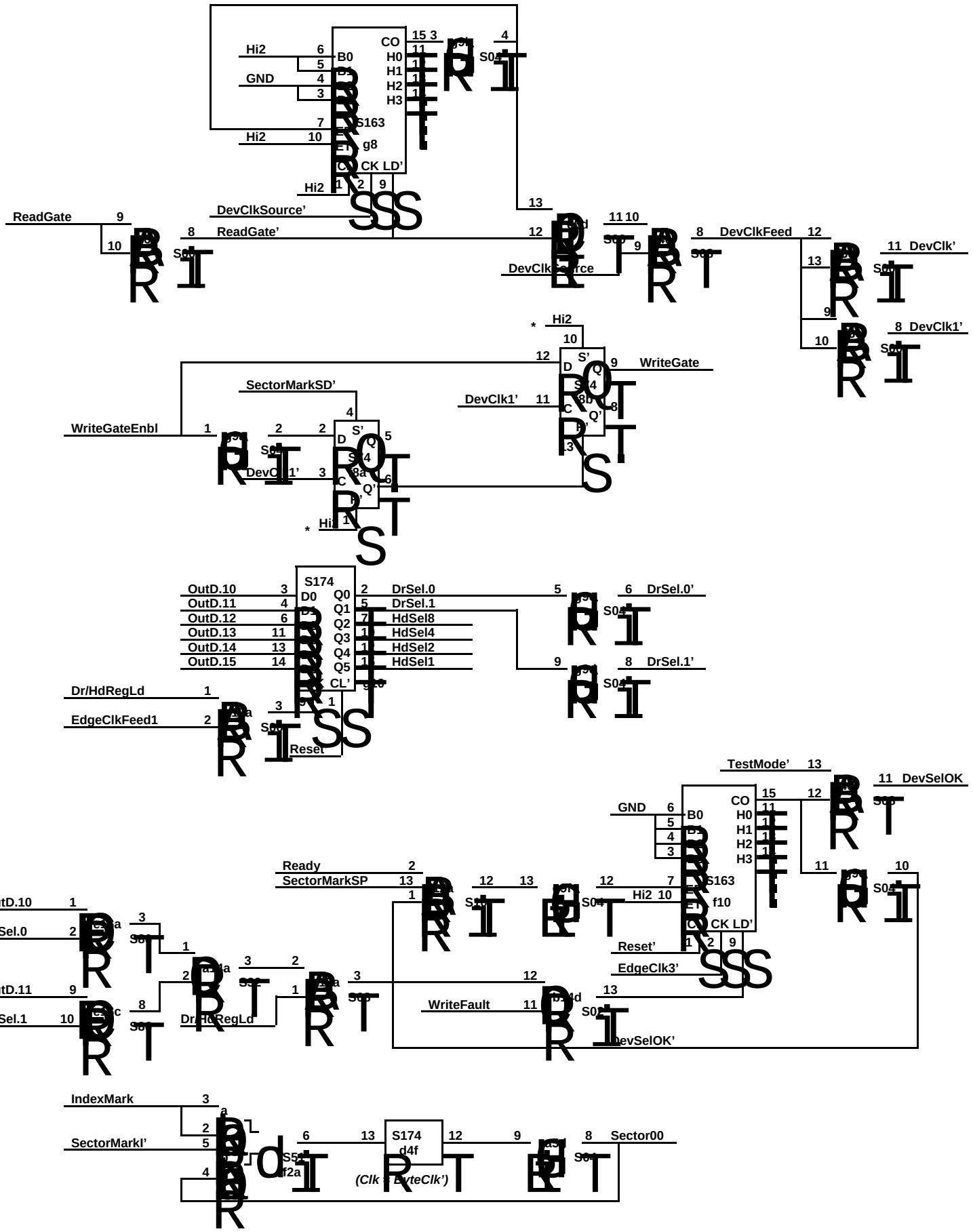


XEROX EOD	Project D0	CRC/ECC Gen/Check	File RDC11.sil	Designer J. F. Cameron	Rev Gc	Date 7/20/80	Page 11



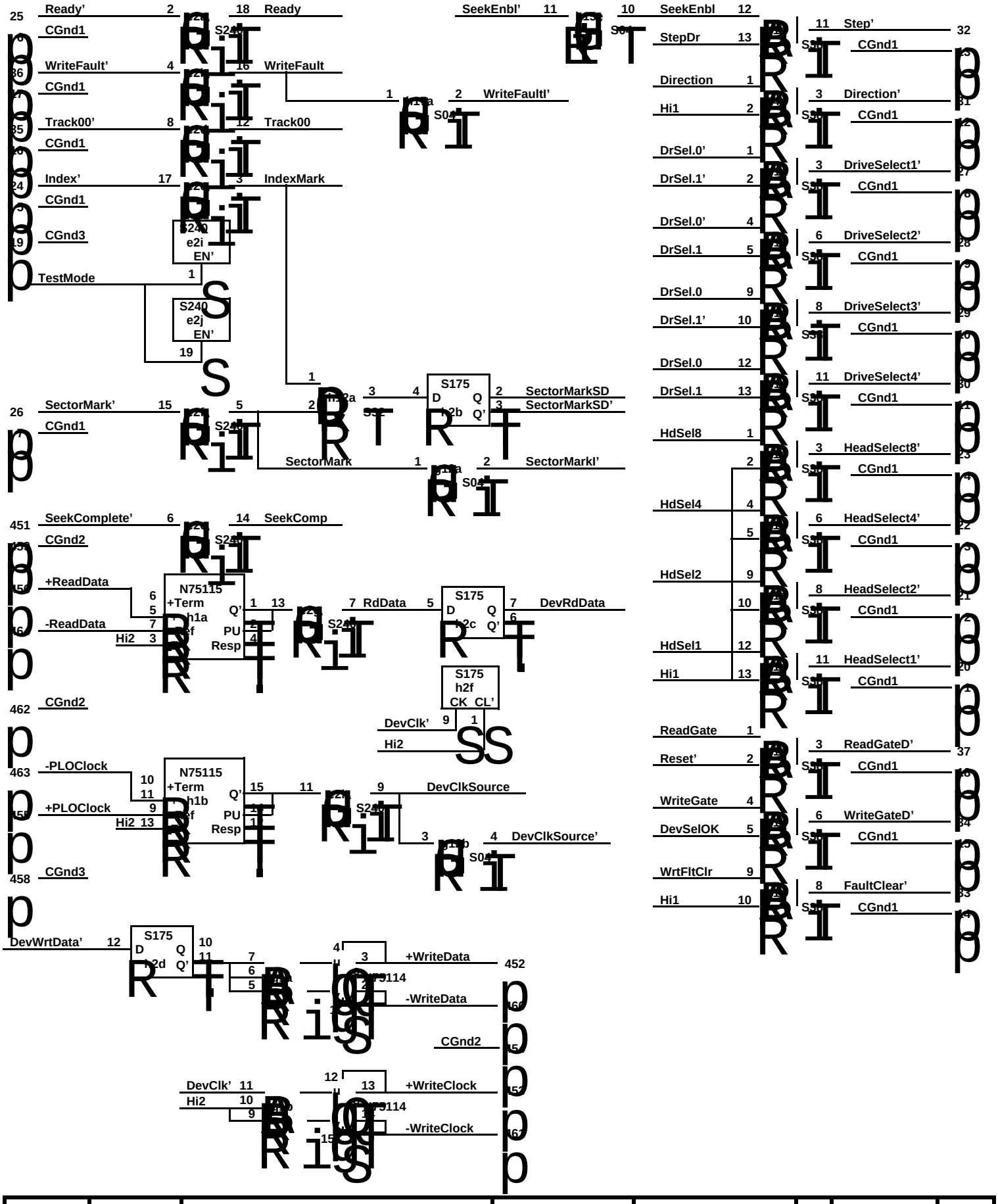
** Testability control to be added for etch module.*

XEROX EOD	Project D0	Sychronization Logic; Error Control	File RDC12.sil	Designer J. F. Cameron	Rev Gc	Date 7/20/80	Page 12

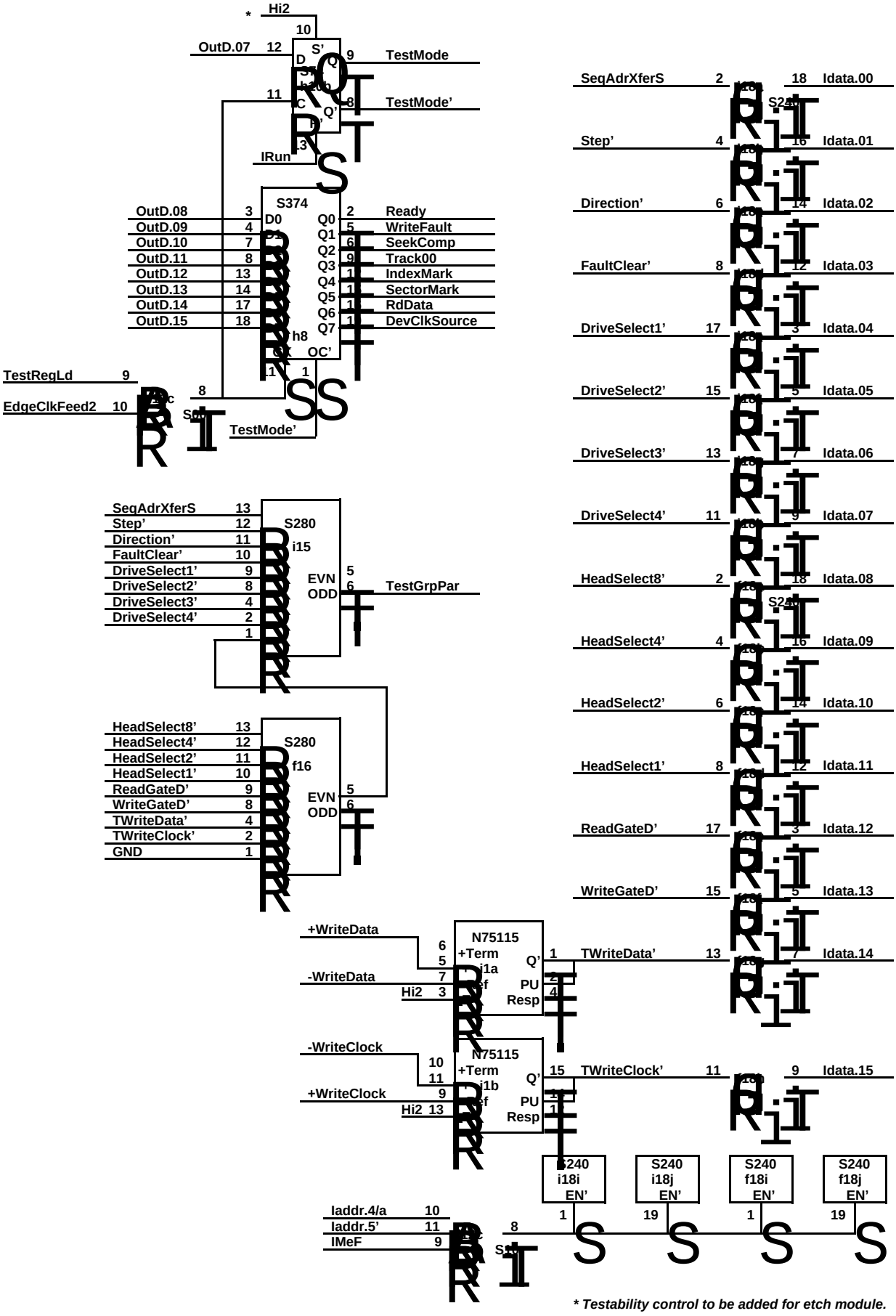


** Testability control to be added for etch module.*

XEROX EOD	Project D0	Drive Select: Interface Control	File RDC13.sil	Designer J. F. Cameron	Rev Go	Date 10/16/78	Page 13

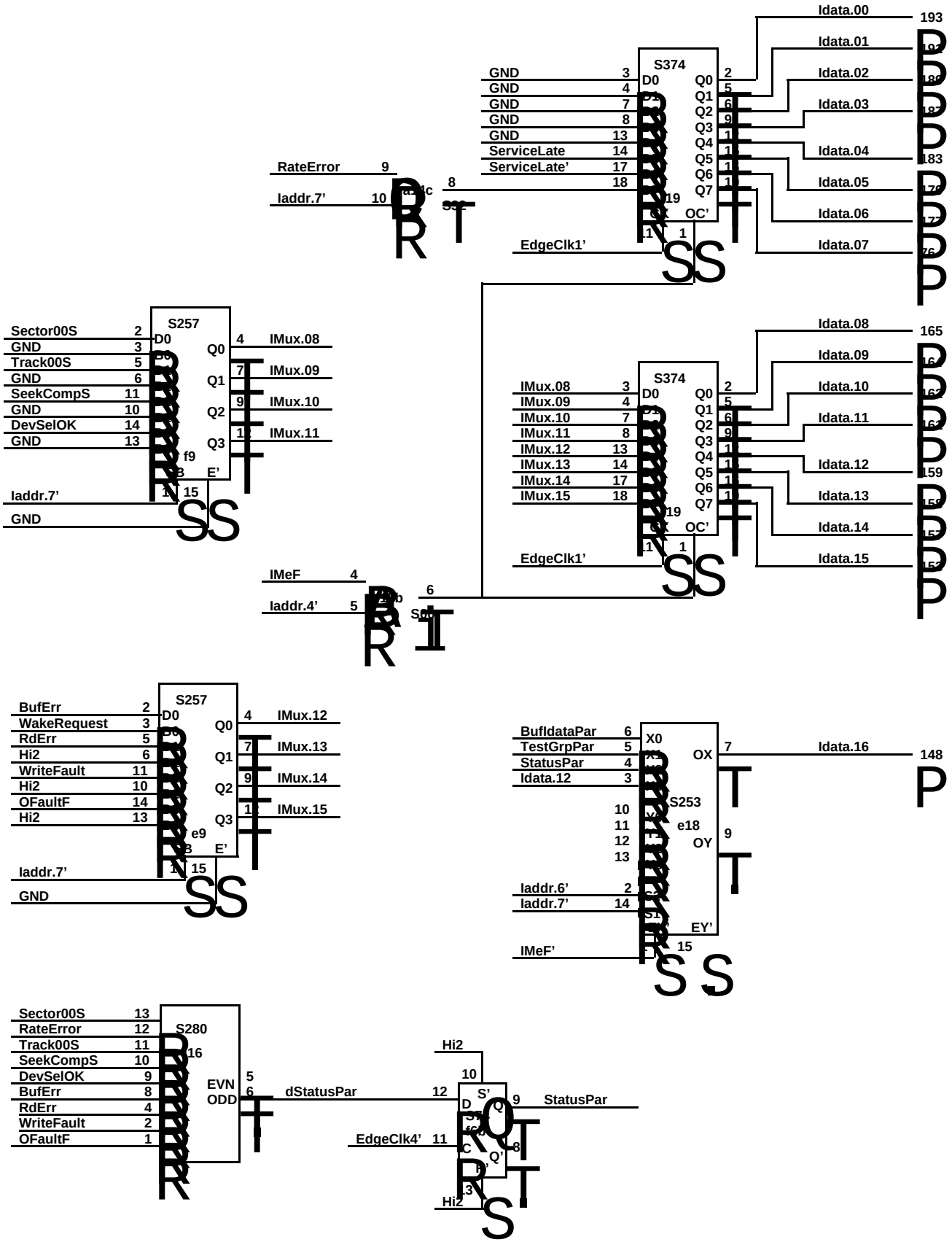


XEROX EOD	Project D0	Drive Interface	File RDC14.sil	Designer J. F. Cameron	Rev Go	Date 12/27/78	Page 14



** Testability control to be added for etch module.*

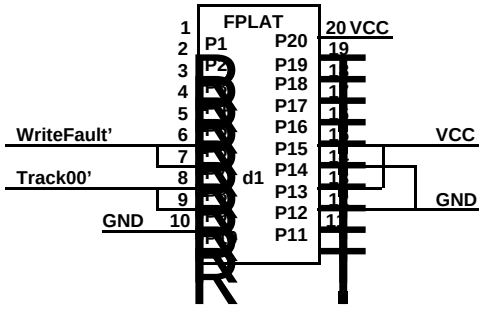
XEROX EOD	Project D0	Diagnostic Control	File RDC15.sil	Designer J. F. Cameron	Rev Go	Date 10/16/78	Page 15



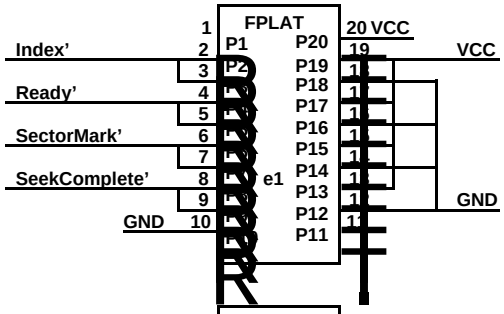
** Testability control to be added for etch module.*

XEROX EOD	Project D0	Idata Mux Register/Parity Gen	File RDC16.sil	Designer J. F. Cameron	Rev Go	Date 2/6/79	Page 16

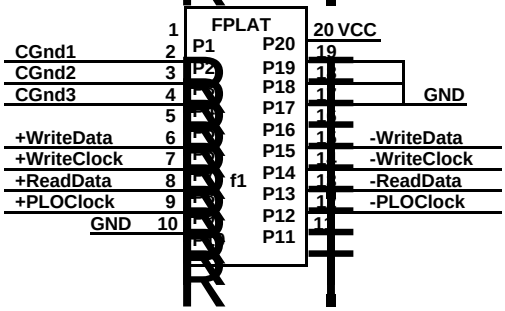
SPLAT A



SPLAT B

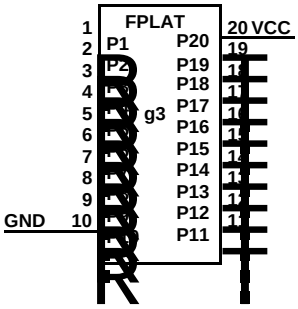


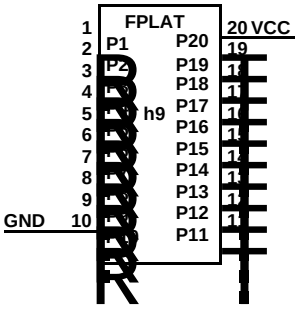
SPLAT C

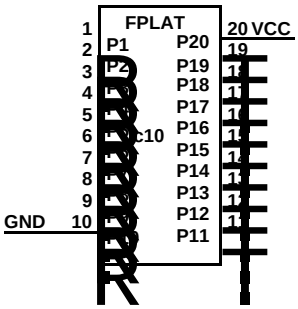


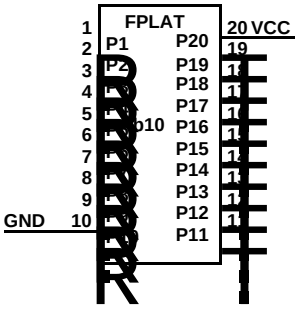
Note: Splats A,B, and C are 16 pin platforms centered in the 20-pin pattern

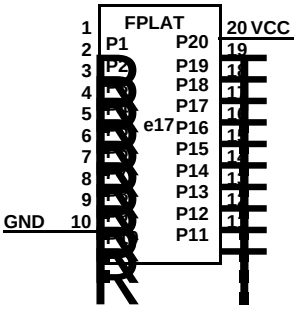
Spare Positions (5):











Rev A: Initial Release

Rev B:
Added SyncTime to Timing Generator PROM address input. Log. Dwg. p. 10.
Changed DevSelOK counter load control so that Dr/HdRegLd loads counter only if DrSel[0:1] is changed. Log. Dwg. p. 14.
Added Seek counter at b9 to produce seek Step pulse when DevOpReg is loaded with Seek bit (OutD.05). Causes SeqAdr[0:3] to be 0000 when Seek is true. Inhibits Wake-up until Step has been generated. Log. Dwg. p. 2, 3, 4, 5, & 15.
Replaced S189 (16 word) buffer with F93422 (256 word) buffer. Log. Dwg. p. 7 & 8.
Deleted Wake PROM and Counter; removed XferLate from IOAttn; deleted Flow Control Counter; added Data Wake up/down counter; added 3 wakw count to IOAttn. Log. Dwg. p. 3 & 13.
Deleted DRConnect signals and IDWord parity gen. Log. Dwg. p. 14 & 16.
Added ability to load DevBufAdrReg & MemBufAdrReg from processor. Log. Dwg. p. 6 & 7.
Numerous minor changes in mechanization as a result of above. Log. Dwg. p. all.

Rev C:
Set SectorMarkSP with SectorMarkSD. Log. Dwg. p. 12
Removed cross wire of MemBufAdrReg Clear and SectorWakeS strings. Log. Dwg. p. 7.
Disabled Seek Counter at max count. Log. Dwg. p. 4.
Changed reset of Op Register from Reset' to RstAbrt/Err'. Log. Dwg. p. 4.
Added RateError FF. Log. Dwg. p. 3.
Added DataReq to hold term for WakeReqF to override IOStrobe reset. Log. Dwg. p. 3.
Added term to Wake Counter enable to prevent incrementing beyond max, or decrementing below 0. Log. Dwg. p. 3.
Adds RateError to Status Parity Generator. Log. Dwg. p. 16.
Inverted Sync pattern. Log. Dwg. p. 9.
Changes DecClkEnable counter clock to DevClkSource'. Log. Dwg. p. 13.
Adds SectorMarkI'. Log. Dwg. p. 14.
Fixes Testability control. Log. Dwg. p. 5.
Fixes Idata Parity select. Log. Dwg. p. 16.
Removes 25S09s from BufAdrReg. Replaces them with s257s. Log. Dwg. p. 7.
Changes RateError qualifier to DataWrt. Log. Dwg. p. 3.
Changed I/O connections to device to reflect etch version with multiple drives. Log. Dwg. p. 14.
Made SequenceEnd' true last byte time of SequenceEnd only. Added S00 at b6. Log. Dwg. p. 5.
Moved S280 from i14 to i15. Log. Dwg. p. 15

Rev D:
Added one clock delay and DevClk synchronization to parity error logic. Log. Dwg. p. 10.
Deleted Abort from Wake Request logic. Log. Dwg. p. 3.
Revised DataXferS logic. Log. Dwg. p. 6.
Changed BufSeqAdr clock qualifier to SeqAdrXferS. Log. Dwg. p. 6.
Devided load on DevClk'. Log. Dwg. various.
Added TestMode' qualifier to DevSelOK to prevent writing on device in Test Mode. Log. Dwg. p. 13.
Added PrimeIData to BufAdrReg Select. Log. Dwg. p. 6 & 7.
Added Write Fault Clear FF. Log. Dwg. p. 2.
"Or'ed VerifyLabel with ReadLabel at Op Reg input. Log. Dwg. p. 4.
Qualified BufSeqAdr Register Clock wiht (IMeF+OMeF)'. Log. Dwg. p. 6.
Changed data error check to look at Syndrome.00 during ECCCheck. Log. Dwg. p. 11.
Changed DevBufAdrReg clear term from SectorWakeS' to ClrDevOpS'. SectorWake cleared too soon. Changed SectorWakeS' to SectorWakeS. Log. Dwg. p. 3, 5, 7, & 12.
Added direct set of MyStrobeF by AllowWake to insure Wake-up inhibit. Log. Dwg. p. 2.
Removed Reset from S174 @ d4 to prevent "glitch" of Sector00. Log. Dwg. p. 5.
Changed reset of XferDataS FF to SequenceEnd'. Log. Dwg. p. 6.
Changed latch of NonComp FF to insure at least 2 DevClk times on. Log. Dwg. p. 9.
Revised serial parity check/gen logic control. Log. Dwg. p. 10.
Added SectorMarkSP "and" ReadGate to Abort set term to indicate missing Sync pattern. Log. Dwg. p. 12.
Reversed phase of PLO Clock to increase margin of strobe on read. Log. Dwg. p. 14.

Rev E:
Added SeqAdrXferS' to BufSeqEnbl to insure transfer of Sequence Address even if IMeF or OMeF is true. Log. Dwg. P. 6 & 7.
Changed CRC control from DataTime to ECCShift. Log. Dwg. p. 11.
Added detection for ServiceLate to indicate Header and Label data not loaded into buffer by Header SyncFound. ServiceLate added as Idata.05 in Status word. Log. Dwg. p. 12 & 16.
Changes Reset functions from single Output function with data specified operations to specific Output functions for General Reset and Error Reset to eliminate gate noise on direct reset lines. Log. Dwg. p. 2.
Deleted MemUsesBuf and PrimeIData from Buffer Control Sequencer to allow firmware control of MemBufAdrReg. Log. Dwg. p. 6 & 7.
Added sychronization of Abort with DevClk (AbortSD) to prevent erroneous setting of Sequencer Address Registers. Log. Dwg. p. 4 & 12.
Added RateErrPossible to Buffer Control Sequencer to define actual time when rateerror can occur. Decreased RateError wake-up count from 3 to 2 to insure RateError detection if delay in memory pipe and only 20 words initially loaded in RDC buffer. Log. Dwg. p. 3 & 6.
REQUIRES REV B PROMS!!!

Rev F:
Replaced Hi in Status Word with ServiceLate' in order to maintain correct parity. Log. Dwg. p. 12 & 16.
Added PrimeIData output function to MemUsesBuf to allow firmware to Prime Idata without parity error Deleted DevBufAdrLd output function. Log. Dwg. p. 2, 6, & 7.
Changed AllowWake and WakeReqF control to allow firmware control of AlowWake. Added WakeRequest to IDWord bit 12 for firmware test. This is to facilitate "booting" from the disk. Log. Dwg. p. 2, 3, 4, & 16.

Rev G:
Changed AllowWake so that Odata.04 = 1 sets AllowWake to comply with unpublished convention of setting output registers to zero causing initialization of controllers. Log. Dwg. p. 4.

Rev Ga: generated from Rev G on 4/11/79 by CPT.

1) Redrew splats at d1, e1, f1 as FPLATS to avoid ROUTE trace cuts (pg 17).

2) Added spare positions at g3, h9, i9, e17, b10, c10 (pg 17).

Rev Ga: generated from Rev G on 4/11/79 by CPT.

1) Redrew splats at d1, e1, f1 as FPLATS to avoid ROUTE trace cuts (pg 17).

2) Added spare positions at g3, h9, i9, e17, b10, c10 (pg 17).

Rev Gb: 9/3/79 - CPT

This change is a manual addition to the revision Ga MultiWire board.

1) Lift the following pins:

a15.12
c16.9
d10.6
i13.10
a13.15

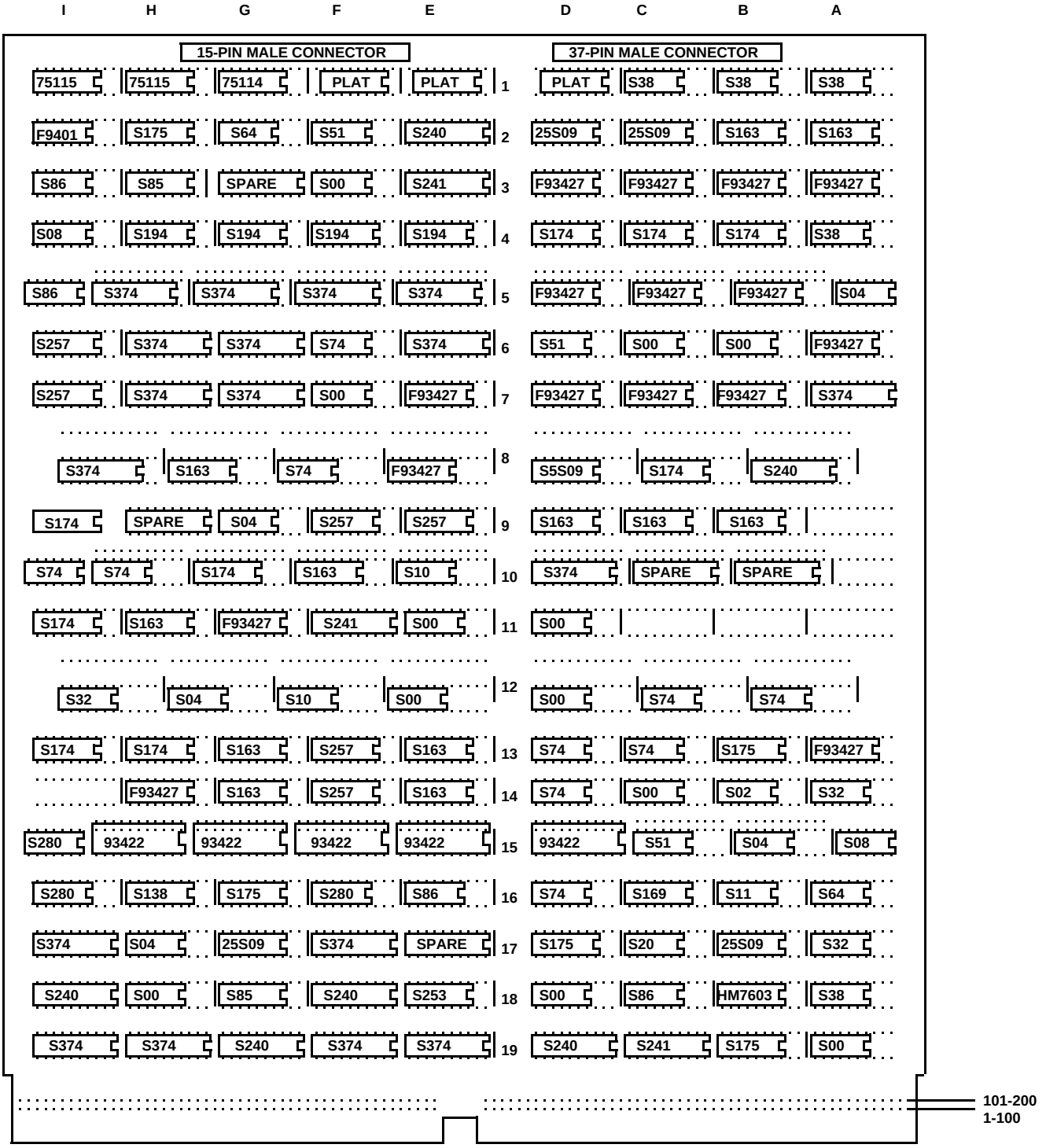
2) Add an S174 IC in position i9, and wire i9.16 to Vcc.

3) Add the following wires:

a15.12 to i16.9 (DevSelOK, pg 2,16)
c16.9 to a15.11 (RstAbrt/Err', pg 3,2)
d10.6 to a15.9 (ClrDevOpS', pg 12)
a15.8 to h13.1 (ClrOp', pg 4,7 - new signal name)
a15.10 to a15.5 (IRun, pg2,12)
i13.10 to 19.4 (Unnamed signal - was InhHdrAbrt, pg 4)
h13.7 to i9.3 (Unnamed signal - was VerifyLabel, pg 4)
i11.9 to i9.9 (OpRegClk', pg 4)
i11.1 to i9.1 (RstAbrt/Err', pg 4)
i9.5 to a13.1 (InhHdrAbrt, pg 4,12)
i9.2 to a13.15 (VerifyLabel, pg 4,12)

Rev Gc: 7/18/80 (Multiwire) - CPT:

1) Formed signal NewSeek (pg 4), and made old Seek signal =0 so that the format sequencer will treat seek as a nop.
2) Changed b13 clock from EdgeClk to RamClk (pg 12).
3) Reset b4 with IRUN (pg 5).
4) a3 Prom must be revision X.
5) Added signal DevSerData (p. 9 and 11) to cause buffer parity generation on DevData to include ECC bits.

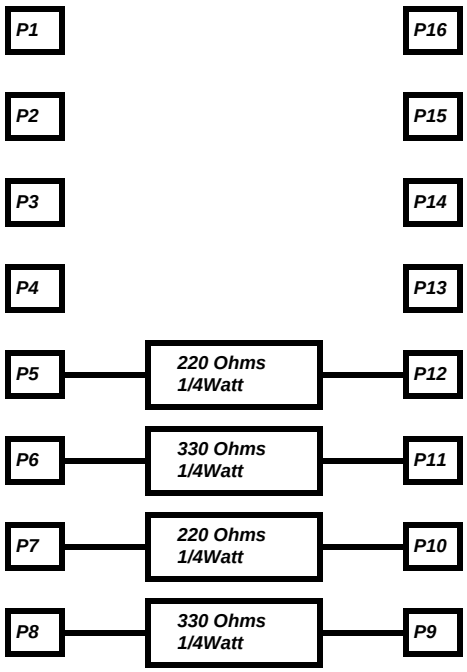


20pins: A 16pins: B 14pins: C 22pins: D 24 pins: E

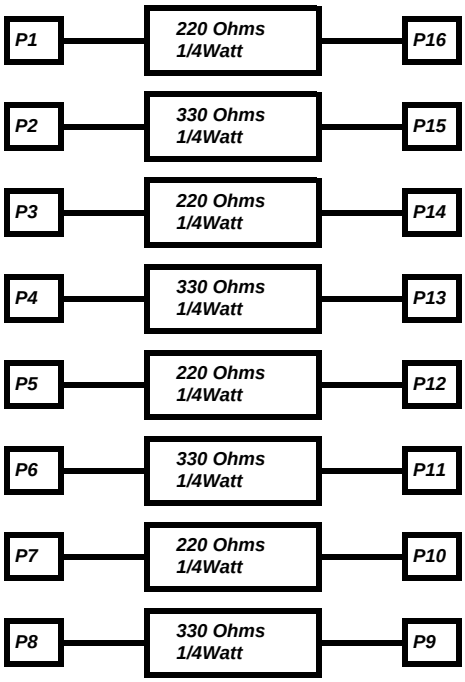
Note: The short vertical lines indicate filter capacitor locations.

XEROX CSL	Project D0	RDC Layout	File RDCLayout.sil	Designer J. F. Cameron	Rev Gc	Date 7/19/80	Page 19

SPLAT A



SPLAT B



SPLAT C