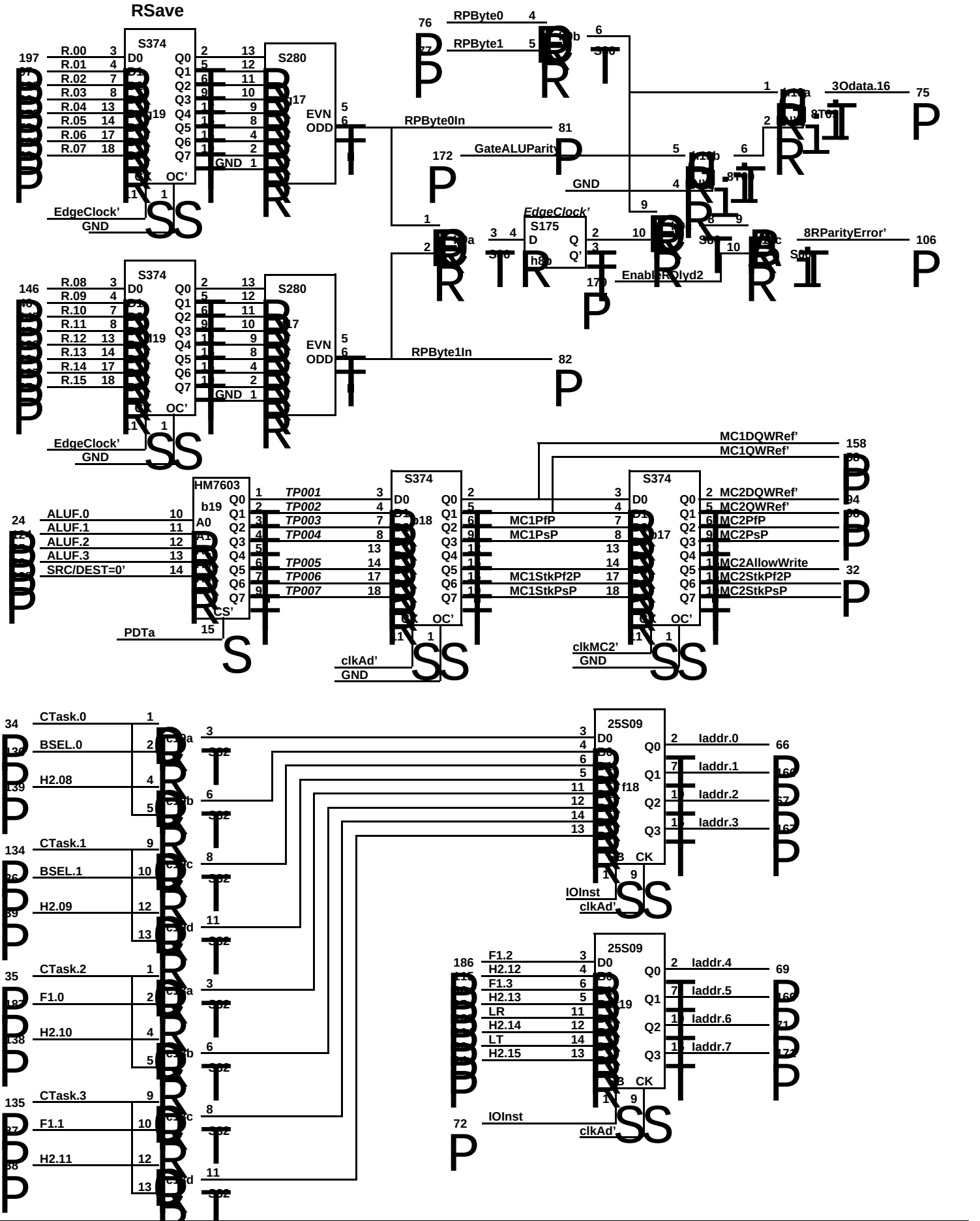
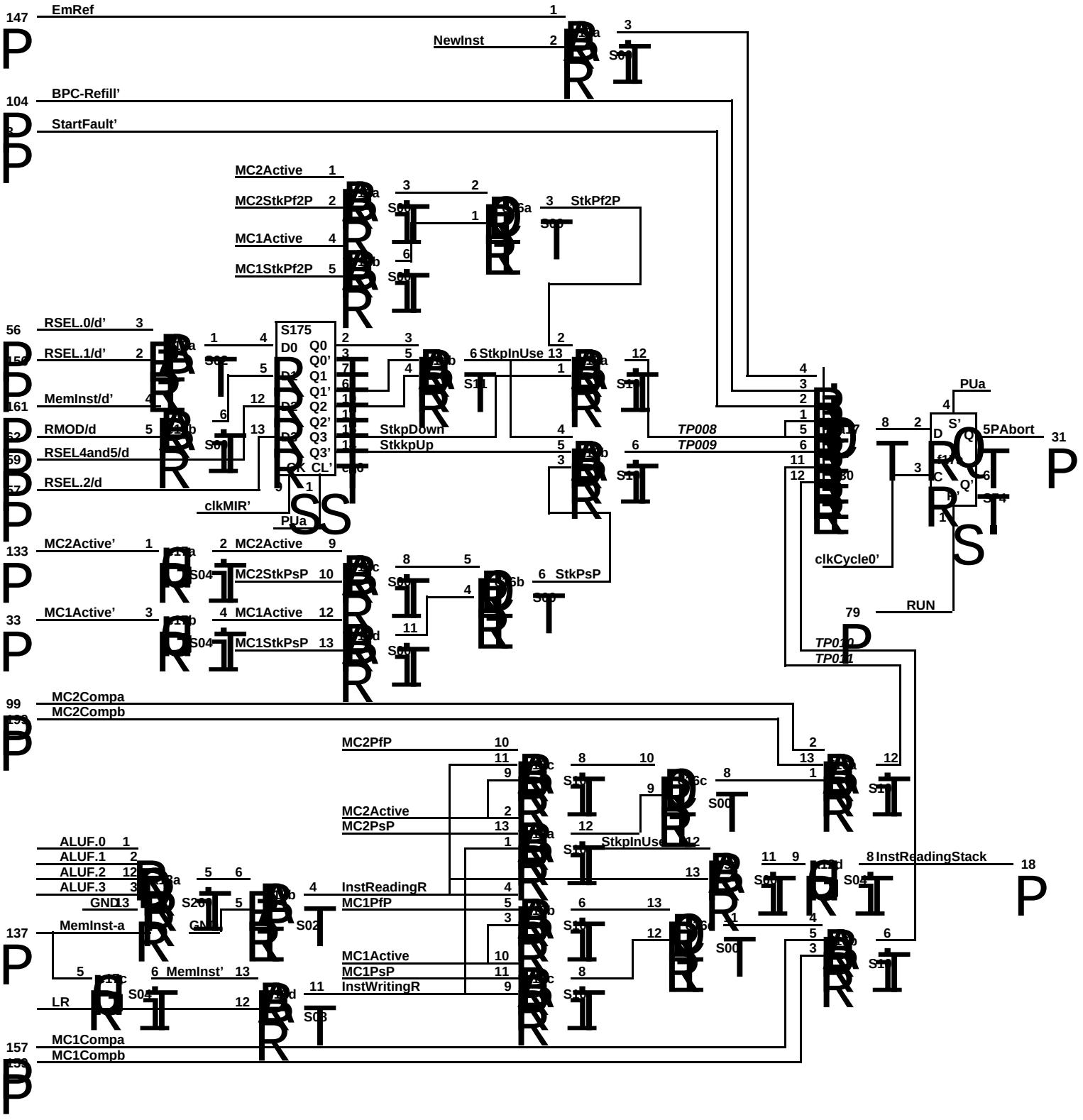
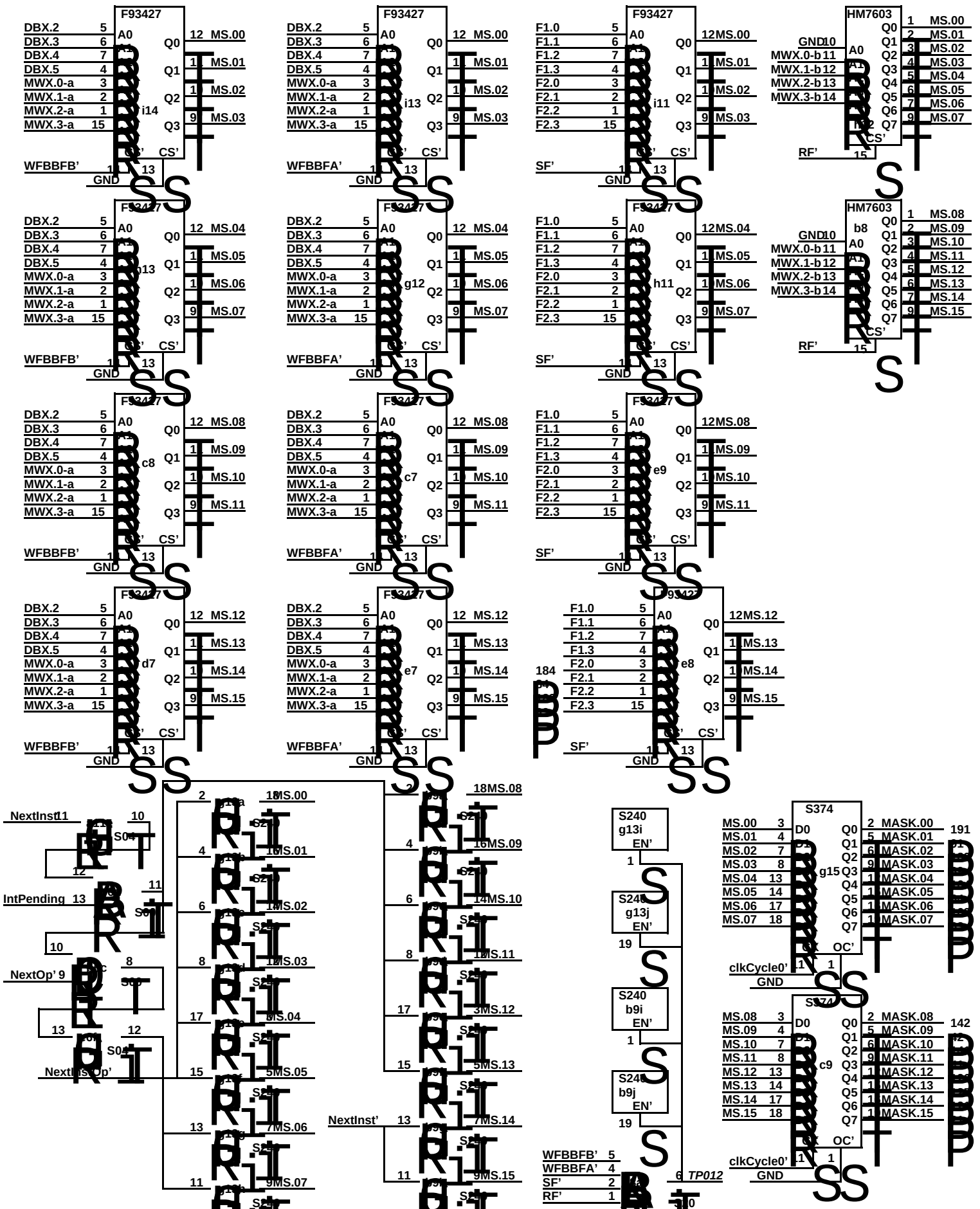


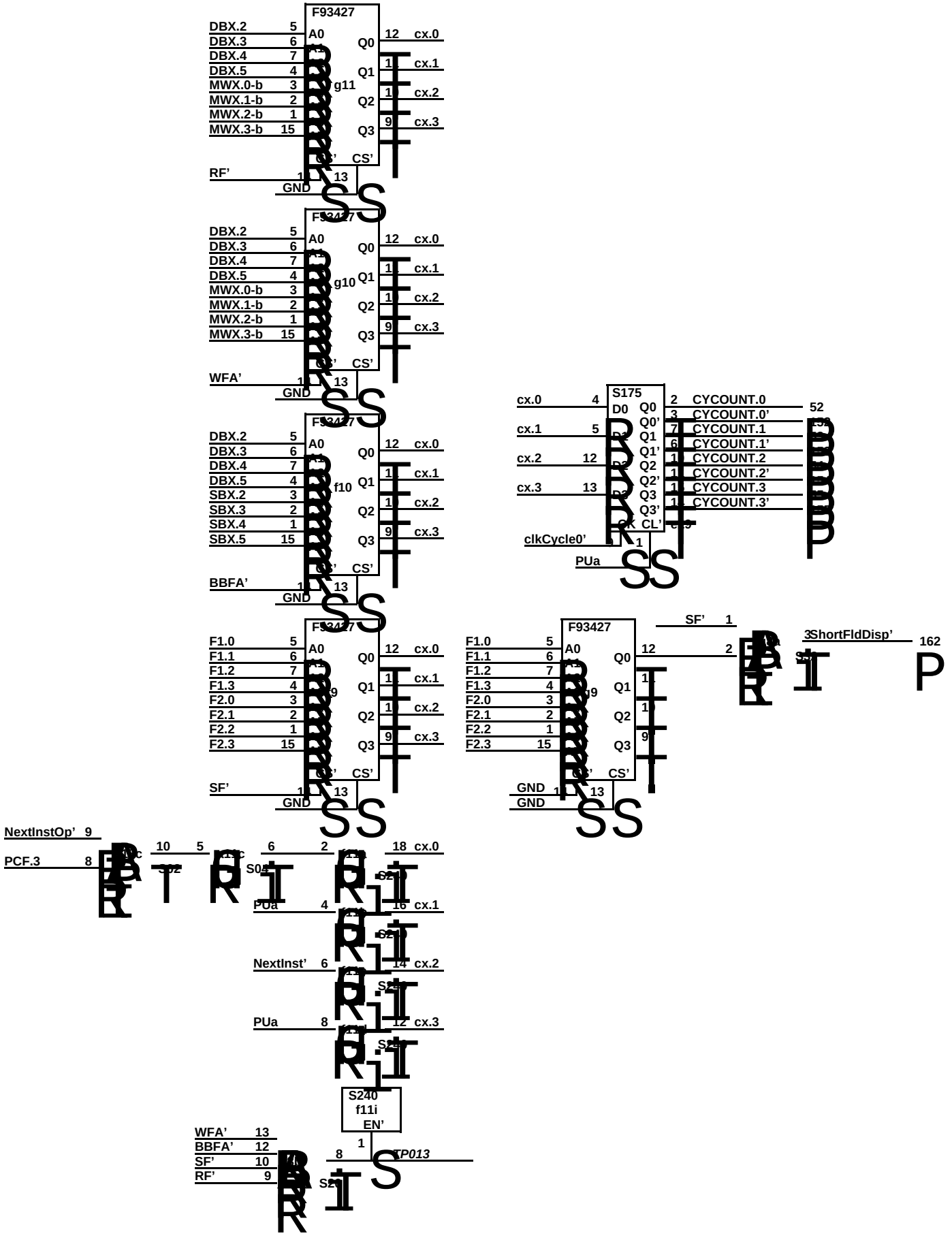
XEROX EOD	Project D0	R Parity, MemType, laddr	File d0Misc01.sil	Designer Thacker	Rev Go	Date 1/18/79	Page 01



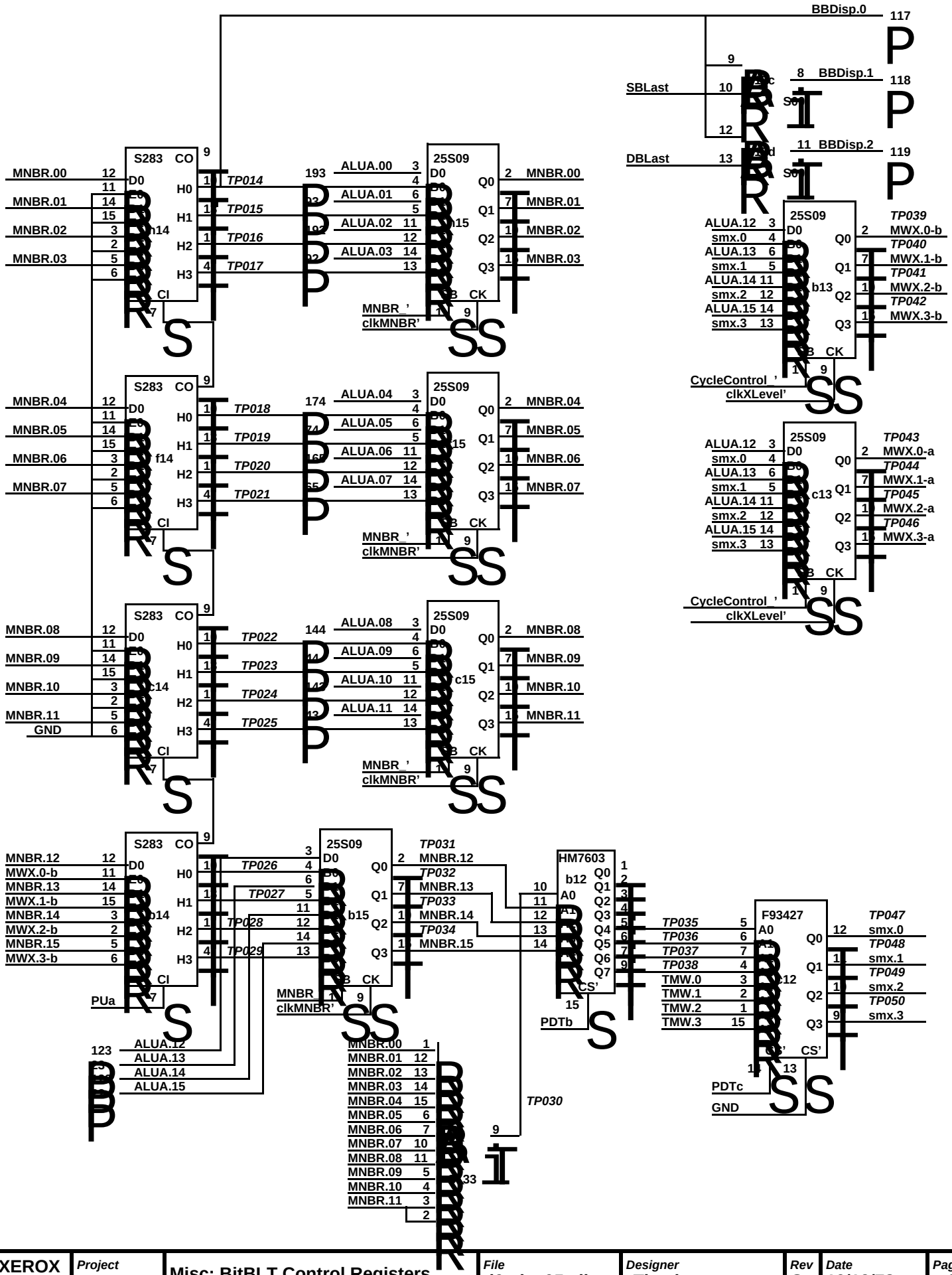
XEROX EOD	Project D0	Misc: Abort Logic	File d0misc02.sil	Designer Thacker	Rev Gc	Date 7/18/80	Page 02



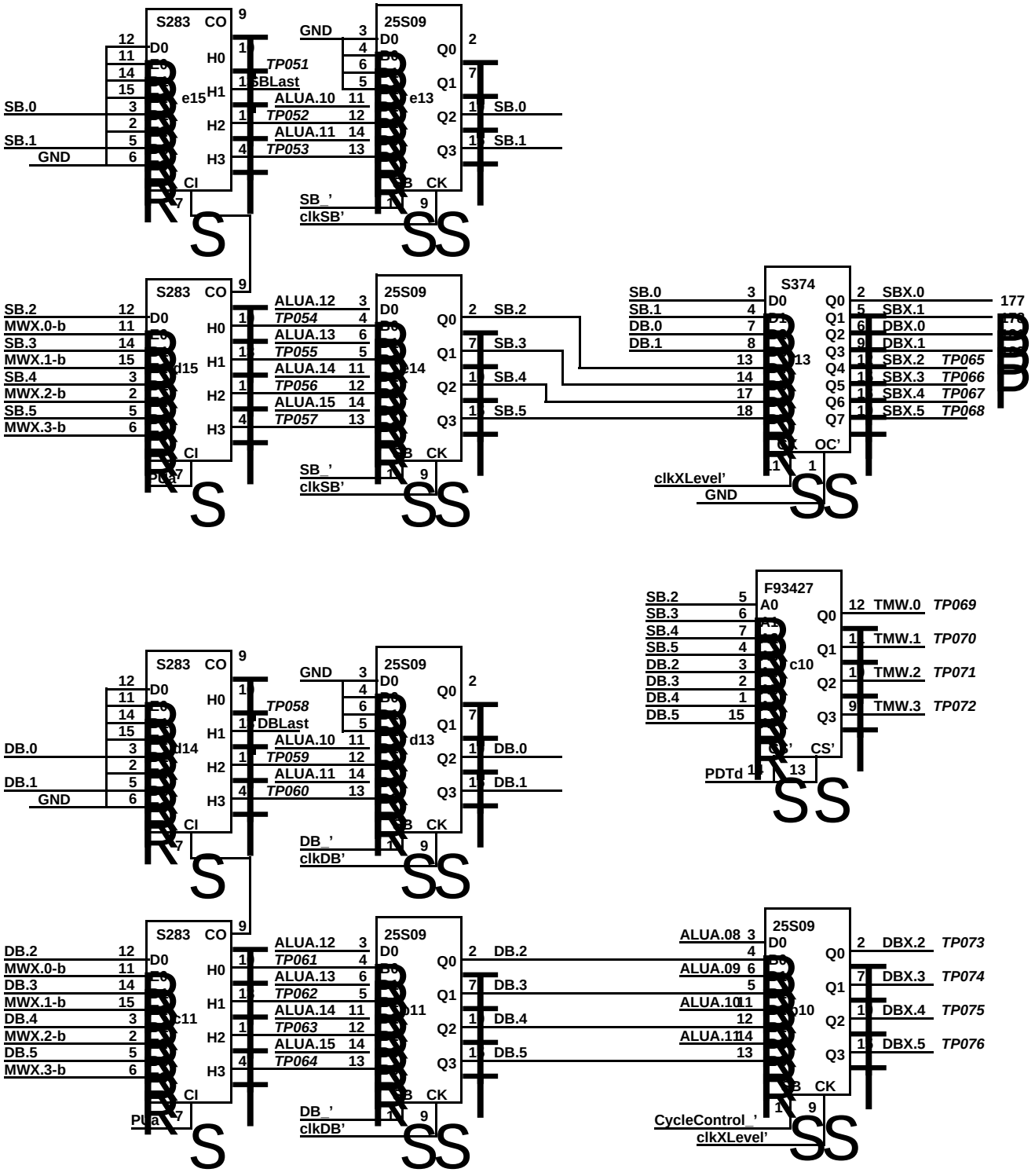
XEROX EOD	Project D0	Misc: Mask Generation	File d0misc03.sil	Designer Thacker	Rev Gc	Date 10/19/78	Page 03



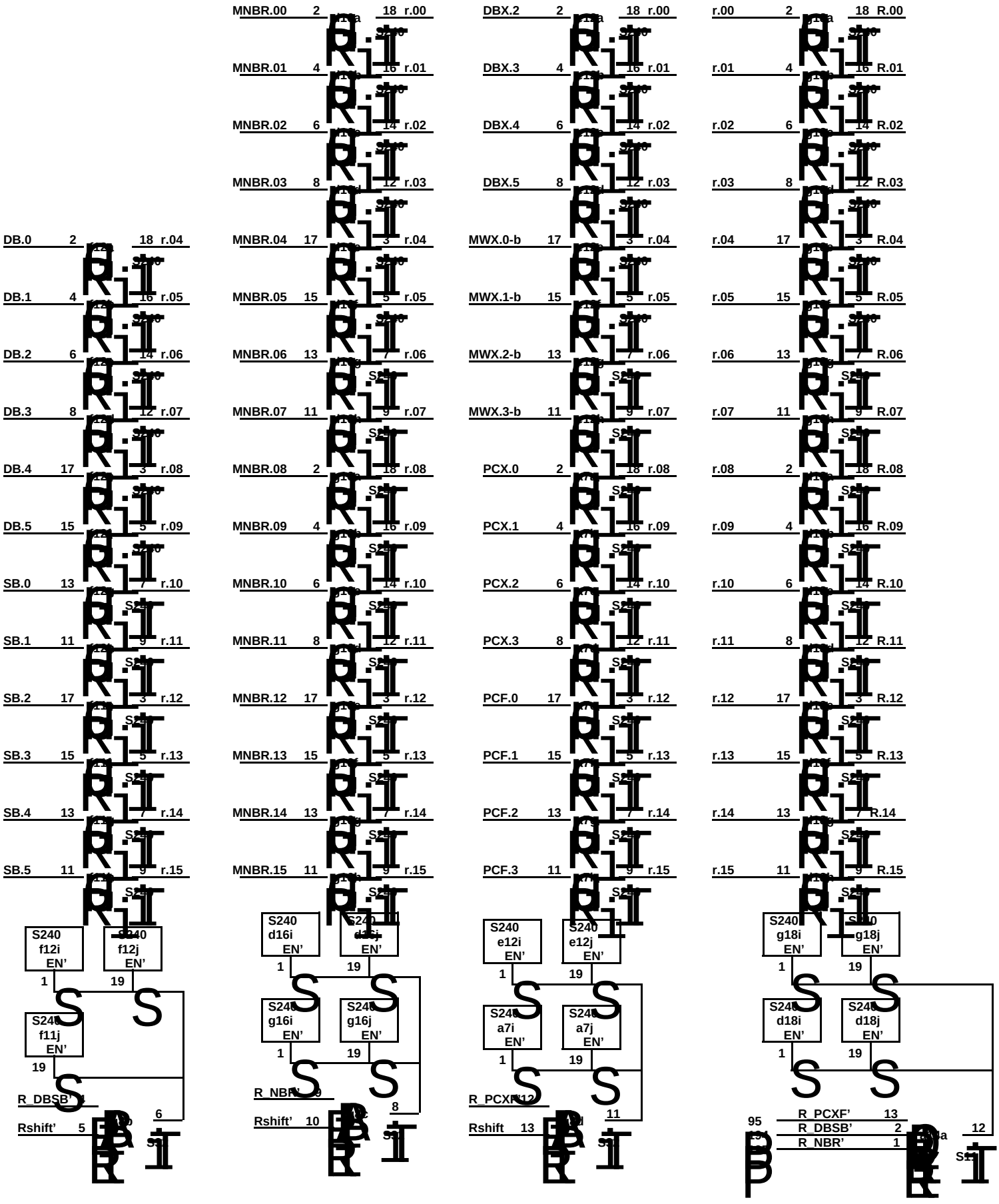
XEROX EOD	Project D0	Misc: Cycle Count Generation	File d0misc04.sil	Designer Thacker	Rev Gc	Date 8/9/78	Page 04



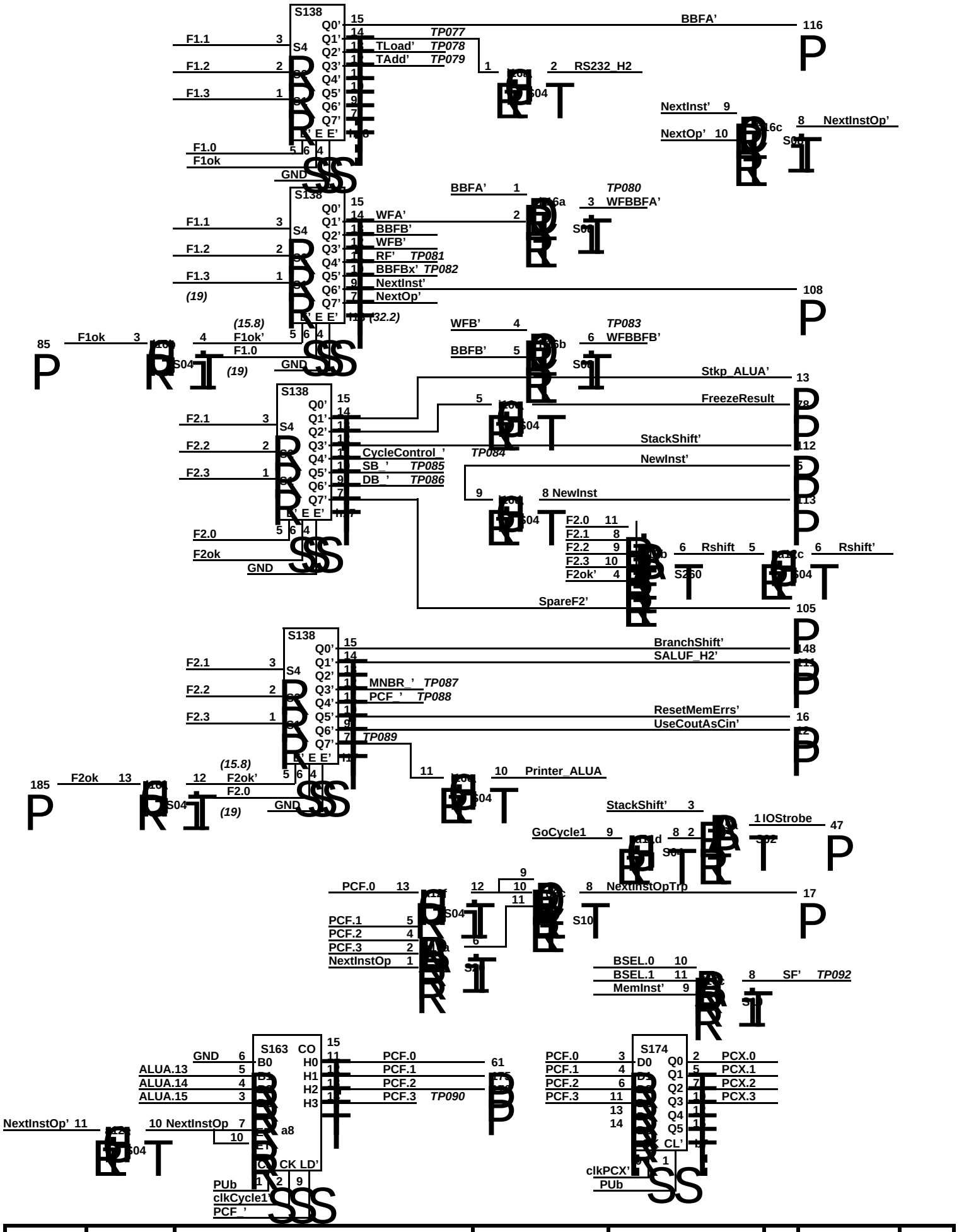
XEROX EOD	Project D0	Misc: BitBLT Control Registers	File d0misc05.sil	Designer Thacker	Rev Gc	Date 10/19/78	Page 05



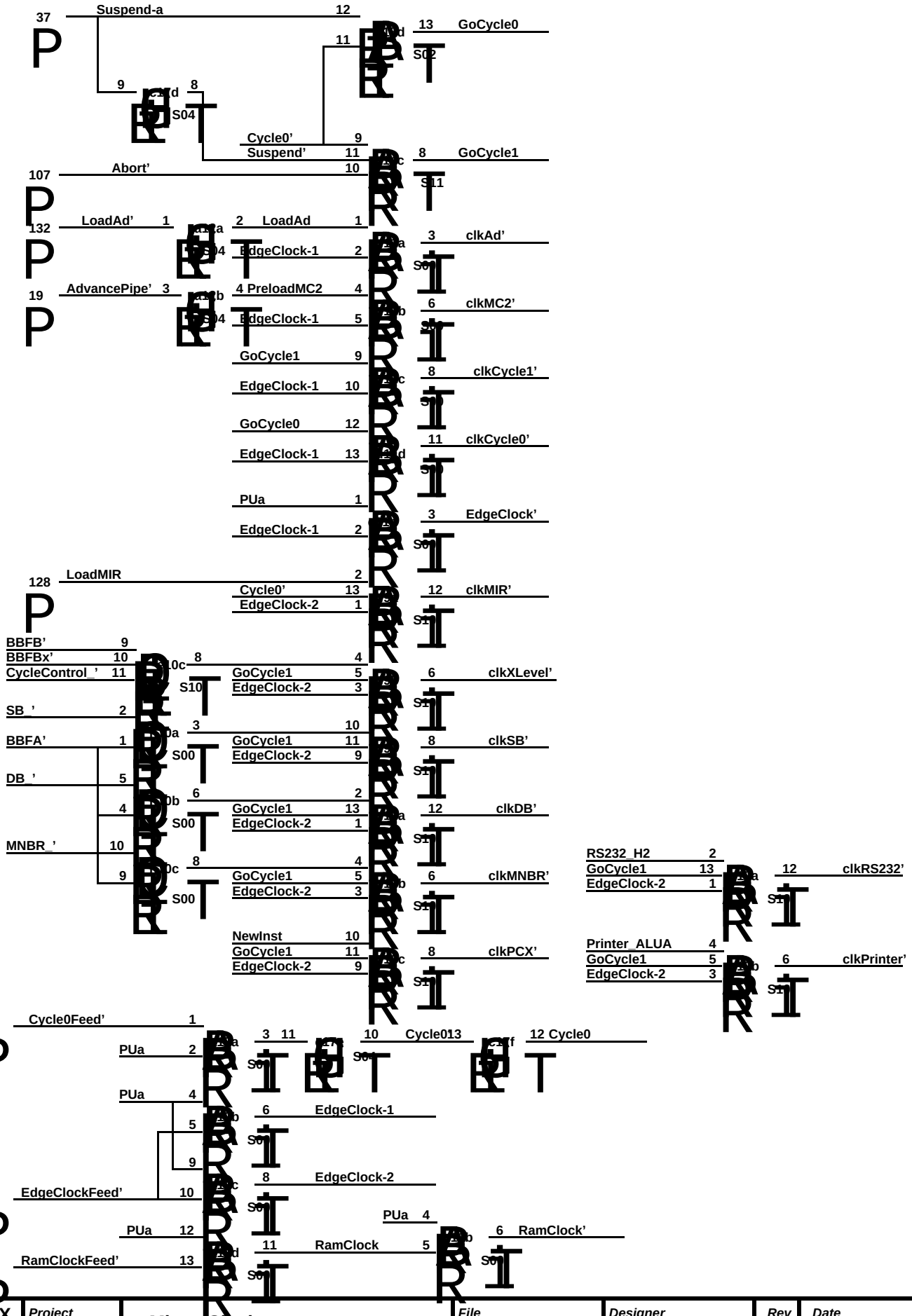
XEROX EOD	Project D0	Misc: BitBLT Control Registers	File d0misc06.sil	Designer Thacker	Rev Gc	Date 10/19/78	Page 06



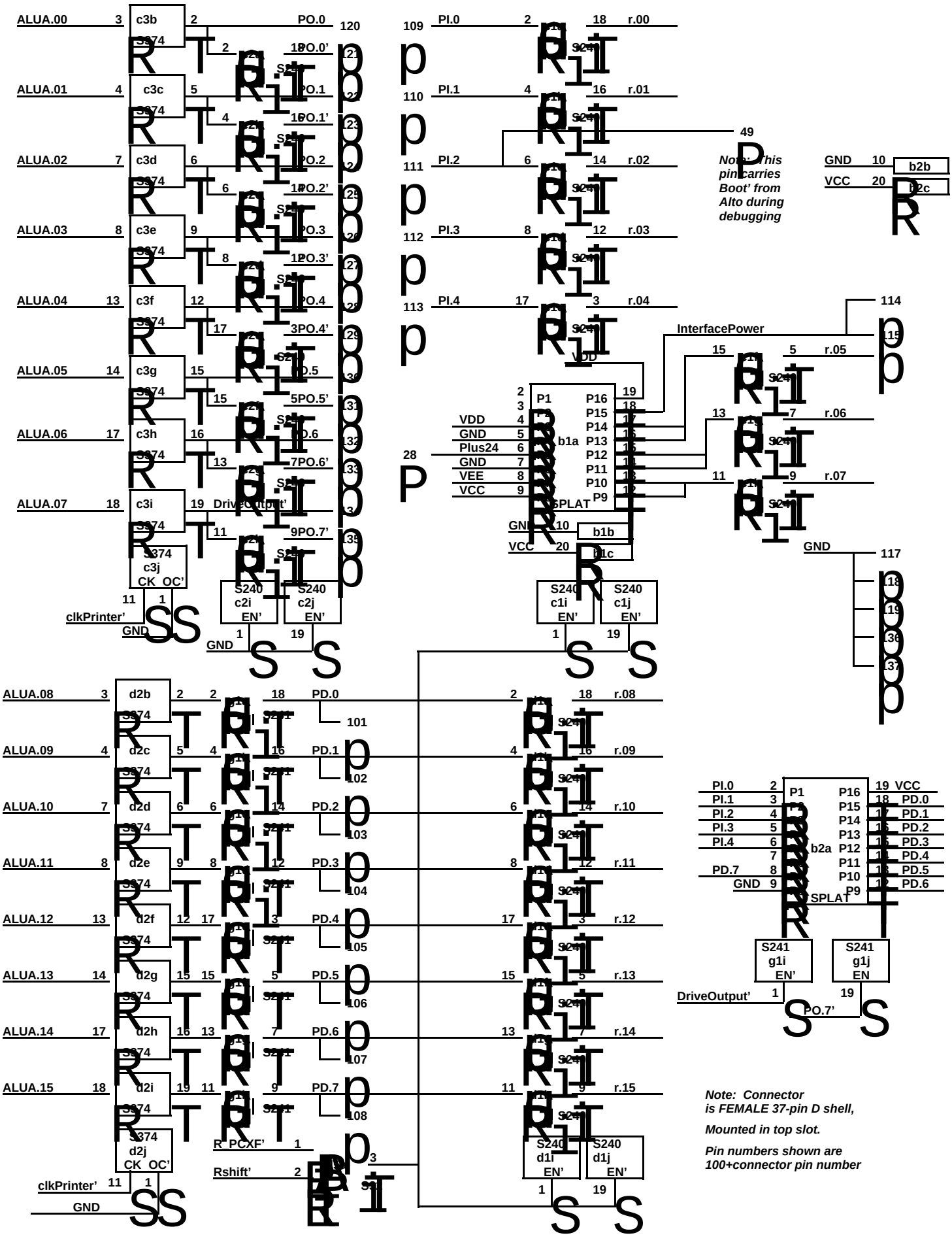
XEROX EOD	Project D0	Misc: R Sources	File d0misc07.sil	Designer Thacker	Rev Gc	Date 8/11/78	Page 07



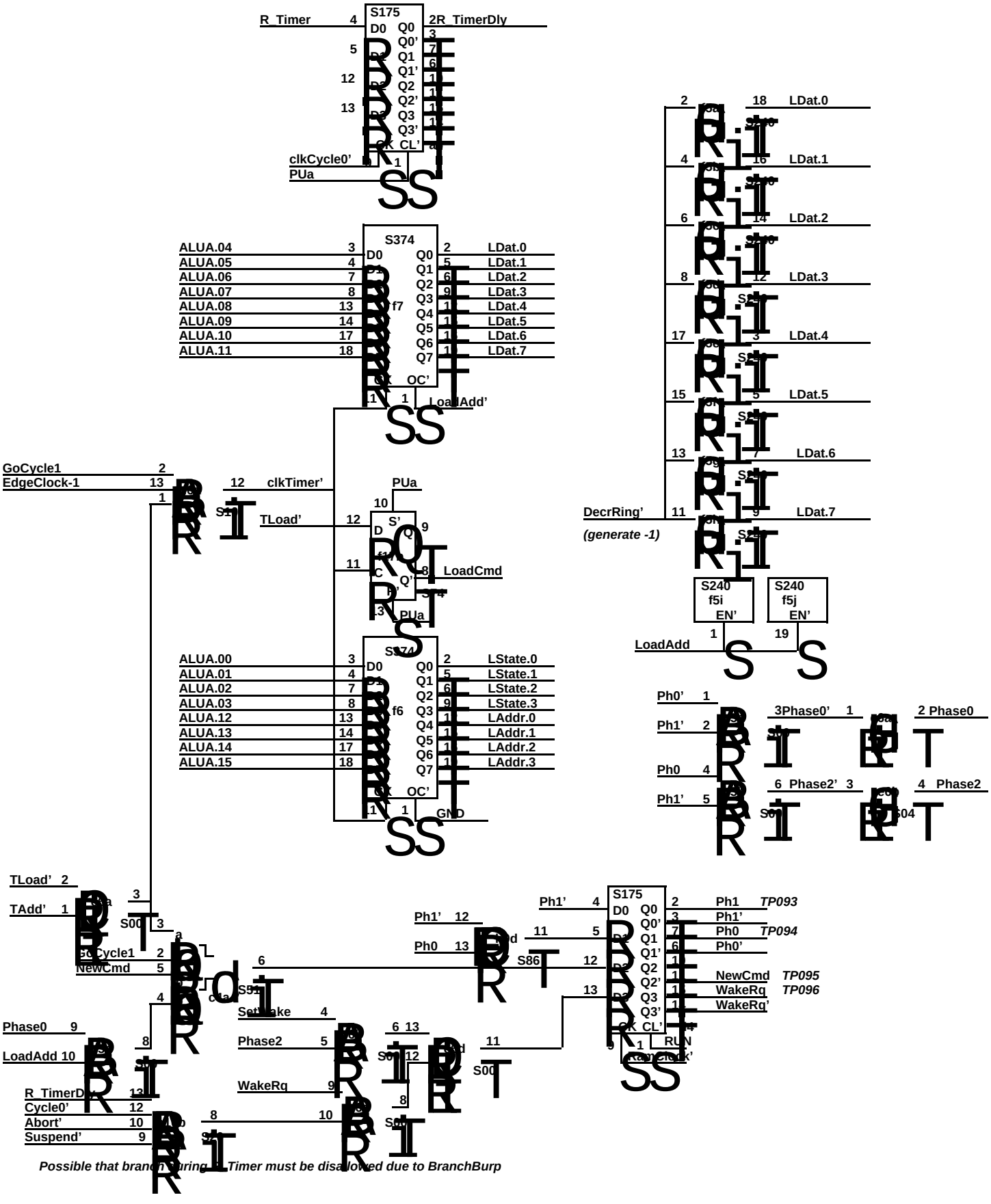
XEROX EOD	Project D0	Misc: F Decodes, PCF, PCX	File d0misc08.sil	Designer Thacker	Rev Gc	Date 1/4/79	Page 08



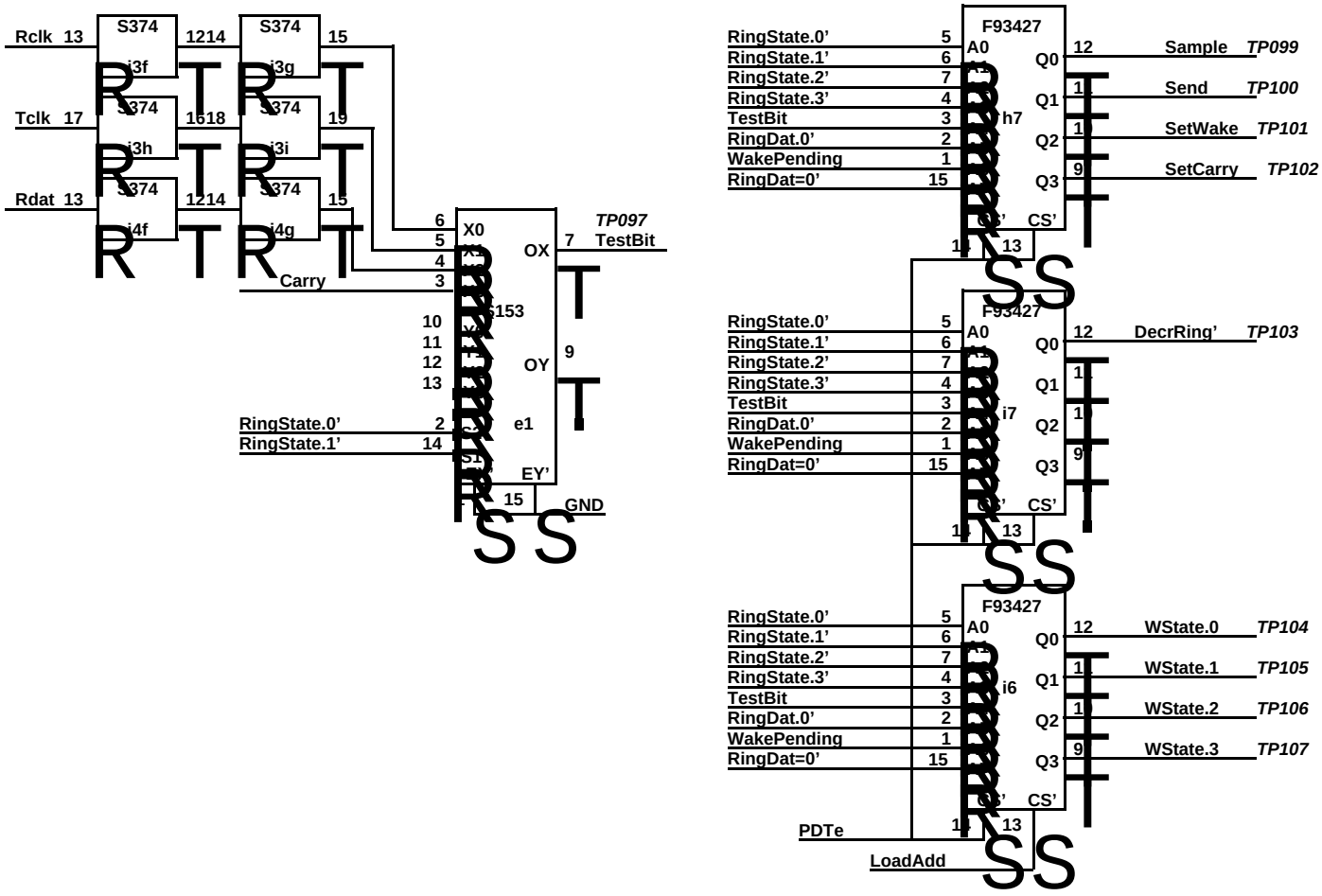
XEROX EOD	Project D0	Misc: Clocks	File d0misc09.sil	Designer Thacker	Rev Go	Date 8/11/78	Page 09



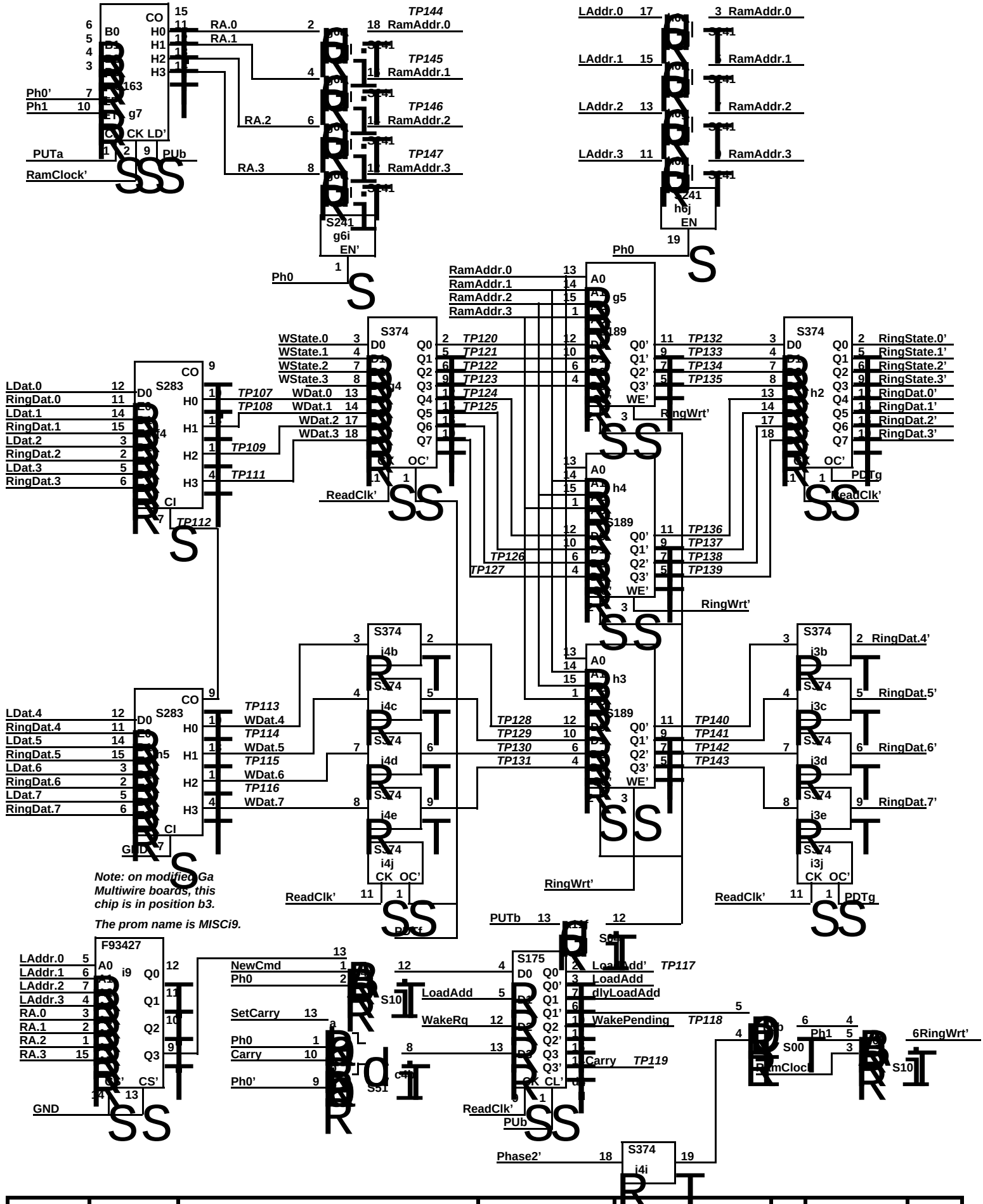
XEROX EOD	Project D0	Misc Board Printer Controller	File d0misc10.sil	Designer Rosen	Rev Gc	Date 1/18/79	Page 10



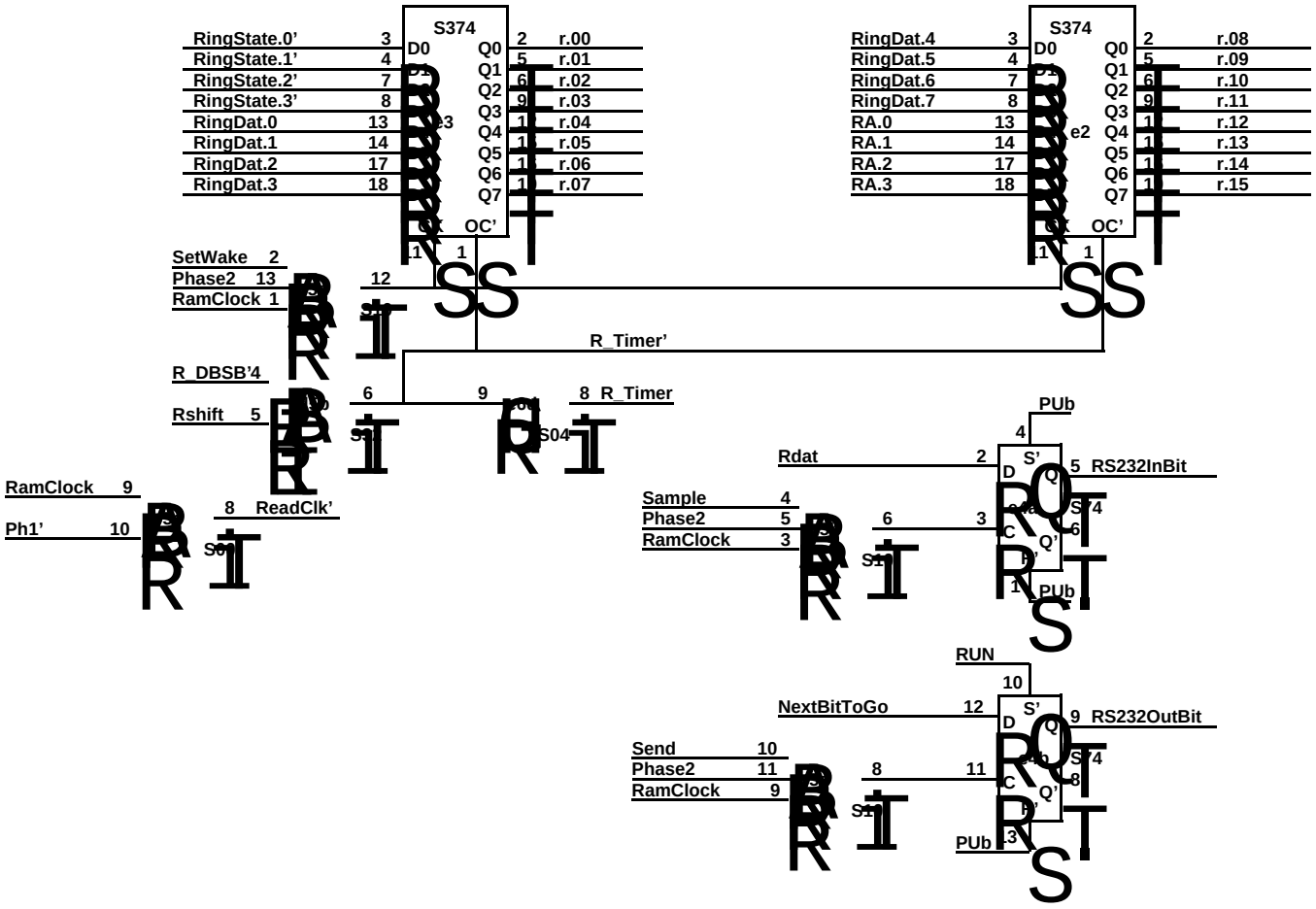
XEROX EOD	Project D0	Timers: Input Register	File d0misc11.sil	Designer L. MARTIN	Rev Gc	Date 8/9/78	Page 11

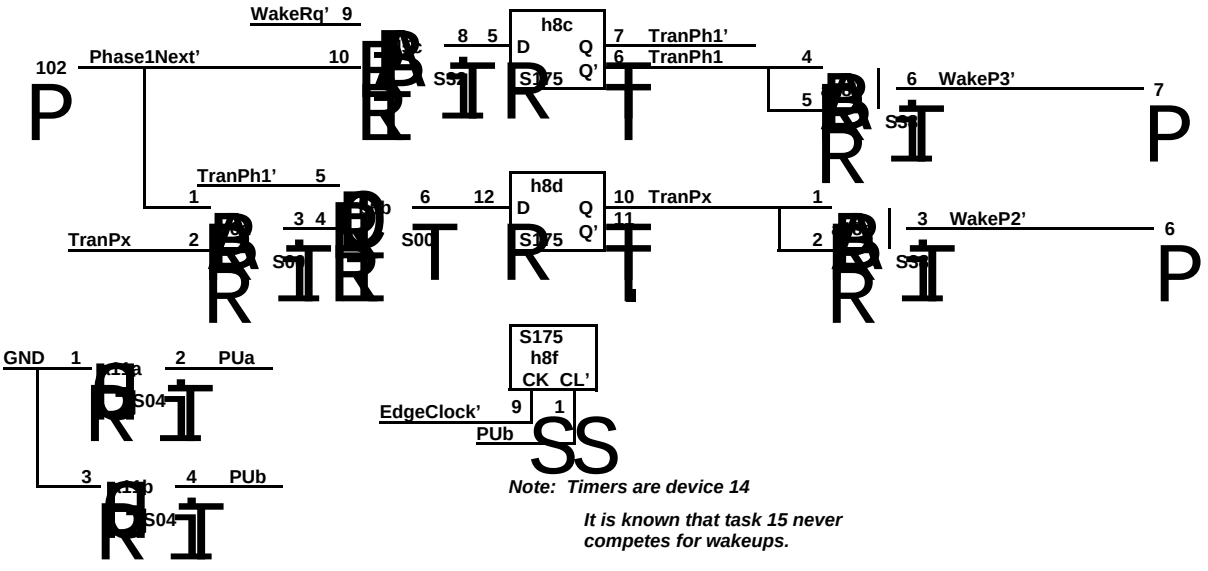


XEROX EOD	Project D0	Timers: Data Control	File d0misc12.sil	Designer L. MARTIN	Rev Gc	Date 1/18/79	Page 12



XEROX EOD	Project D0	Timers: Ring Ram and Addressing	File d0misc13.sil	Designer L. MARTIN	Rev Gc	Date 10/21/79	Page 13

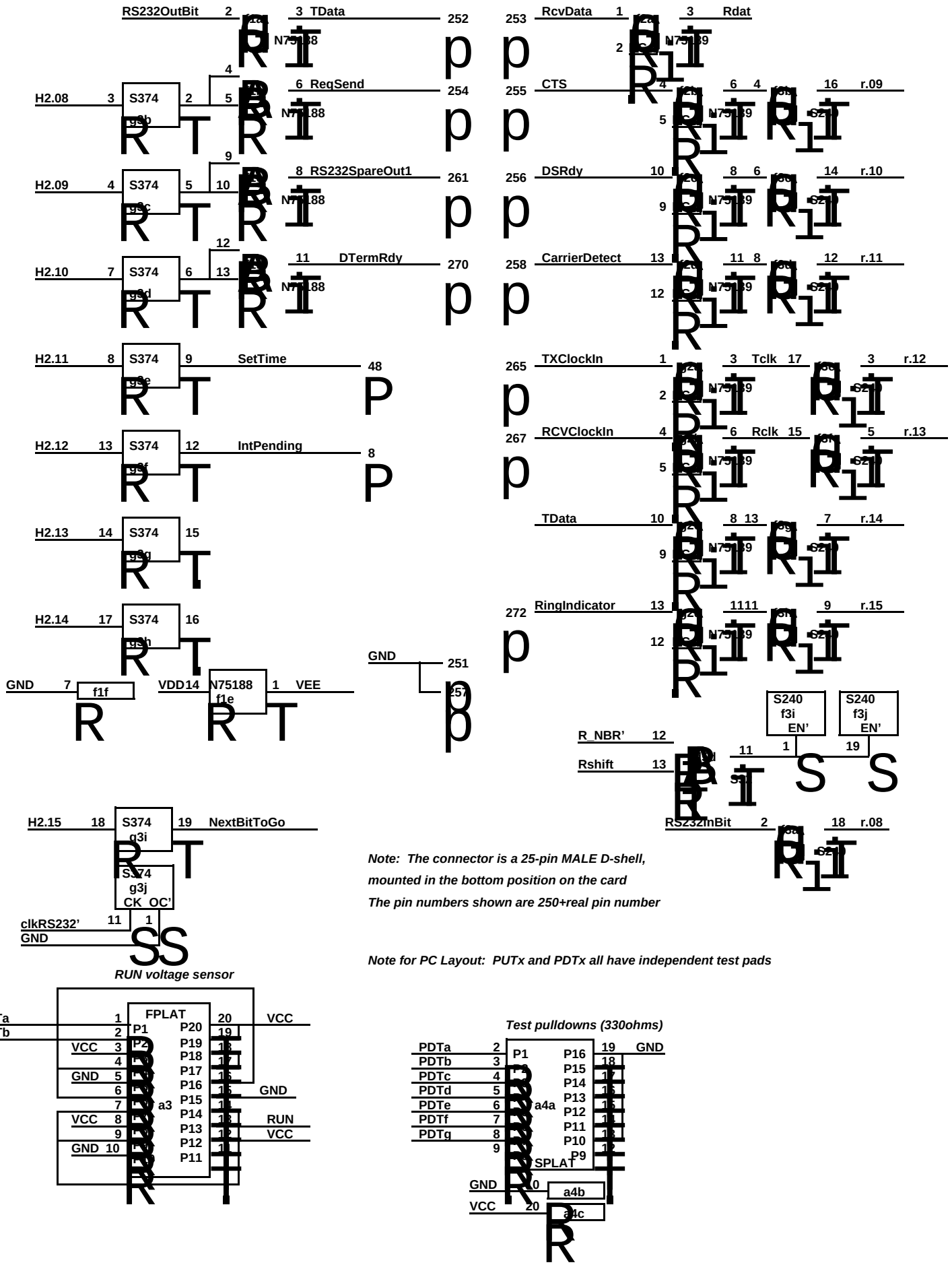




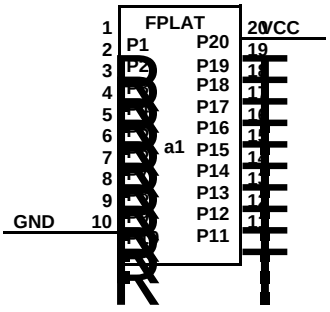
Note: Timers are device 14

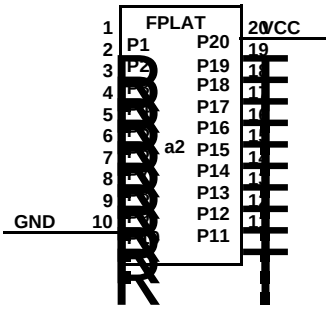
It is known that task 15 never competes for wakeups.

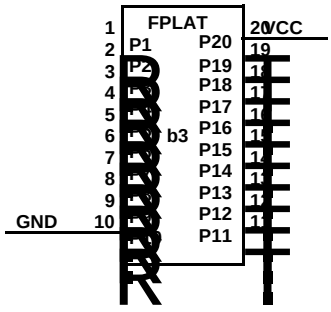
XEROX EOD	Project D0	Timers: Output,Logic,Wakeups	File d0misc14.sil	Designer L. MARTIN	Rev Gc	Date 2/6/78	Page 14

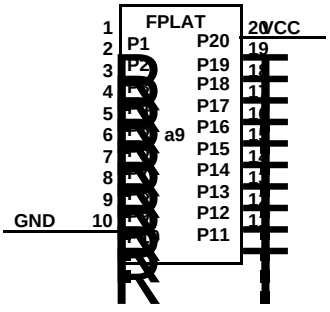


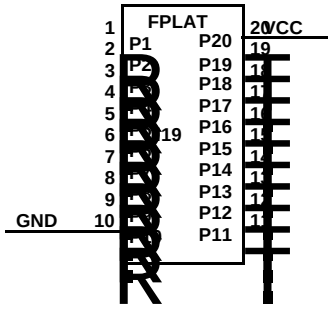
XEROX EOD	Project D0	Misc: RS232 Interface	File d0misc15.sil	Designer Thacker	Rev Gc	Date 10/20/78	Page 15











XEROX EOD	Project D0	Misc: Spare IC's	File d0misc16.sil	Designer Thacker	Rev Gc	Date 10/14/79	Page 16

Changes for Rev E to Rev F (8/11/78, C. Thacker)

1) Added signal GateALUParity and inverter to receive it (Pg 1).
2) Deleted signal MC2EnableRP' (Pg 1).
3) Added S02 at i15a to form IOStrobe (Note: earlier E-1 revision generated this signal incorrectly) (Page 8)
4) Connected RS232 drivers f1 and g1 to VEE (-5.2V) supply (Page 15).

Changes for rev F to rev G (10/17/78 - C. Thacker)

1) Reduced number of outbound RS232 lines to 4. Looped RS232 data back on R.14. Added SetTime as bit 11 in the output register (goes to E48). Added IntPending as bit 10 of the register. All changes on pg 15.
2) Terminated PI.0 - PI.4. Used R bus drivers PI.5-7 for voltage monitors.
3) Added a11e, b6d, b6c, e6f on pg 3 to cause IntPending to dispatch to Opcode0 on interrupt.
4) Added test pullups and pulldowns.
5) Added +5 monitor at a3 (pg 15) to control RUN.

Changes for rev G to rev H (1/4/79 - C. Thacker)

1) Brougnt signal InstReadingR to E018 (pg 2).
2) h17 pin 7 was NewInst', is now SpareF2, connected to E105
3) NewInst' is now connected to E005 rather than to h17.7.
   Note: Control boards with revision <I must have E005 jumpered to E105 on the backplane.
4) Removed the time-to-task counter (a9) and freed inverter a12d (pg8).
5) Terminated PD.0-7 with splat (R-pack) at b2
6) Added InterfacePower signal (short-circuit protected +12V) to Printer Interface connector

Changes for rev H to rev I (1/18/79 - C.T)

1) Changed layout - g1 is S241, not 75188
2) Modified platforms b1, a3.
3) (pg 1) b17.1 is GND, not PDTf.
4) (pg 10) b1.9 is VCC, not GND
5) (pg 10) Added S241 driver for PD.0-PD.7. (note - early etch boards will NOT have this change)
6) (pg 12) i6.14 is PDTe, not LoadAdd
7) (pg 13) i4.1 is PDTf, not GND

Changes for rev I to rev J (1/31/79 - CT)

1) Changed E18 from InstReadingR to InstReadingStack (pg2). Corrects a bug in overflow checking

Note: Revision J = Revision Ga

Changes for revision Ga to revision Gb (10/14/79 by CT). Fixes interval timer inaccuracy.

Note: This change comes in two flavors: Revision Ga multiwire boards have 2 extra IC's mounted in spare positions b3 (93427) and b4 (74S10). In the Multiwire Gb version, the S10 is in position b4, but the 93427 replaces the S85 in position i9. The logic diagrams show the revision Gb multiwire version of the change. To modify a revision Ga multiwire board, proceed as follows:

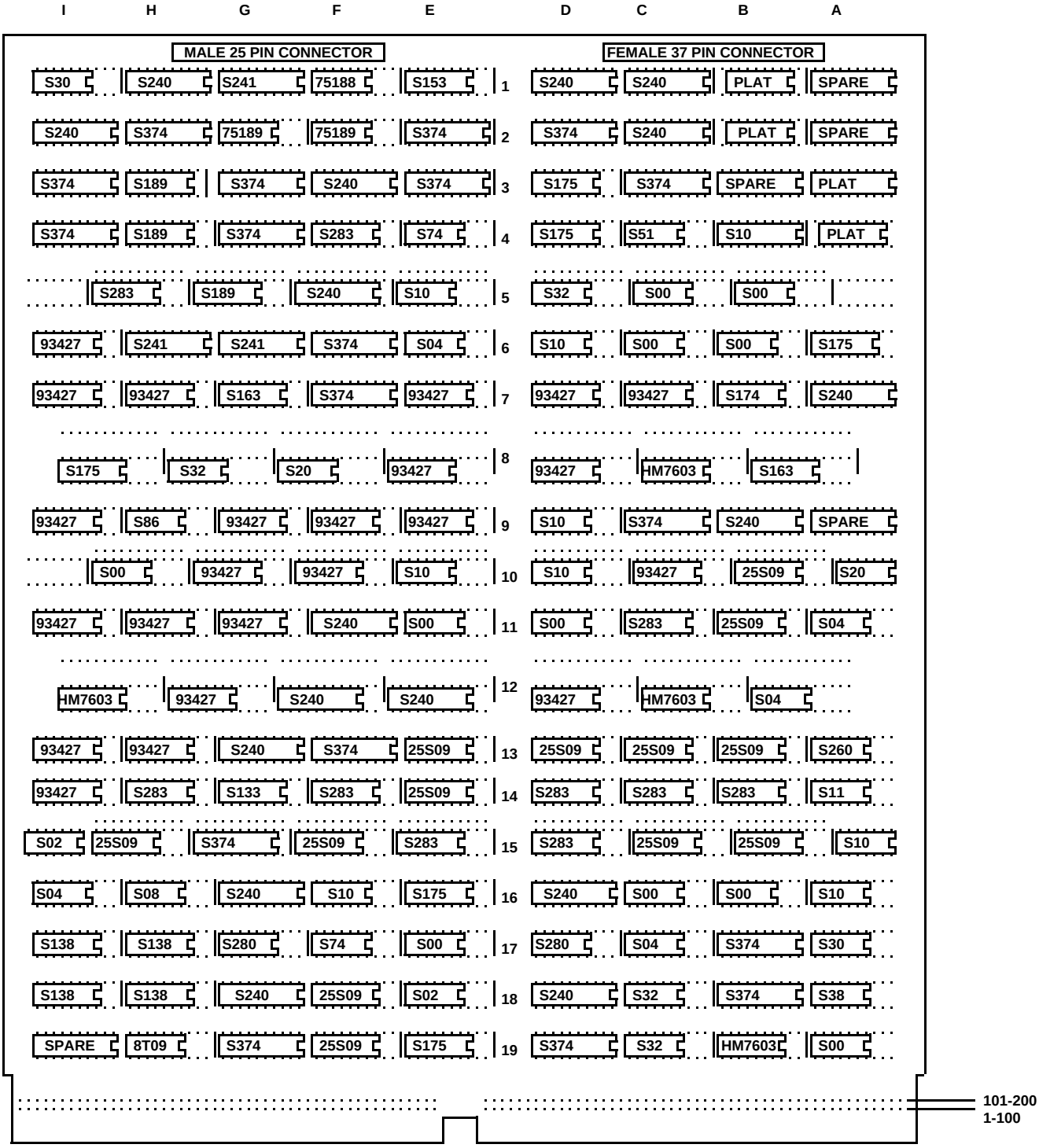
In the steps below, pin numbers are those of the chips, not those of the 20 pin sockets used to hold the chips. Chip b4 is mounted with pin 7 in pin 10 of the 20 pin pattern, b3 is mounted with pin 8 in pin 10 of the 20 pin pattern. All wiring is to be done on the back (non-component) side of the board.

1) Add an S10 in position b4 and wire b4.14 to pin 20 of the pattern (Vcc).
2) Add a 93427 (programmed) in position b3, and wire b3.16 to pin 20 of the pattern (Vcc).
3) Lift pins b5.1, b5.2, and b5.3.
4) Remove chip i9 and jumper i9.6 to i9.8
5) Add b5.1 to b4.1
6) add b5.2 to b4.2
7) add b5.3 to b4.12
8) add b3.14 to b3.13 to b3.8
9) add b3.5 to f6.12
10) add b3.6 to f6.15
11) add b3.7 to f6.16
12) add b3.4 to f6.19
13) add b3.3 to e2.13
14) add b3.2 to e2.14
15) add b3.1 to e2.17
16) add b3.15 to e2.18
17) add b3.9 to b4.13

Changes for revision Gb to Gc (7/17/80 - CPT)

1) e18.5 _ gnd (pg. 2) This causes memory reference instructions to interlock when referencing base registers

XEROX PARC/CSL	Project D0	Title D0 MISC board Changes	File D0MISCChanges.sil	Designer Thacker	Rev Gc	Date 7/17/80

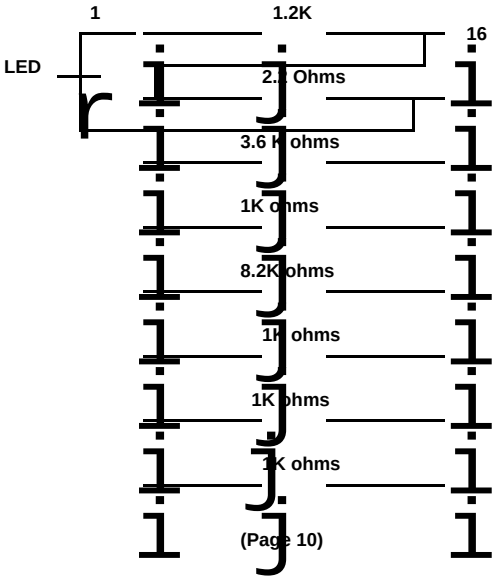


20pins: A 16pins: B 14pins: C 22pins: D 24 pins: E

Note: The short vertical lines indicate filter capacitor locations.

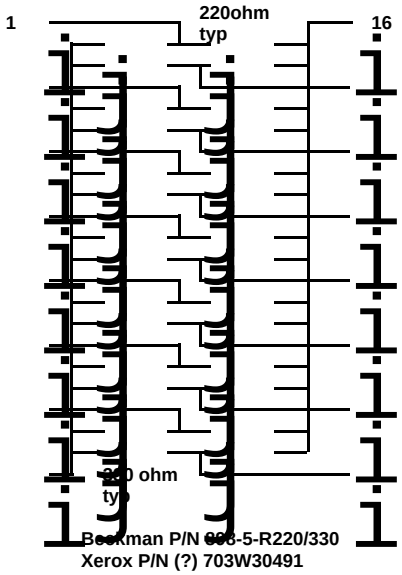
XEROX CSL	Project D0	D0 Misc Board	File D0MiscLayout.sil	Designer Thacker	Rev Gc	Date 7/17/80

SPLAT at b1



(Page 10)

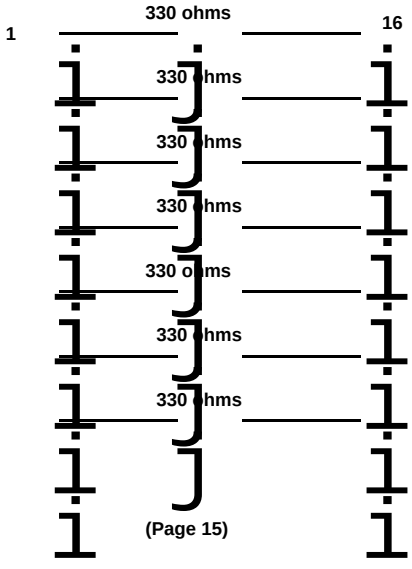
SPLAT b2



Beckman P/N 898-5-R220/330
Xerox P/N (?) 703W30491

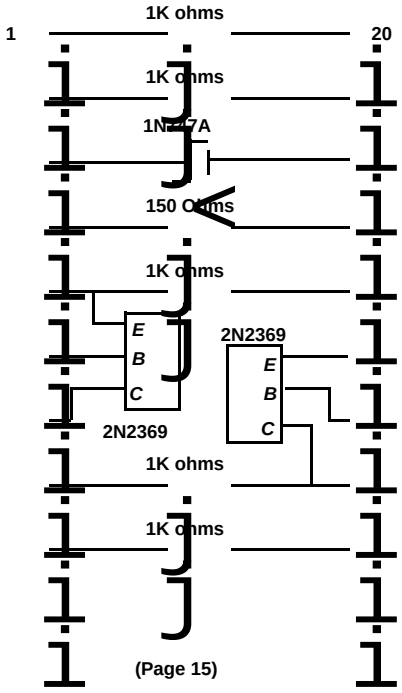
(Page 10)

SPLAT at a4



(Page 15)

FPLAT a3



(Page 15)

XEROX EOD	Project D0	D0 MISC Board PlatForms	File D0MiscPlatforms.sil	Designer Thacker	Rev Gc	Date 7/17/80