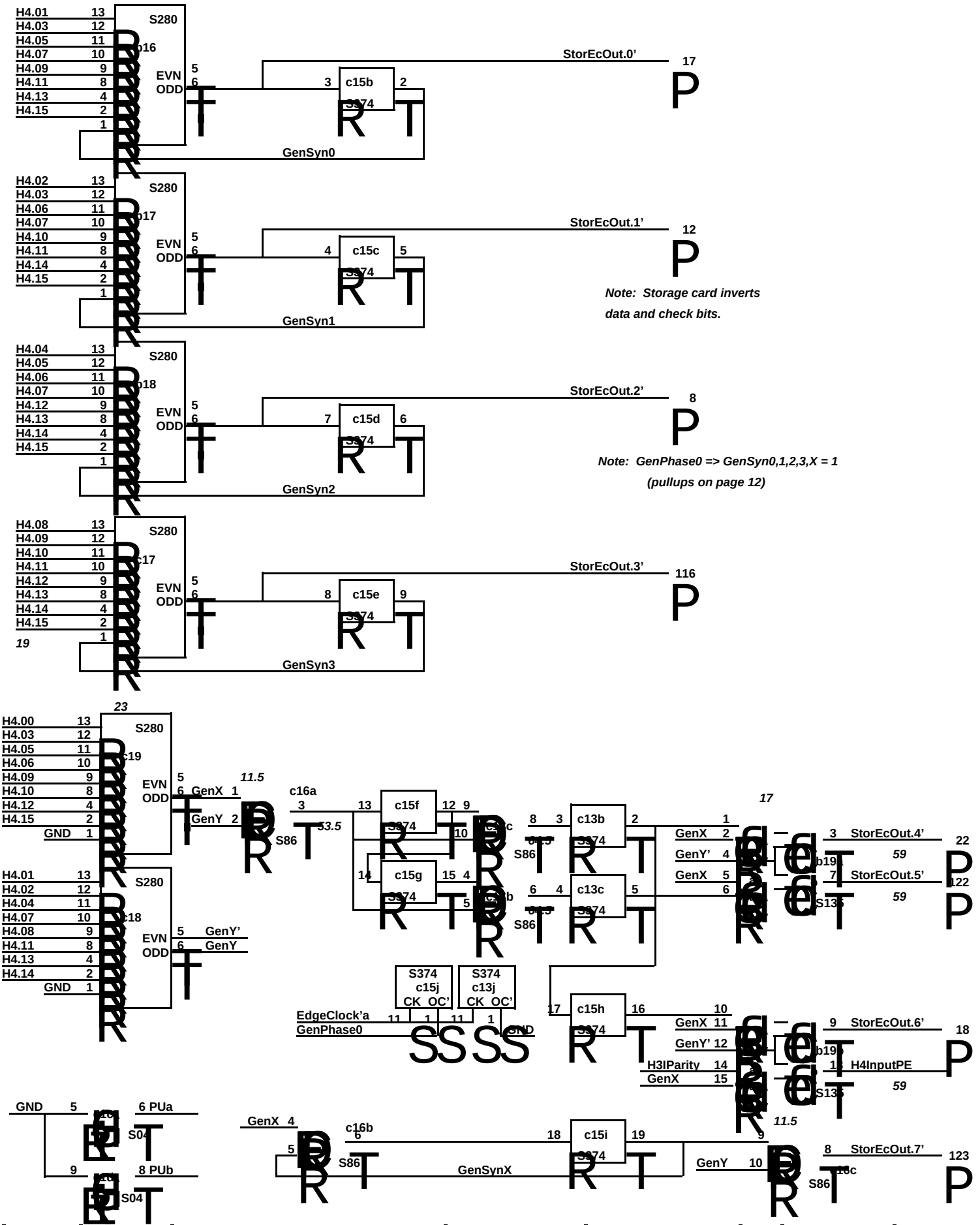
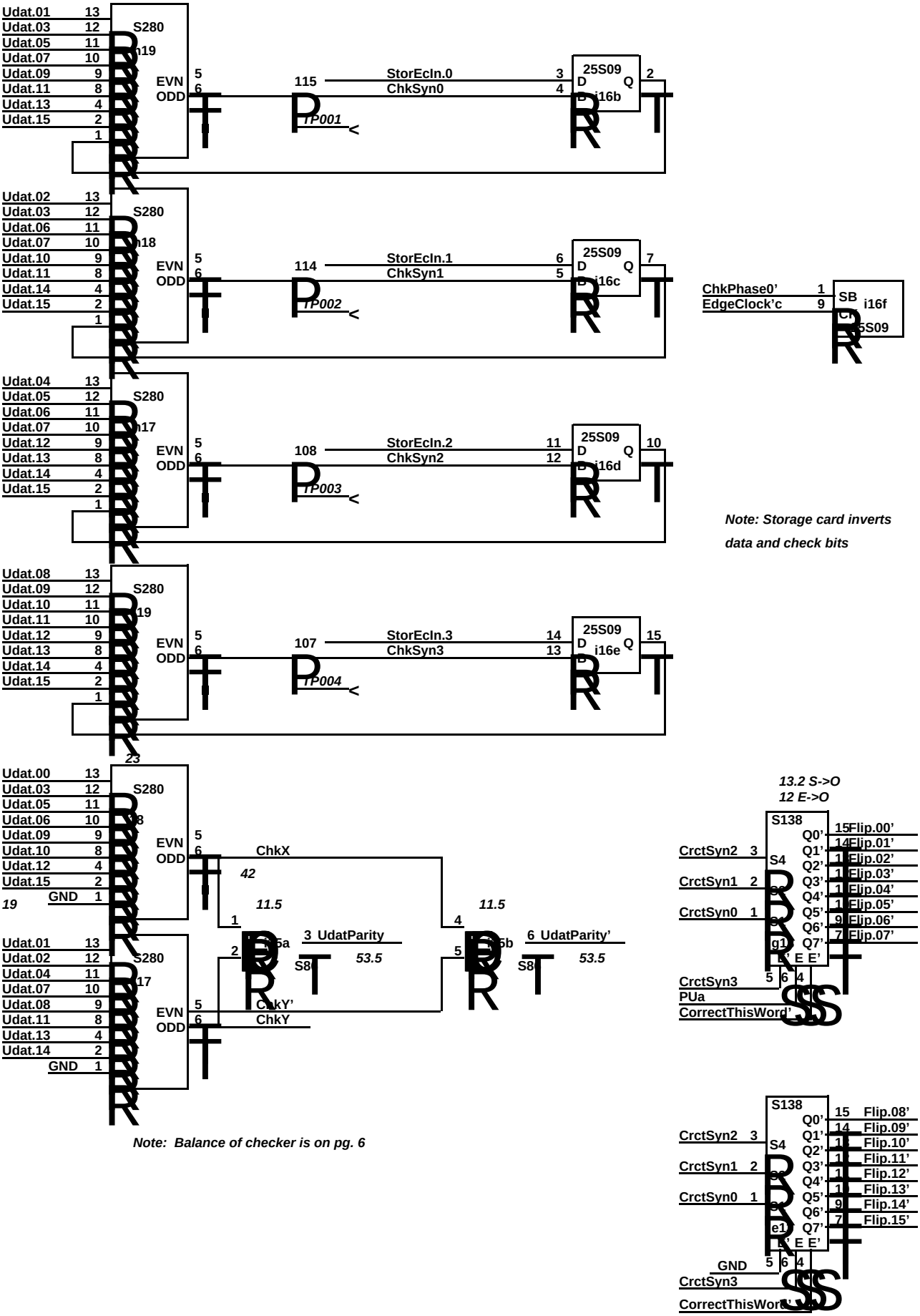


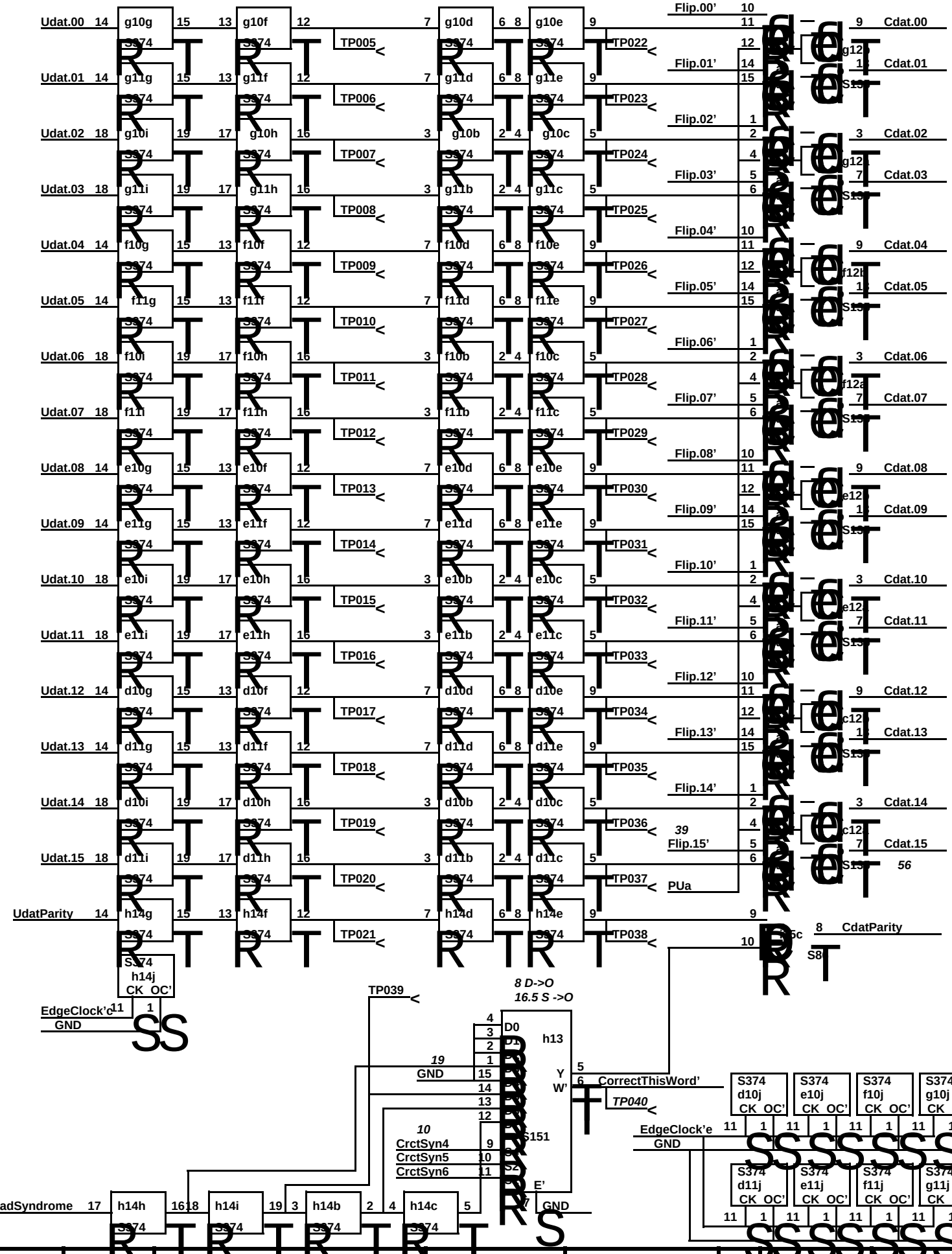
XEROX EOD	Project D0	Memory Control Error Correction Generator	File D0mem01.sil	Designer Thacker	Rev Gb	Date 7/18/80	Page 01

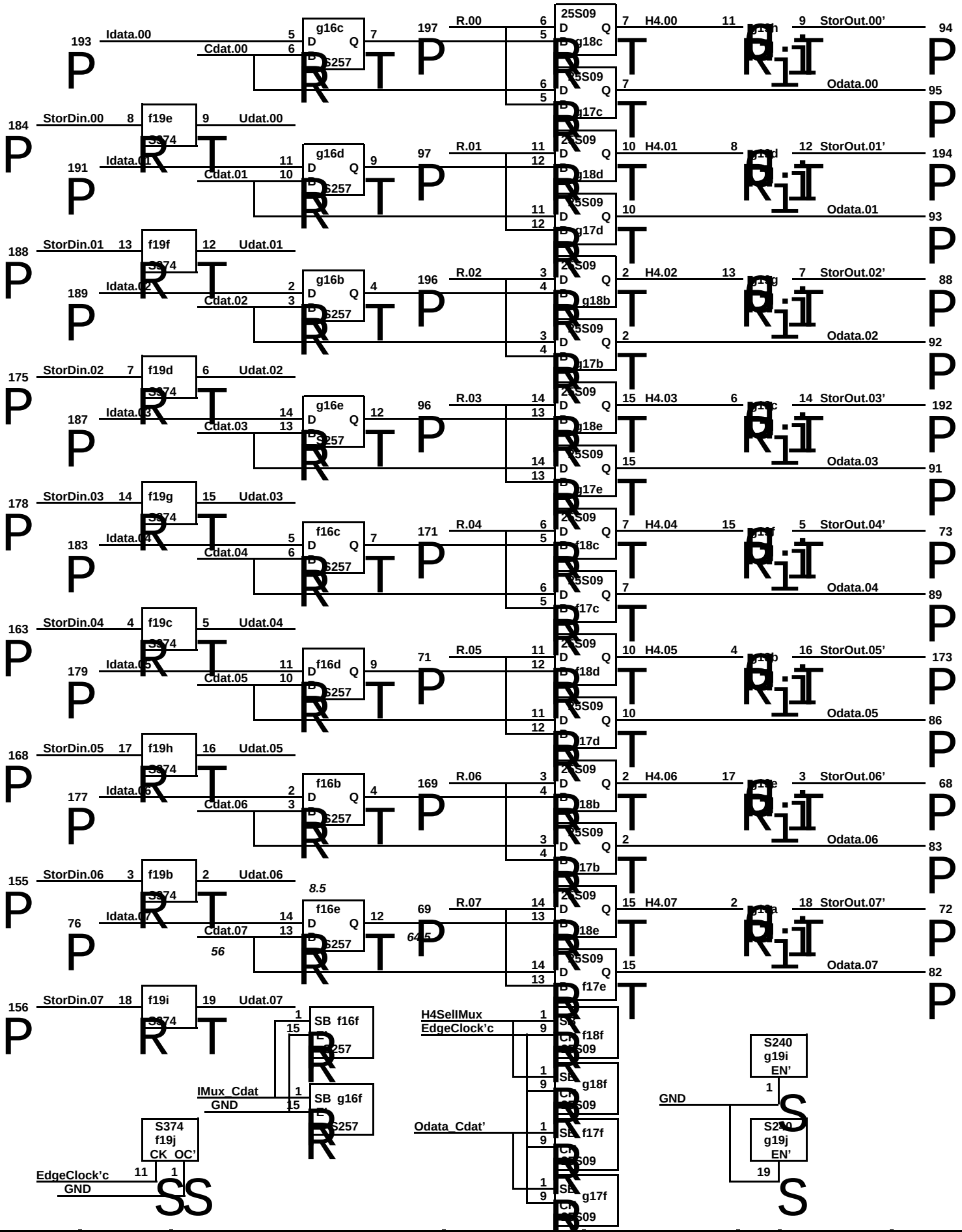


Note: Storage card inverts data and check bits

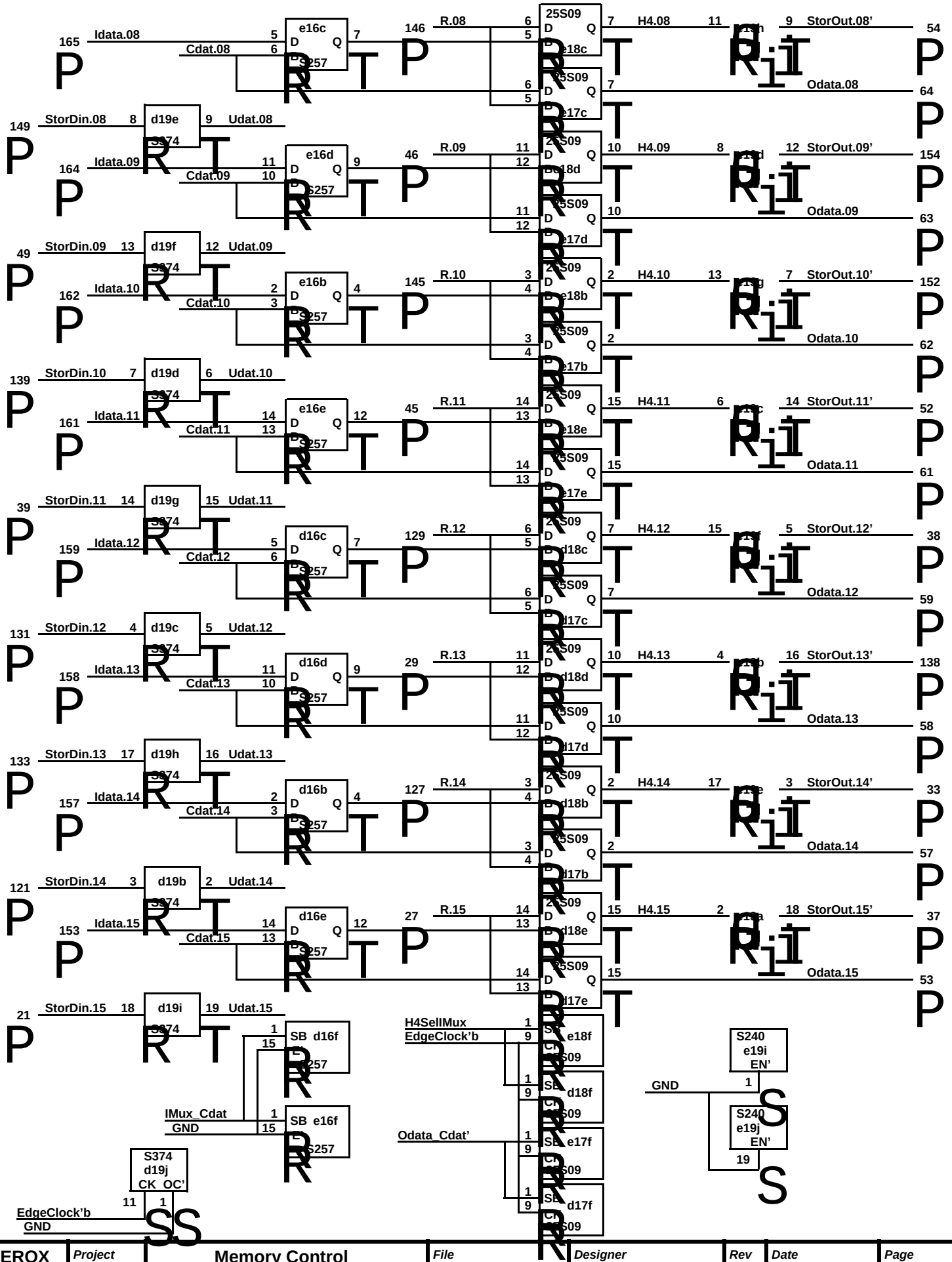
Note: Balance of checker is on pg. 6

XEROX EOD	Project D0	Memory Control Error Correction Checker	File D0mem02.sil	Designer Thacker	Rev Gb	Date 8/13/78	Page 02


Udat.00
Udat.01
Udat.02
Udat.03
Udat.04
Udat.05
Udat.06
Udat.07
Udat.08
Udat.09
Udat.10
Udat.11
Udat.12
Udat.13
Udat.14
Udat.15
UdatParity
g10g
g10f
g10d
g10e
g11g
g11f
g11d
g11e
g10i
g10h
g10b
g10c
g11i
g11h
g11b
g11c
f10g
f10f
f10d
f10e
f11g
f11f
f11d
f11e
f10i
f10h
f10b
f10c
f11i
f11h
f11b
f11c
e10g
e10f
e10d
e10e
e11g
e11f
e11d
e11e
e10i
e10h
e10b
e10c
e11i
e11h
e11b
e11c
d10g
d10f
d10d
d10e
d11g
d11f
d11d
d11e
d10i
d10h
d10b
d10c
d11i
d11h
d11b
d11c
h14g
h14f
h14d
h14e
S374
TP005
TP006
TP007
TP008
TP009
TP010
TP011
TP012
TP013
TP014
TP015
TP016
TP017
TP018
TP019
TP020
TP021
TP022
TP023
TP024
TP025
TP026
TP027
TP028
TP029
TP030
TP031
TP032
TP033
TP034
TP035
TP036
TP037
TP038
Flip.00'
Flip.01'
Flip.02'
Flip.03'
Flip.04'
Flip.05'
Flip.06'
Flip.07'
Flip.08'
Flip.09'
Flip.10'
Flip.11'
Flip.12'
Flip.13'
Flip.14'
Flip.15'
PUa
Cdat.00
Cdat.01
Cdat.02
Cdat.03
Cdat.04
Cdat.05
Cdat.06
Cdat.07
Cdat.08
Cdat.09
Cdat.10
Cdat.11
Cdat.12
Cdat.13
Cdat.14
Cdat.15
CdatParity
h14j
CK OC'
EdgeClock'c
GND
TP039
8 D->O
16.5 S ->O
h13
D0
S151
CrctSyn4
CrctSyn5
CrctSyn6
CorrectThisWord'
TP040
EdgeClock'e
d10j
e10j
f10j
g10j
d11j
e11j
f11j
g11j
LoadSyndrome
h14h
h14i
h14b
h14c
XEROX
EOD
Project
D0
Memory Control
Error Correction
File
D0mem03.sil
Designer
Rosen/Thacker
Rev
Gb
Date
2/19/79
Page
03

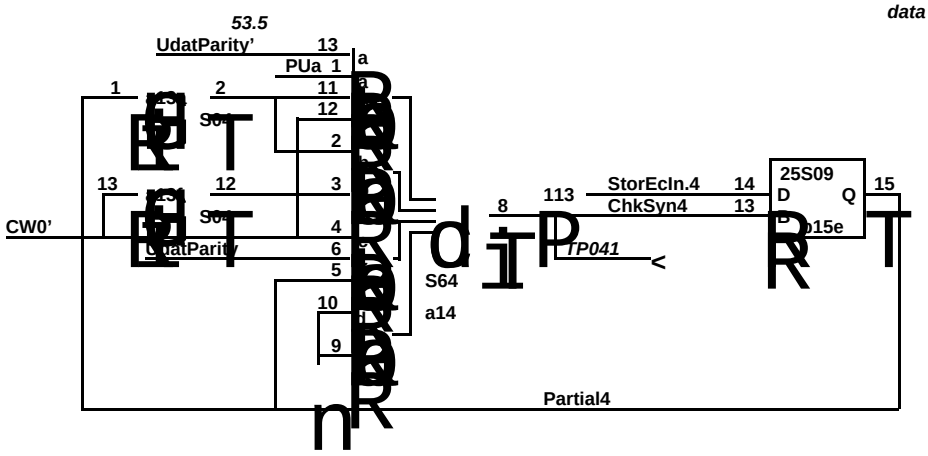


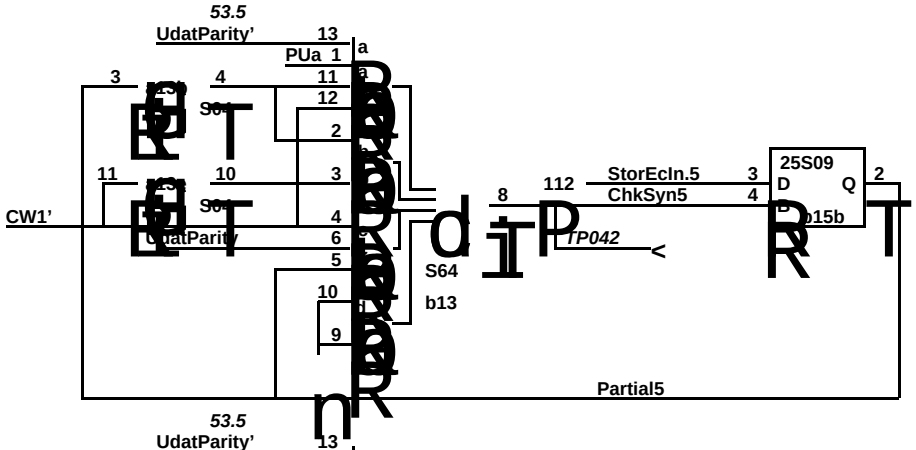
XEROX EOD	Project D0	Memory Control Data Paths	File D0mem04.sil	Designer Rosen	Rev Gb	Date 9/19/77	Page 04

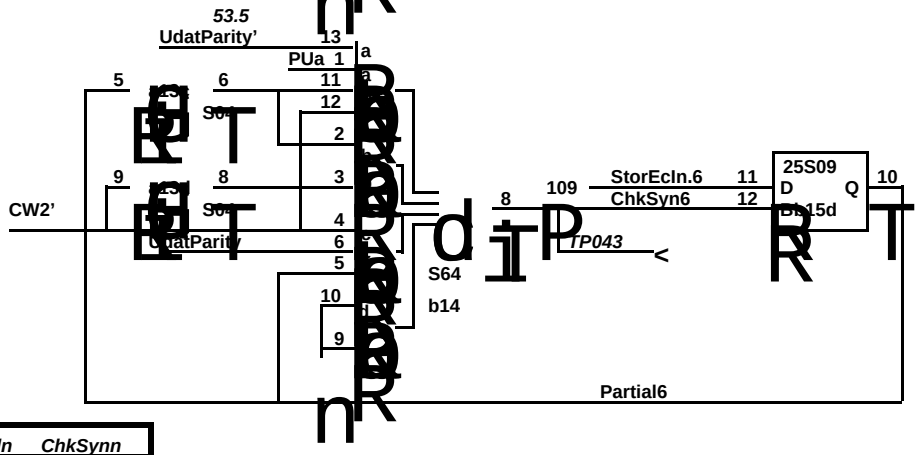


XEROX EOD	Project D0	Memory Control Data Paths Bits 08:15	File D0mem05.sil	Designer Rosen	Rev Gb	Date 11/20/77	Page 05

Note: Storage card inverts data and check bits





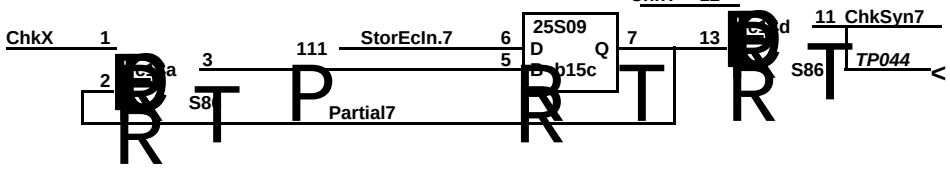


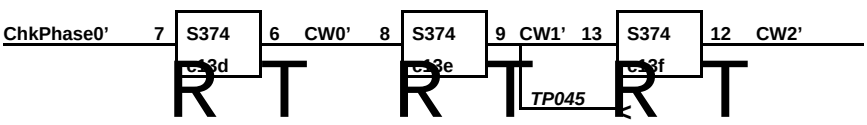
CW'=1:

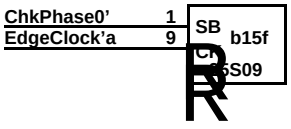
UdatParity	*PartialN*	*ChkSynn*
0	*0*	*0*
0	*1*	*1*
1	*0*	*1*
1	*1*	*0*

CW' = 0

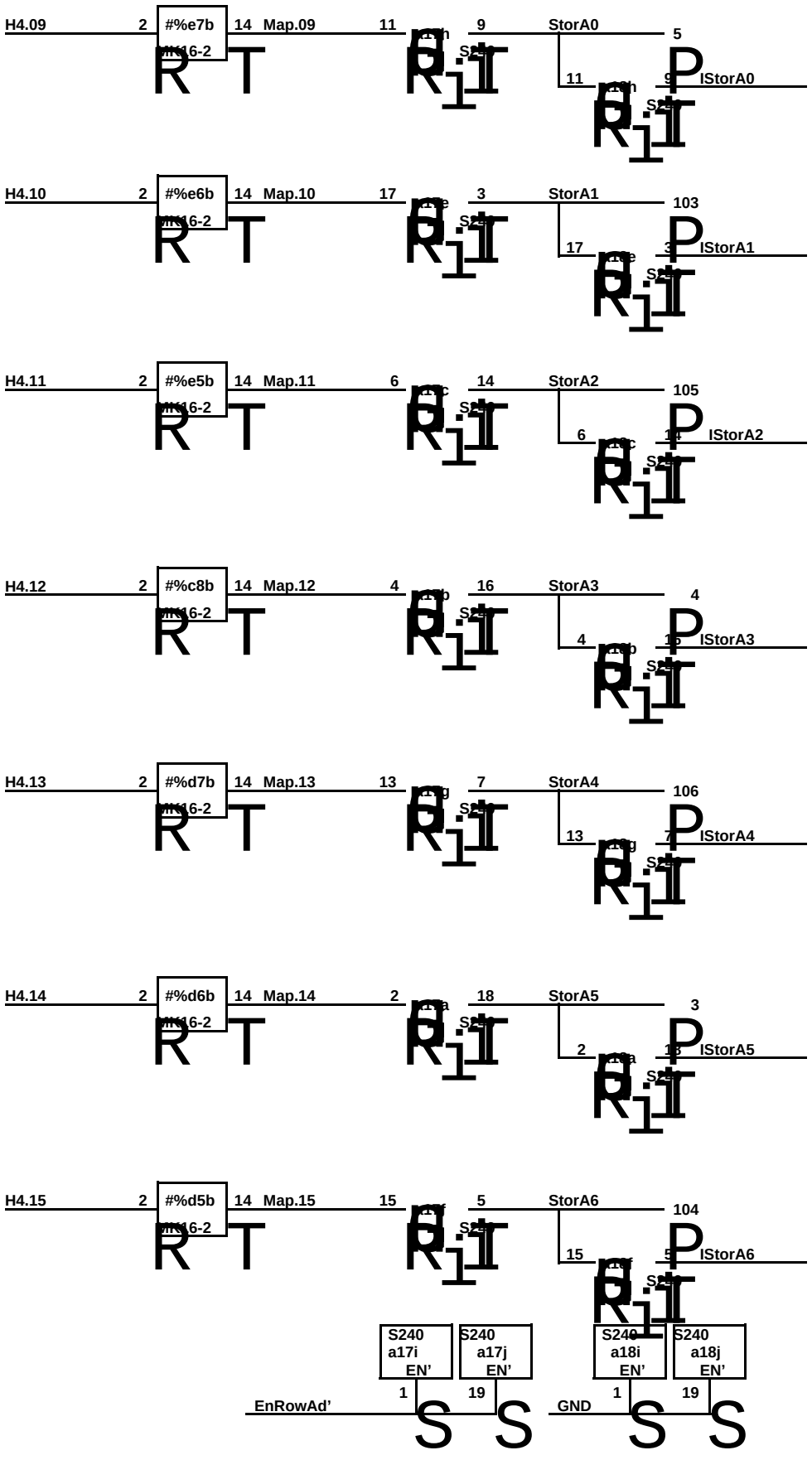
PartialN	*ChkSynn*
0	*0*
1	*1*



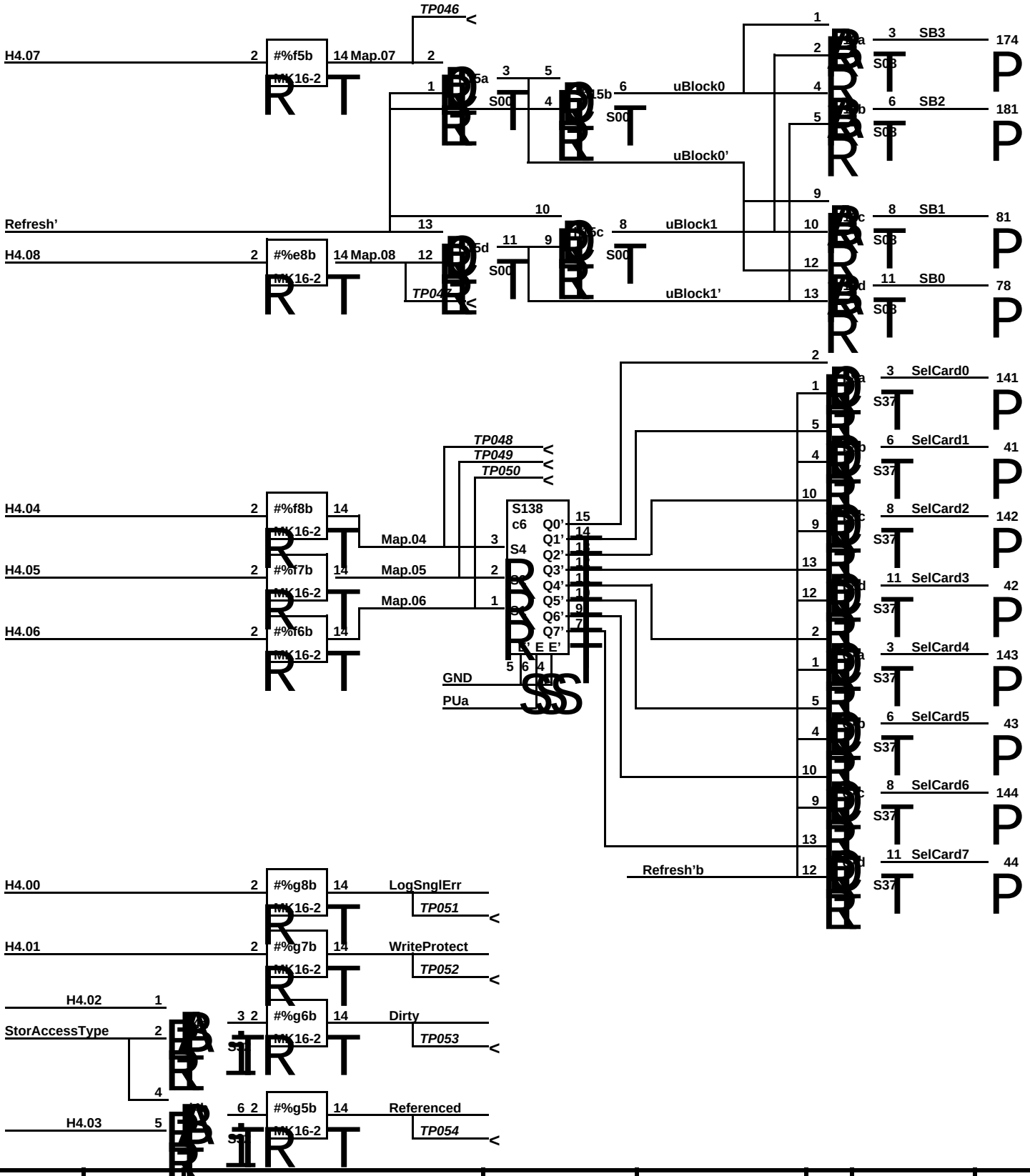




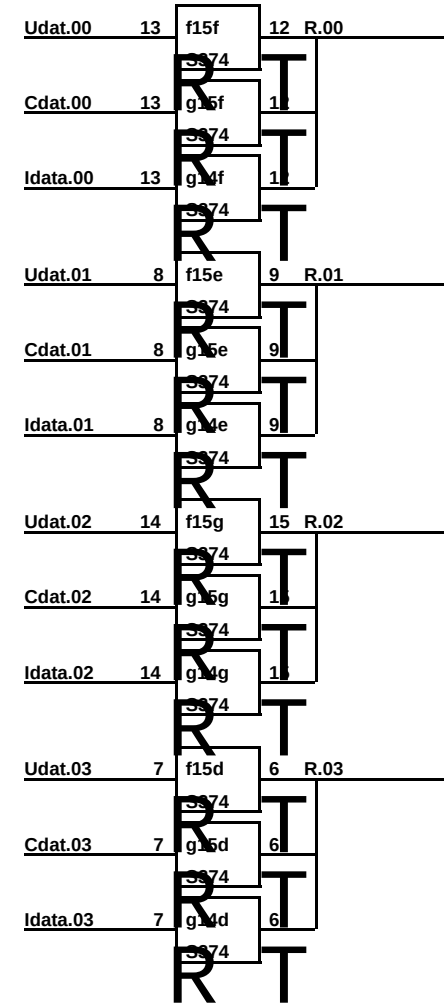
XEROX EOD	Project D0	Memory Control Error Correction Checker	File D0mem06.sil	Designer Thacker	Rev Gb	Date 5/9/78	Page 06

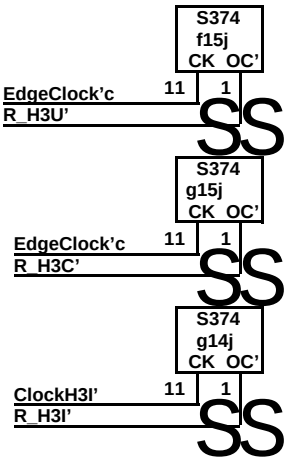


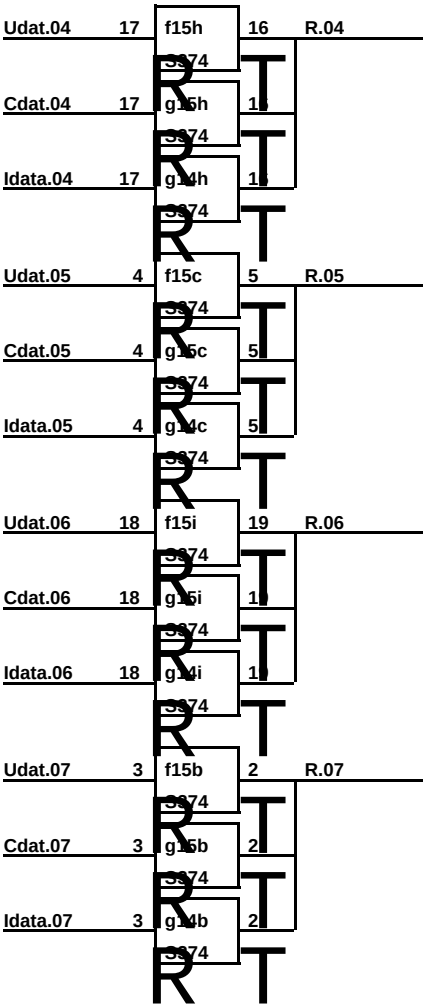
XEROX EOD	Project D0	Memory Control Map & Mem Address	File D0mem07.sil	Designer Rosen	Rev Gb	Date 2/19/79	Page 07



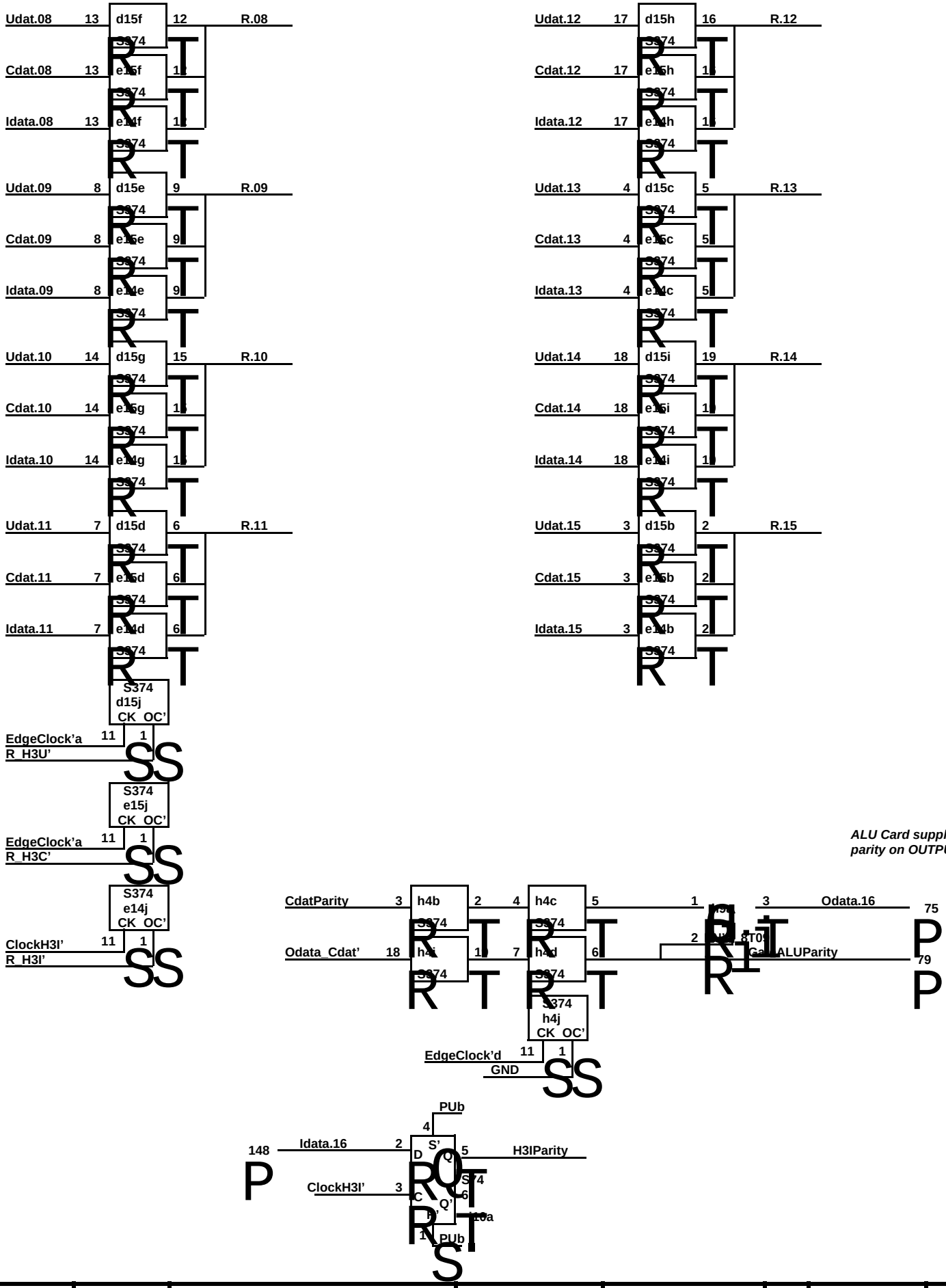
XEROX EOD	Project D0	Memory Control Map A0, Bank, Card, Flags	File D0mem08.sil	Designer Rosen	Rev Gb	Date 2/19/79	Page 08



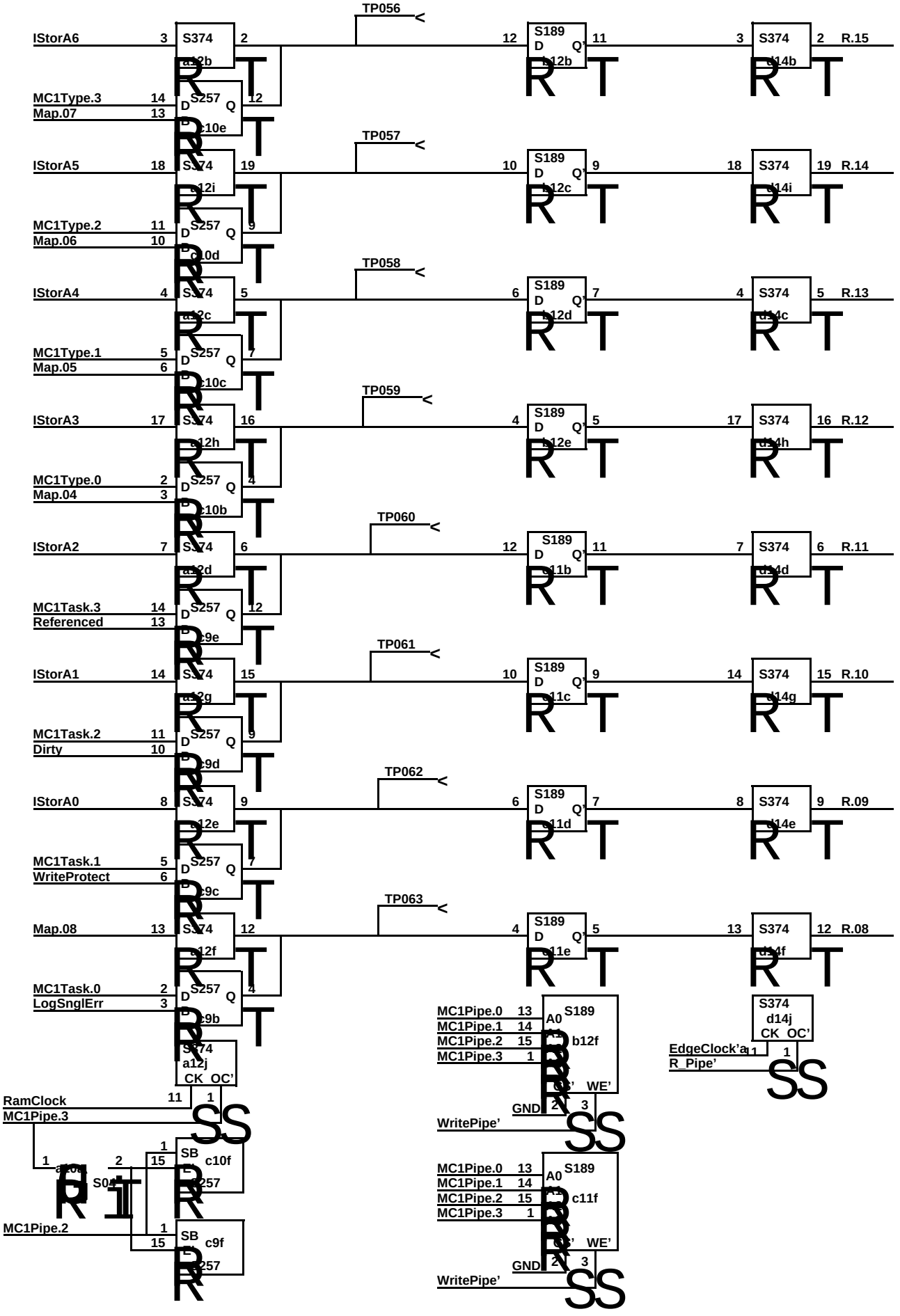




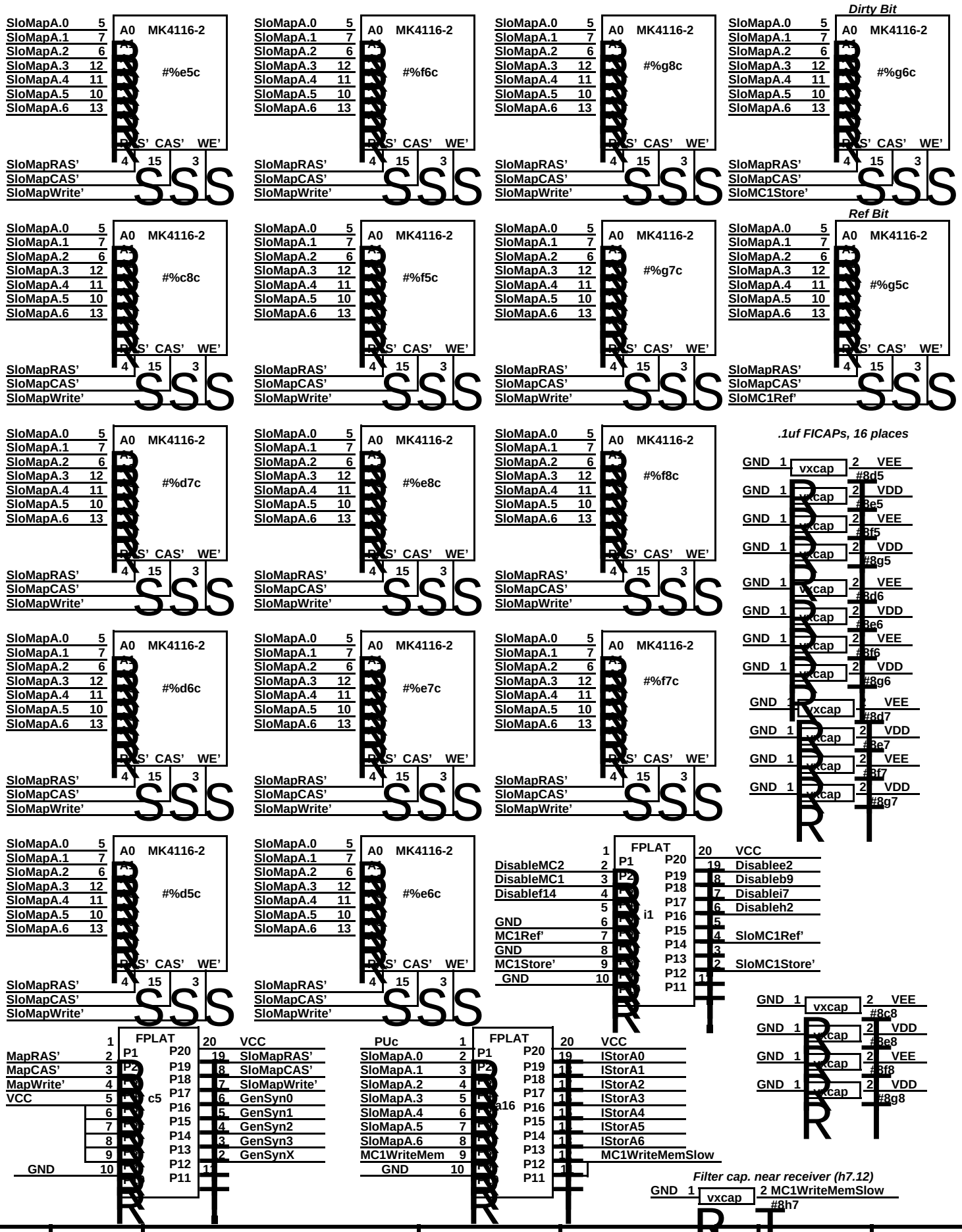
XEROX EOD	Project D0	Memory Control R Sources Hi	File D0mem09.sil	Designer Rosen	Rev Gb	Date 9/19/77	Page 09



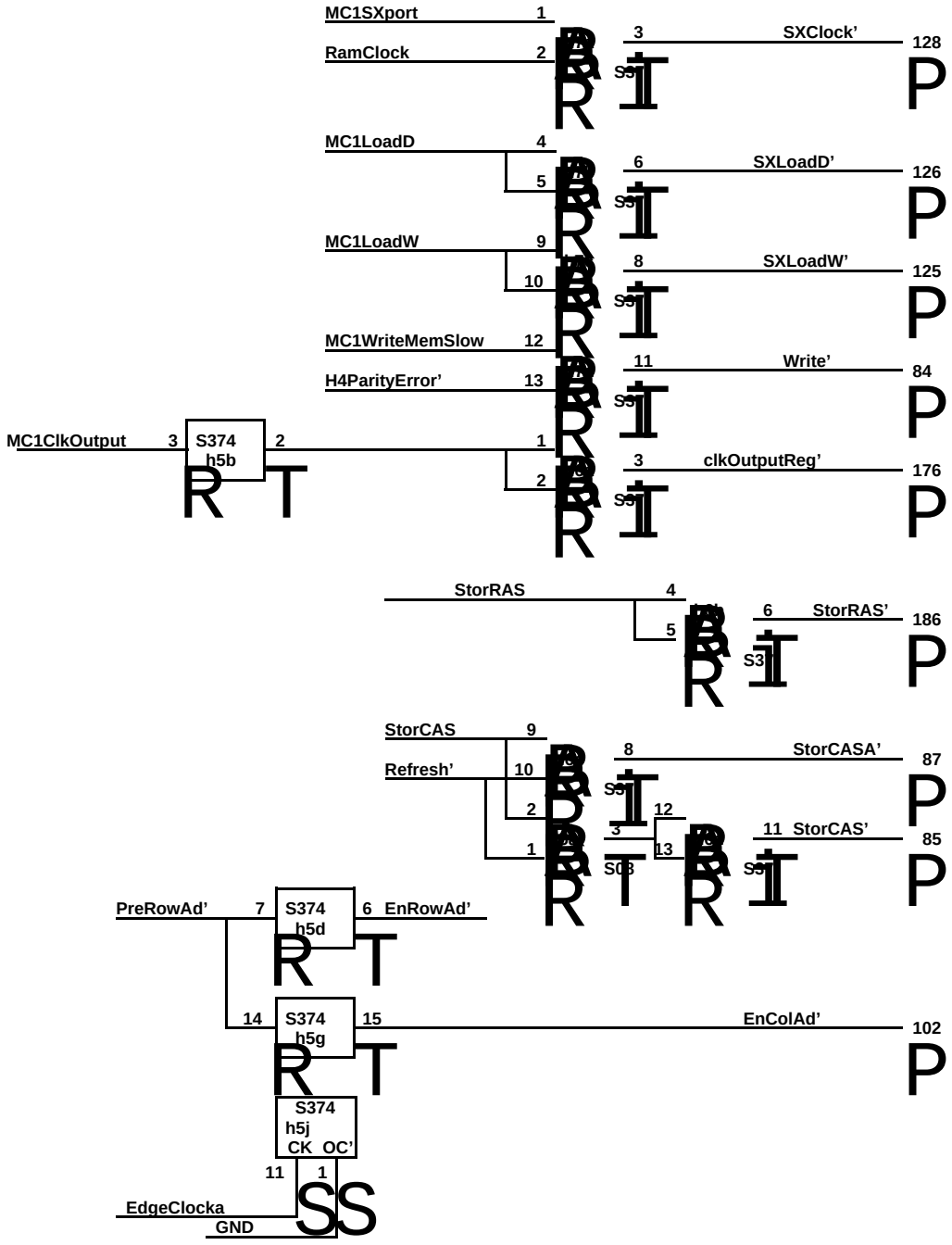
XEROX EOD	Project D0	Memory Control R Sources Lo, Parity	File D0mem10.sil	Designer Thacker	Rev Gb	Date 8/12/78	Page 10



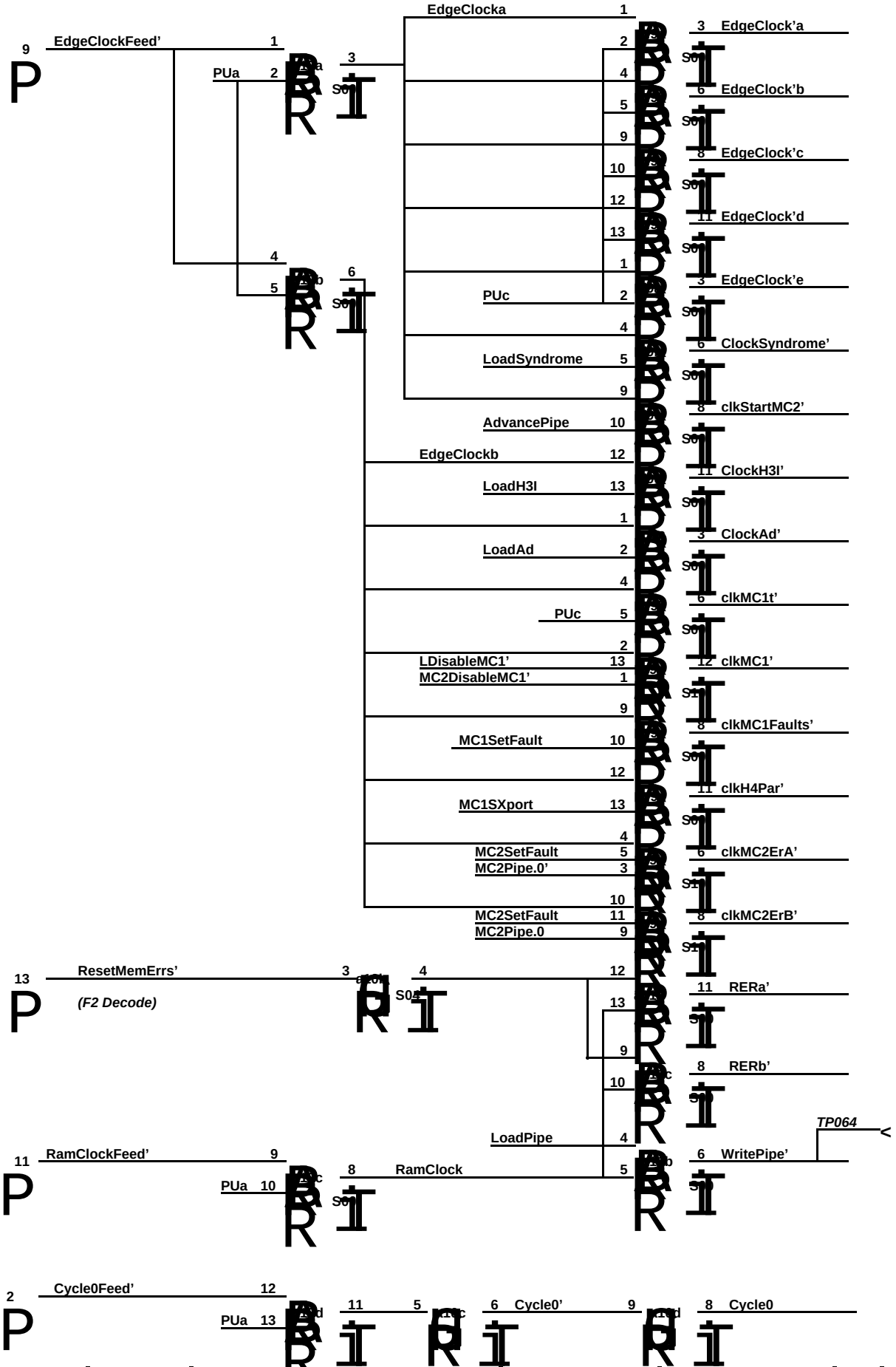
XEROX EOD	Project D0	Memory Control Pipe Data	File D0mem11.sil	Designer Thacker	Rev Gb	Date 5/9/78	Page 11



XEROX EOD	Project D0	Memory Control Map Chip Address Sections	File D0mem12.sil	Designer Thacker	Rev Gb	Date 7/18/80	Page 12



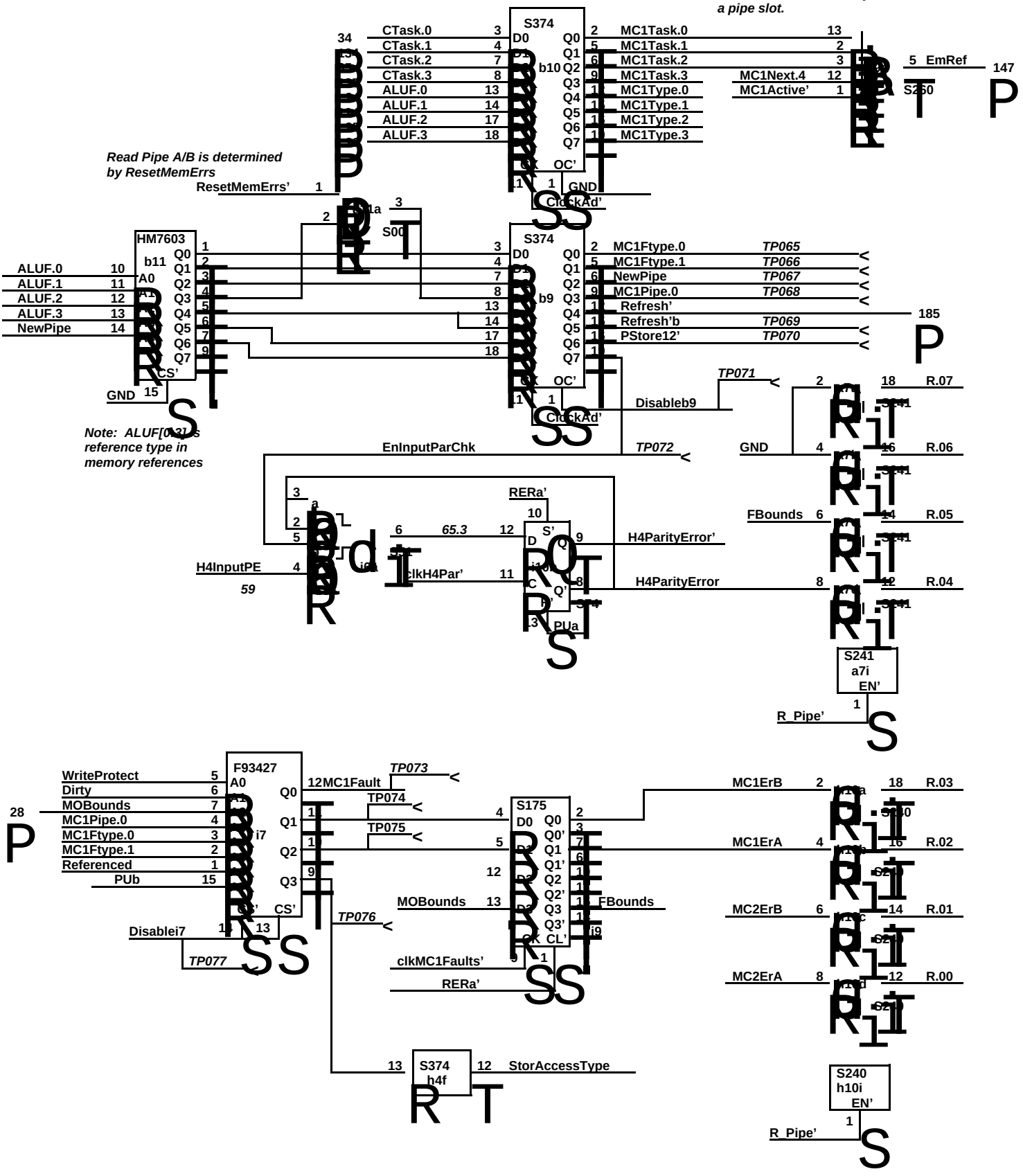
XEROX EOD	Project D0	Memory Control Storage Card Controls	File D0Mem13.sil	Designer Thacker	Rev Gb	Date 12/9/78	Page 13



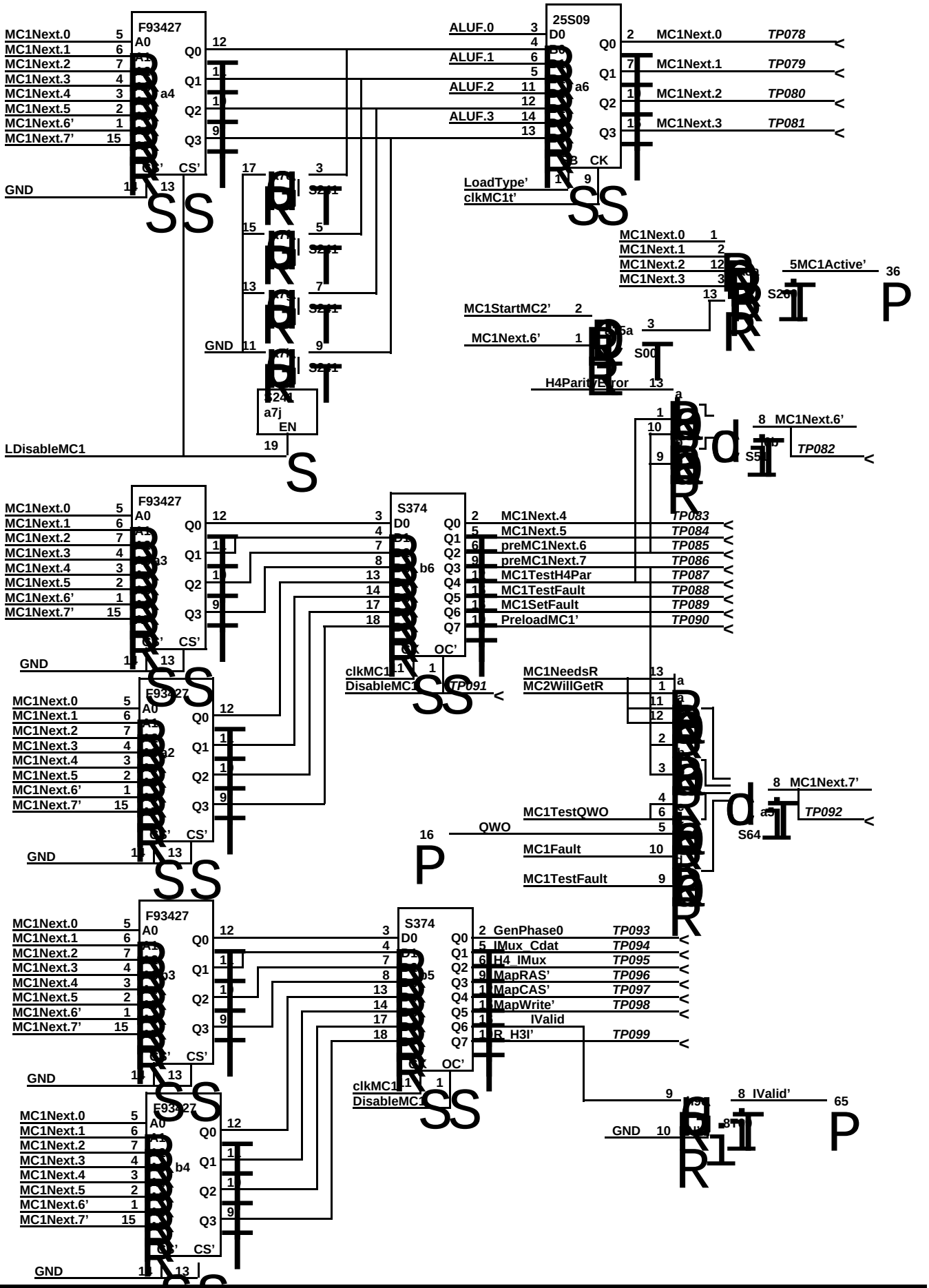
XEROX EOD	Project D0	Memory Control Clocks & Read Mem	File D0mem14.sil	Designer Thacker	Rev Gb	Date 7/18/80	Page 14

Ftype classifies references according to the types of faults they can cause: Non-memory/Fetch/Store

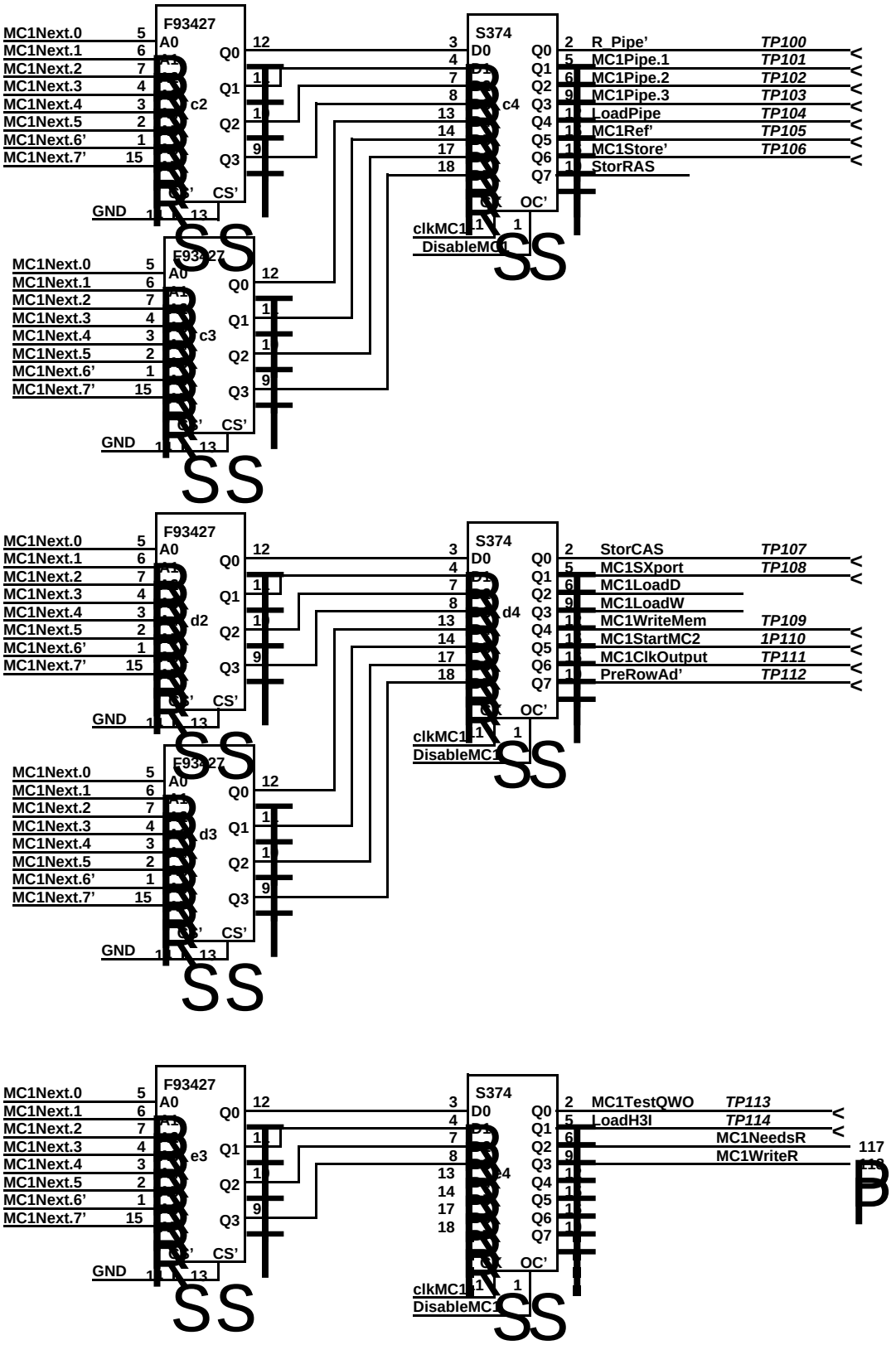
Referecnes are also classified as to whether or not they use a pipe slot.



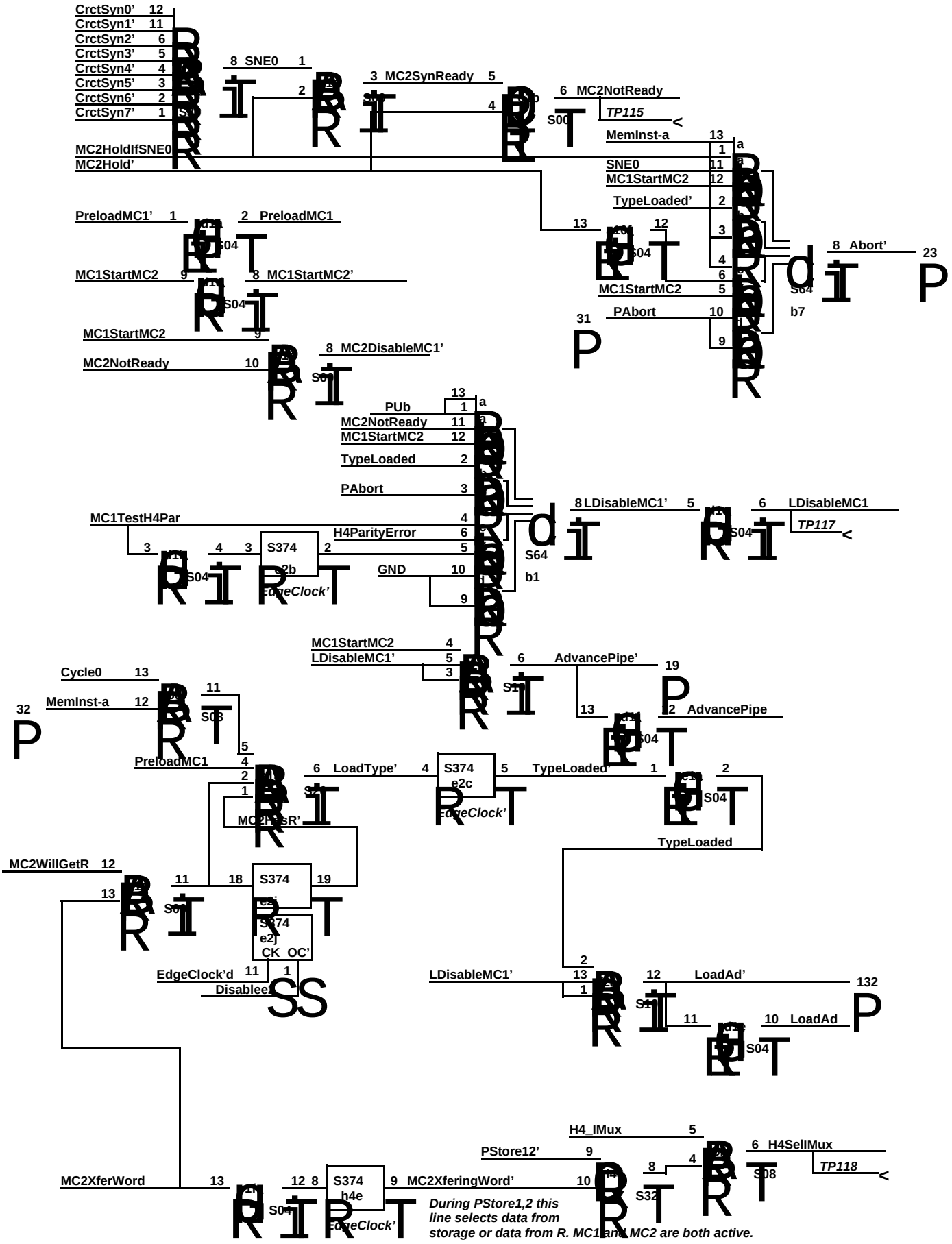
XEROX EOD	Project D0	MC1 Input Register, MC1 Faults	File d0mem15.sil	Designer Thacker	Rev Gb	Date 11/1/78	Page 15



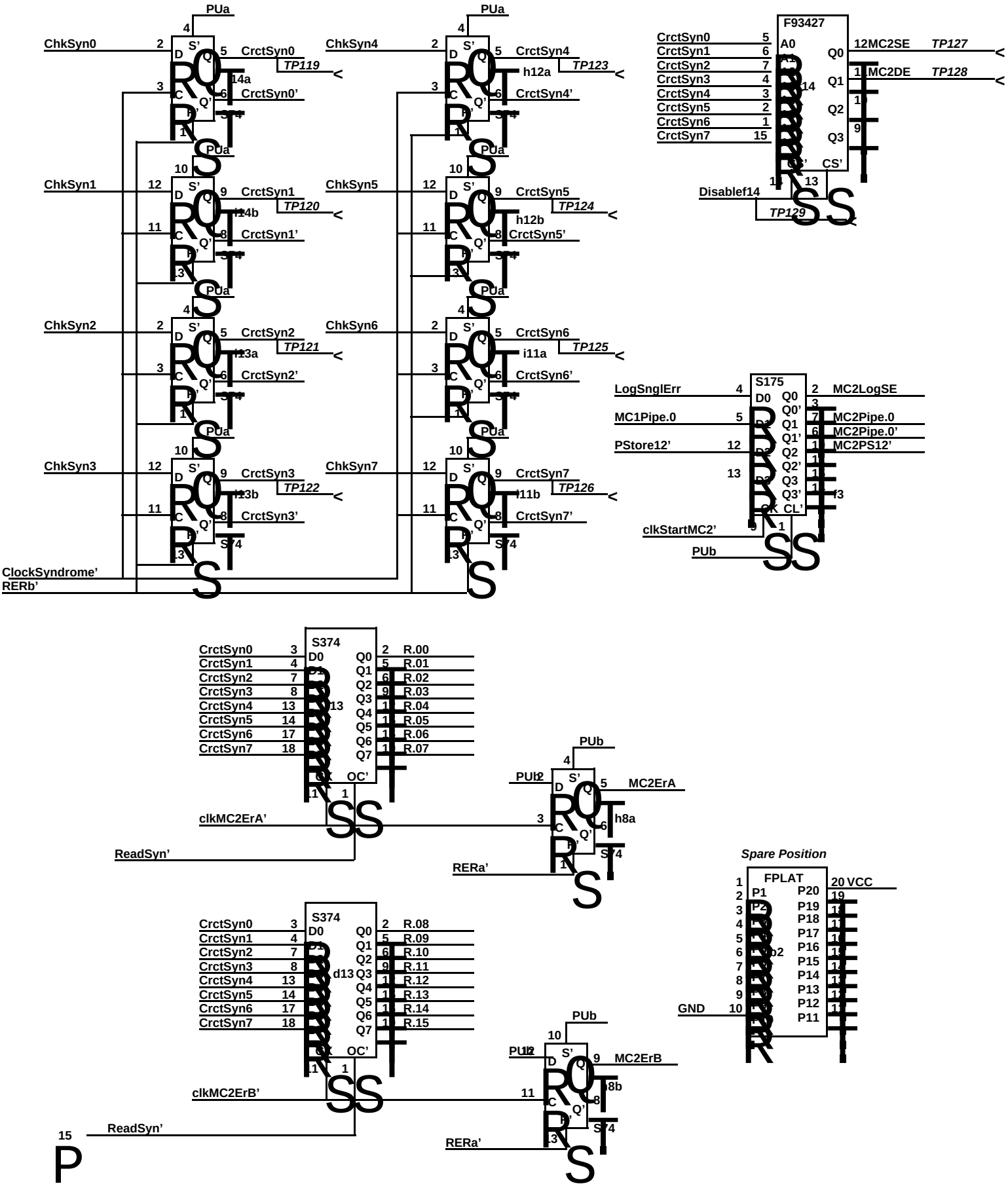
XEROX EOD	Project D0	MC1	File d0mem16.sil	Designer Thacker	Rev Gb	Date 8/12/78	Page 16



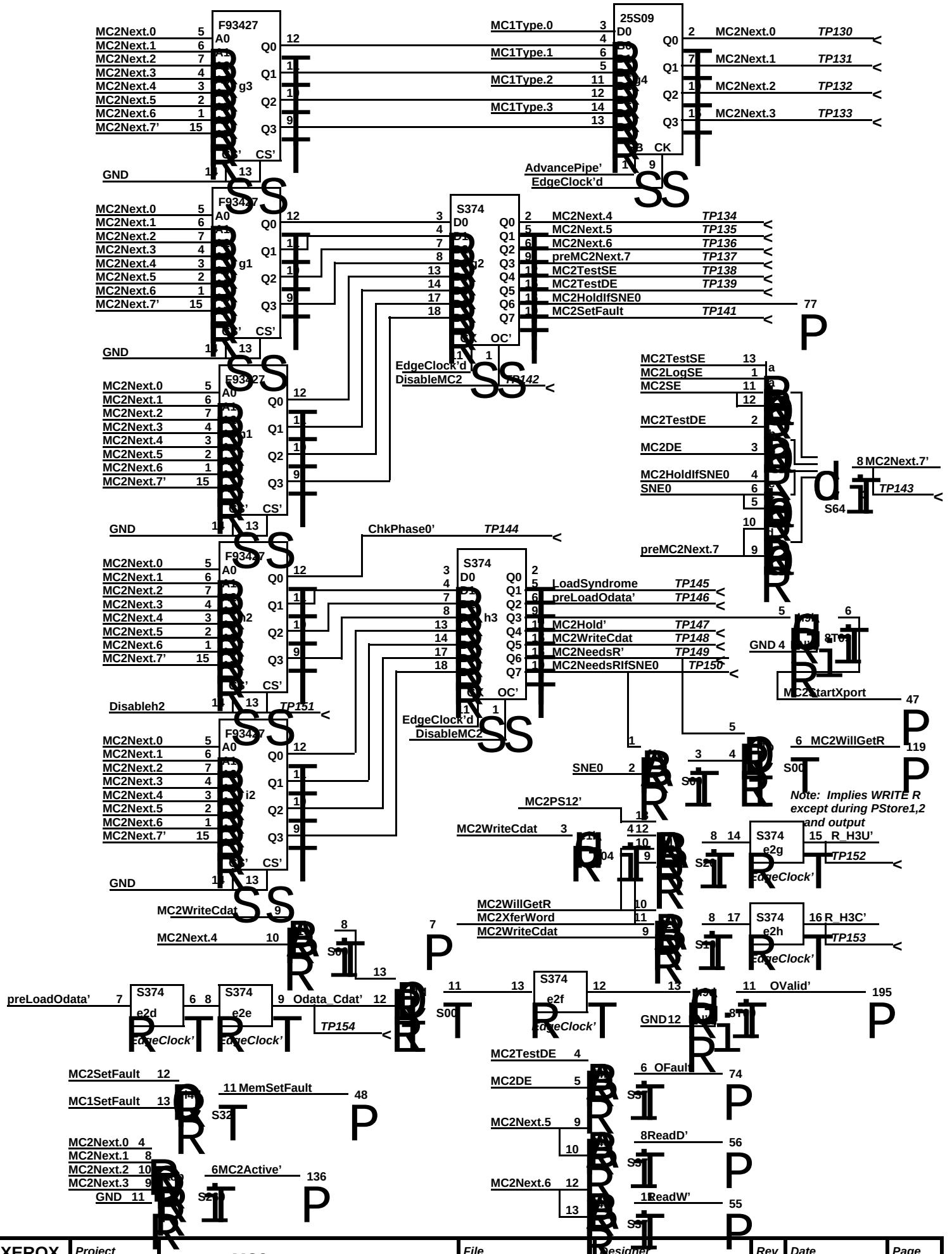
XEROX EOD	Project D0	More MC1	File d0mem17.sil	Designer Thacker	Rev Gb	Date 5/9/78	Page 17



XEROX EOD	Project D0	MC1/MC2 Logic	File d0mem18.sil	Designer Thacker	Rev Gb	Date 7/18/80	Page 18



XEROX EOD	Project D0	MC2 Input Register/Errors	File d0mem19.sil	Designer Thacker	Rev Gb	Date 7/18/80	Page 19



XEROX EOD	Project D0	MC2	File d0mem20.sil	Designer Thacker	Rev Gb	Date 5/9/78	Page 20

Changes from Rev E to Rev F:

1) Added the signal Disableh2 (pg 20,12) for test

2) Removed H4ParityError' from the term that forms Abort' (gate at a15 now free, inverter at e1a moved).

Note: This change deletes IC a15.

Changes from RevF to RevG:

1) b11.15 (pg 1) _ GenX, not GenX' (this was wrong in .nl file, ok on dwg.)

2) h13.9 _ CrctSyn4, h13.11 _ CrctSyn6 (pg. 3)

Changes from RevG to RevH:

1) (pg13) Change c1.13 from RamClock to EdgeClocka

2) (pg 13,15) Changed i9 from S74 to S175. Relocated i9's functions to i10. Added MOBounds as R.05 during R_Pipe operation.

3) (pg 16) Deleted S04 at a10e. Replaced with S00 a15a, and added MC1StartMC2' as input to MC1Active.

4) Added MC2PS12' by replacing f3 (S74) with S175 (pg 19). MC1PS12' is used instead of PStore12' at a1.13 (pg 20).

Changes from RevH to RevI (5/9/78)

1) (pg 20) h3.9 was MC2HoldIfSNE0, is now MC2StartXport' after passing through the 8T09 at h9b (used as a driver).

2) Renamed signal MC2TestSNE0 to MC2HoldIfSNE0 (essentially, these two signals have been coalesced into one).

3) Added test points.

4) Added comments on Vee bypass and -10V supply changes to D0memplatforms.sil

Changes from Rev I to Rev J (8/12/78 - C. Thacker)

1) Renamed signal TP055 GateALUParity, and connected it to E079 (pg 10)

2) Latched signal StorAccessType in S374 at h4f (pg 15)

3) Removed MC2XferWord and MC1XferWord from a5.11 and a5.12. Connected a5.11 and a5.12 to a5.13 (pg 16). Note thac signal MC1XferWord is no longer used on this card, so E006 is free.

4) Removed -10V supply components on D0memplatforms.sil

Changes from Rev J to rev K (10/8/78 - C. Thacker)

1) Changed h7.12 from MC1WriteMem to MC1WriteMemSlow (pg13). This signal is generated at platform a16 (pg12).

2) Changed platform a16 to 20pins to make room for MC1WriteMemSlow (pg12).

3) Added capacitors on SloMapRAS' and SloMapWrite' (platform c5, page 12).

4) Changed a9.12 from MC1Task.3 to MC1Next.4 (pg15).

5) Changed i7.1 from PUb to Referenced (pg15). This requires changing PROM i7 to revision E.

Changes from Rev K to rev L (11/1/78 - C. Thacker)

1) Signal clkOutputReg is now clkOutputReg' by removing S37 at h6a (now free) page 13.

2) b10.1 (pg15) was Disableb10, is now GND. Also removed Disableb10 from SPLAT i1 (pg 12).

There are no prom changes in this revision.

Changes from Rev L to rev M (12/9/78 - C. Thacker)

1) Changed platforms c5 and i1 - removed capacitors and changed values.

2) Changed the generation of clkOutputReg' (pg 13). This signal is now one cycle wide, rather than being a qualified EdgeClock.

3) The input to h5g (pg 13) is PreRovAd', not EnRowAd'. This board requires an ALU board of rev M for proper operation.

There are no prom changes in this revision.

Note: Rev M = Rev Ga

Changes from rev Ga to rev Gb (7/18/80 - CPT).

1) Added 16 FICAPS for MK4116 chips (VDD and VEE)

2) Added glitch suppression capacitor adjacent to h7 (on MC1WriteMemSlow - 100pf).

3) Changed interlock logic on page 18.

Current PROM Revisions:

a4, a3, a2, b3, b4, c2, c3, d2, d3, e3 (MC1 Sequencer): E

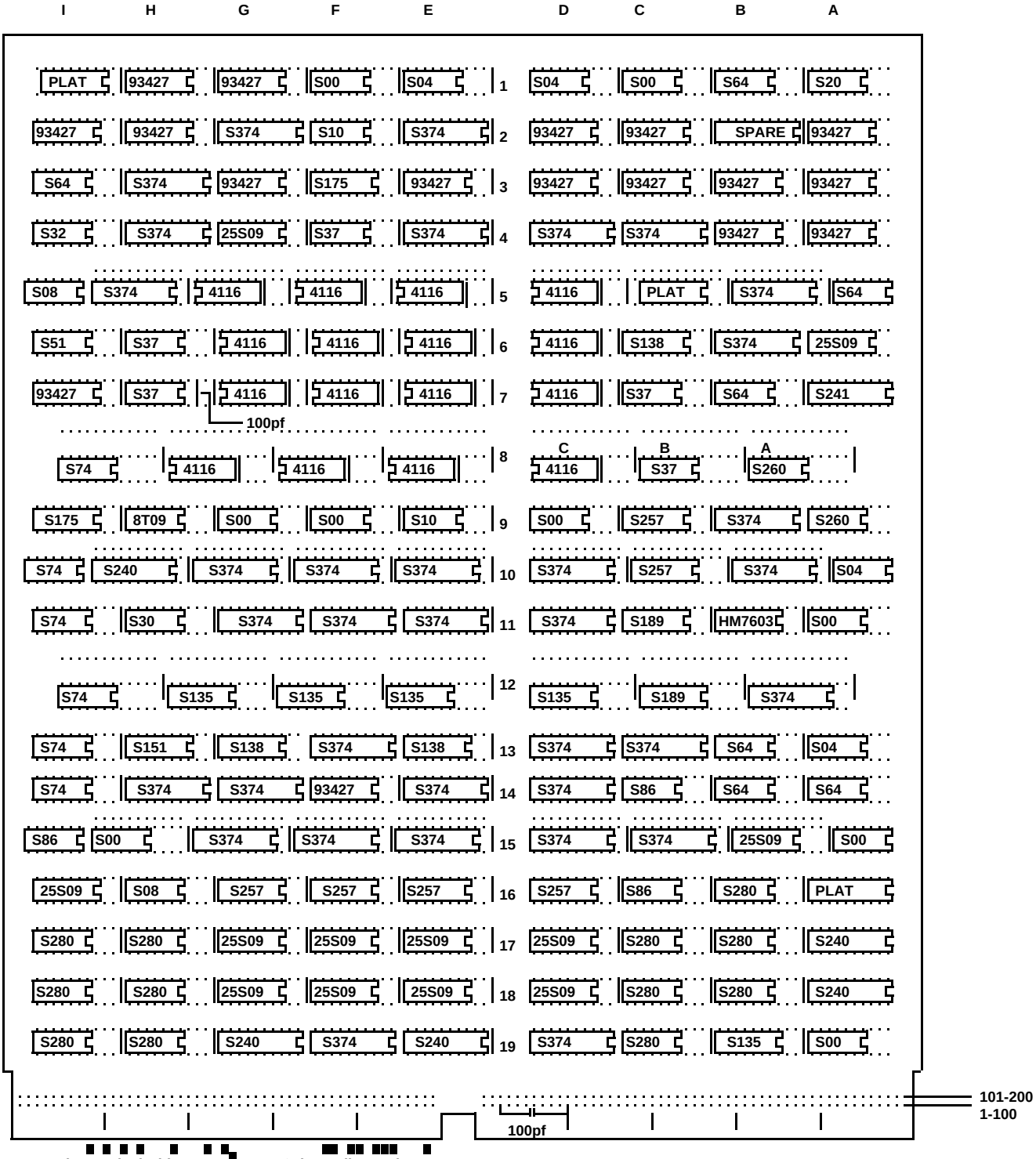
g3, g1, h1, h2, i2 (MC2 Sequencer): D

i7 (Fault): E

b11 (Ftype, Pipe): D

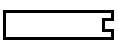
f14 (Single/Double errors): D

XEROX EOD	Project D0	Memory Control Changes	File d0memchanges.sil	Designer Thacker	Rev Gb	Date 7/18/80



Note: Pinx marked with ■ have 470ohm pullup resistors to +5v.

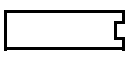
20pins: A



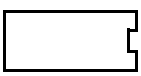
16pins: B

14pins: C

22pins: D



24 pins: E

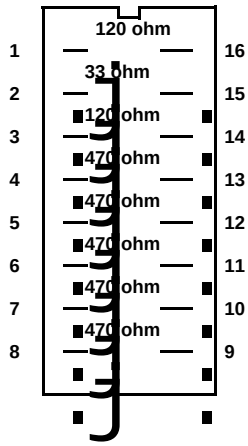


Note: The short vertical lines indicate filter capacitor locations.

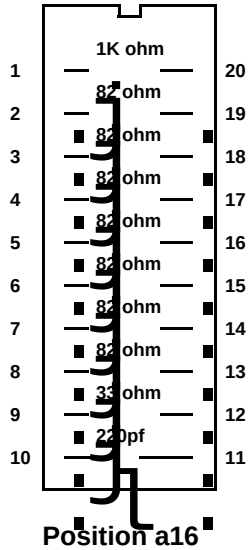
(143 Places)

16pins REVERSED!!!
typical of MK4116: F

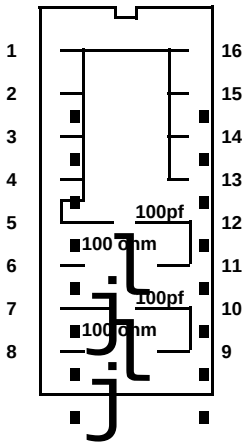
XEROX CSL	Project D0	Memory Control Board Layout	File d0memlayout.sil	Designer Thacker	Rev Gb	Date 7/18/80



Position c5



Position a16



Position i1

XEROX EOD	Project D0	Memory Control PLATFORMS	File D0MemPLATFORMS.sil	Designer Thacker	Rev Gb	Date 7/18/80