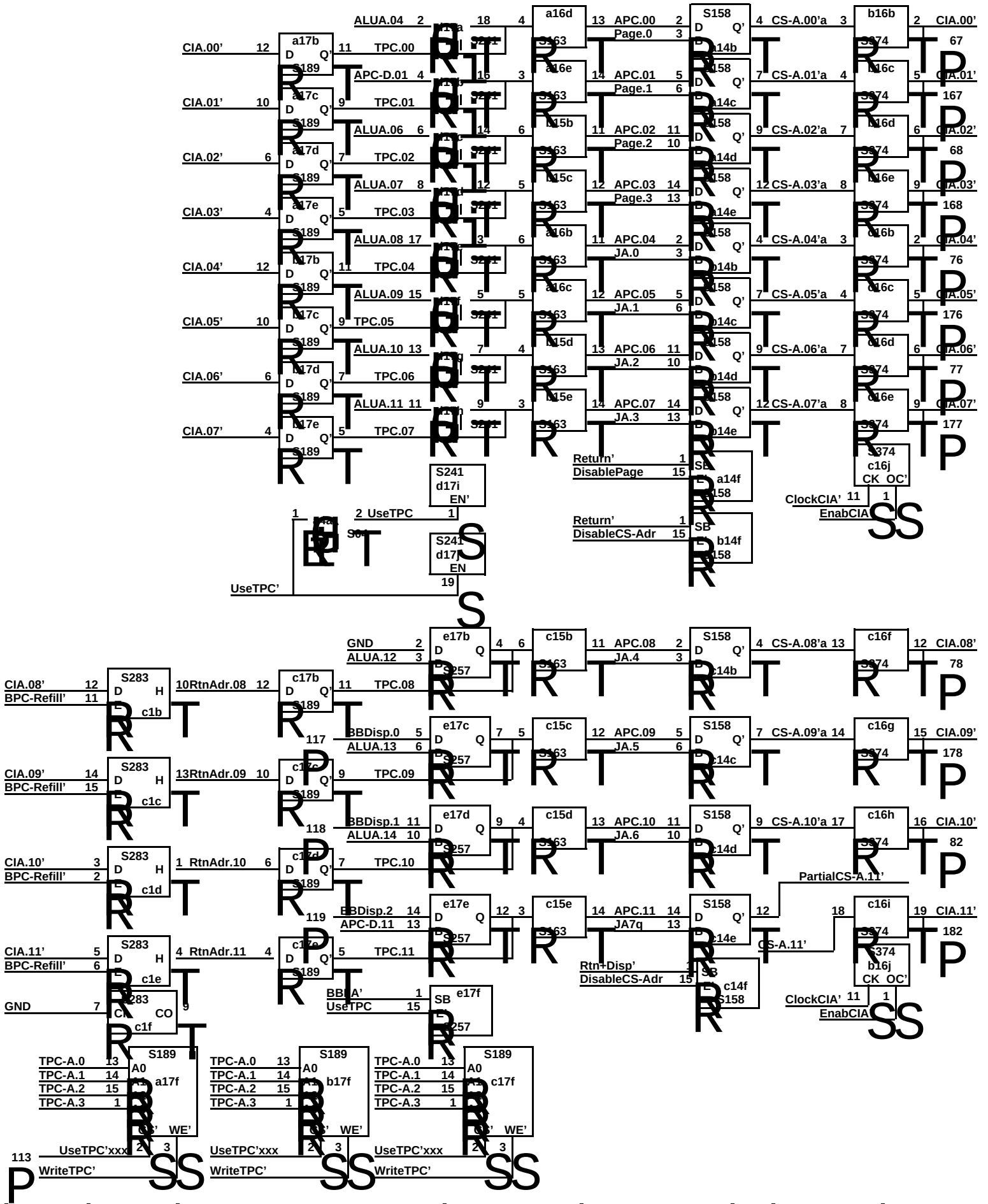
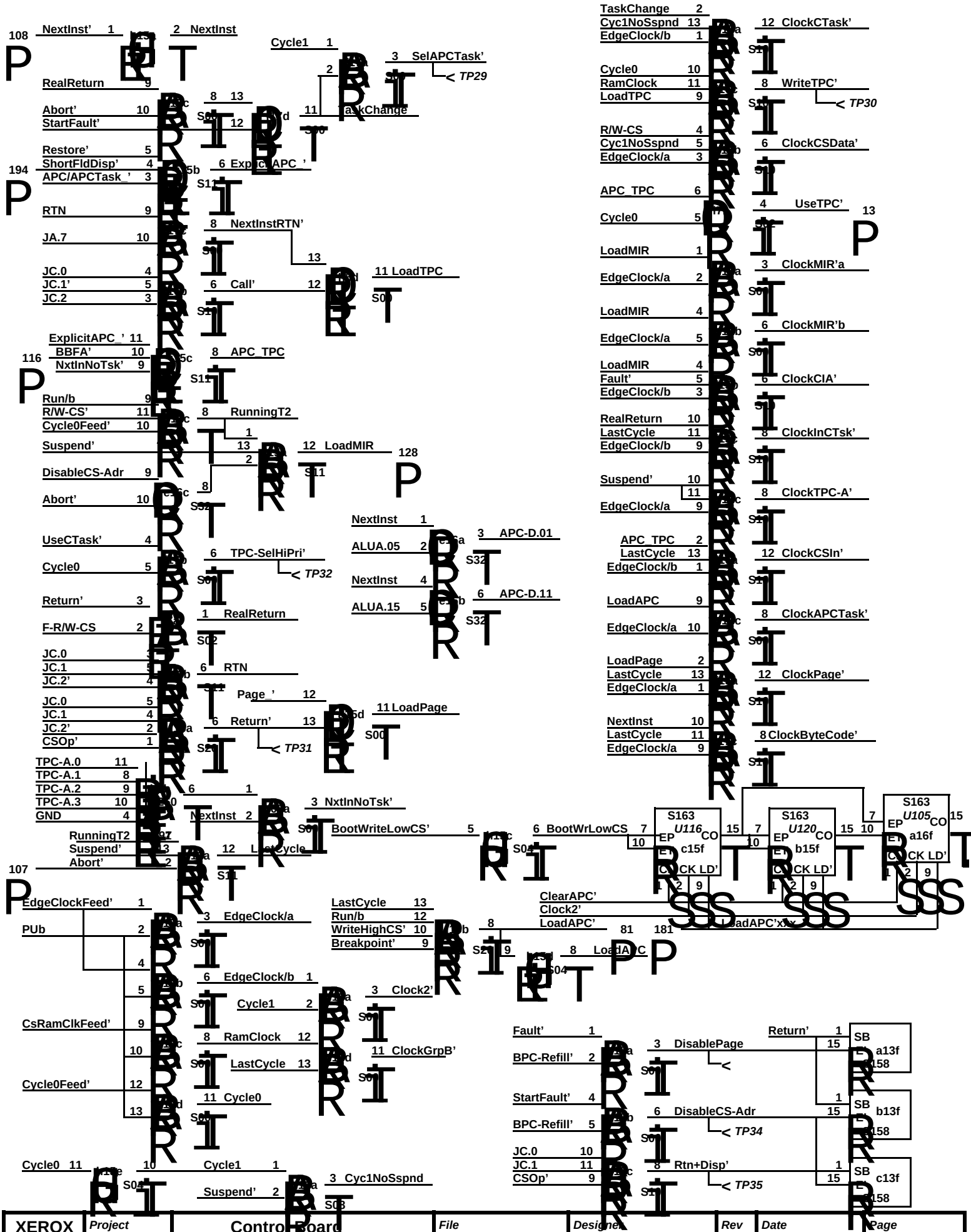
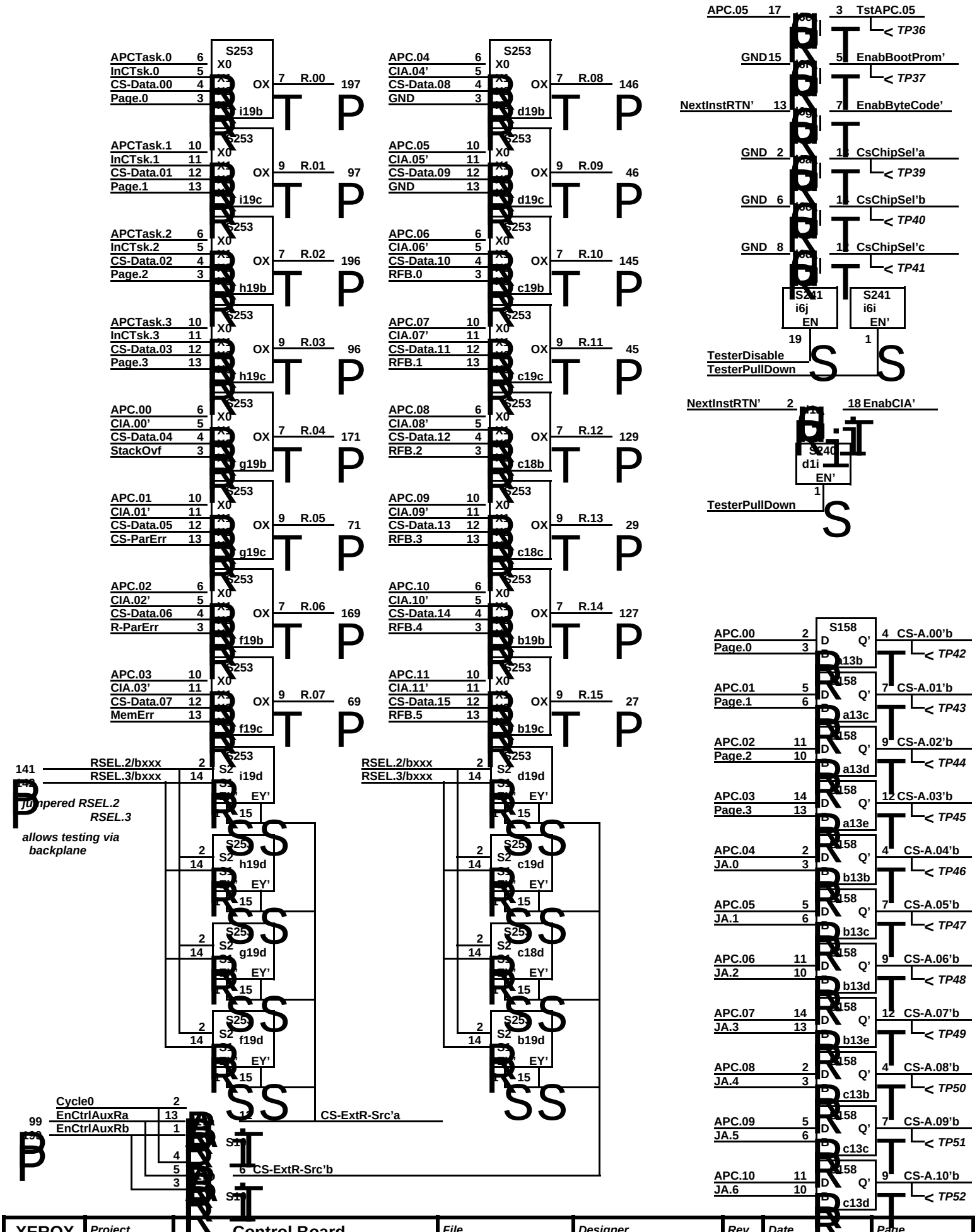
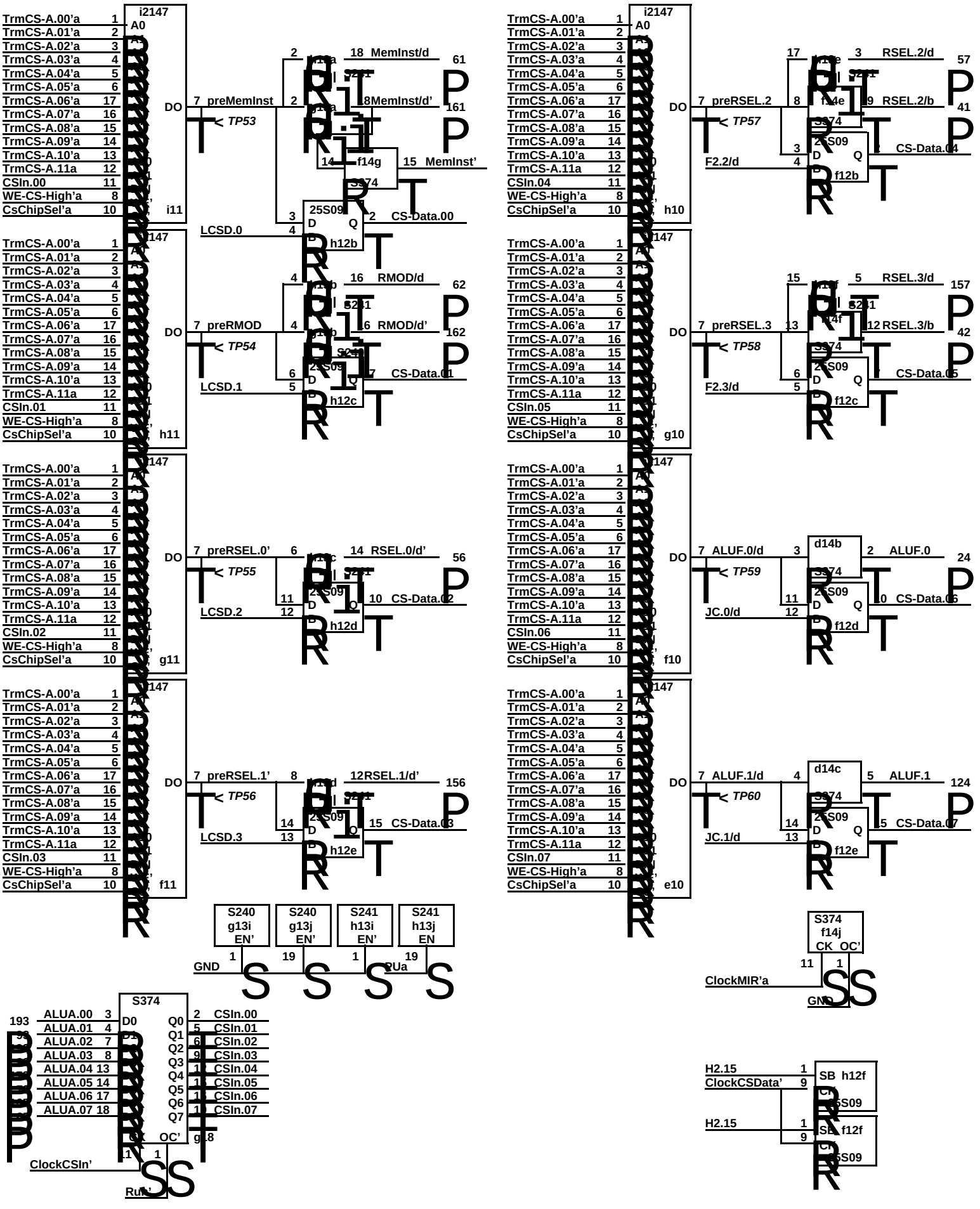


XEROX EOD	Project D0	Control Board Tasks/PCs/CS-Address	File D0cs01.sil	Designer Rosen	Rev Gc	Date 11/26/78	Page 01

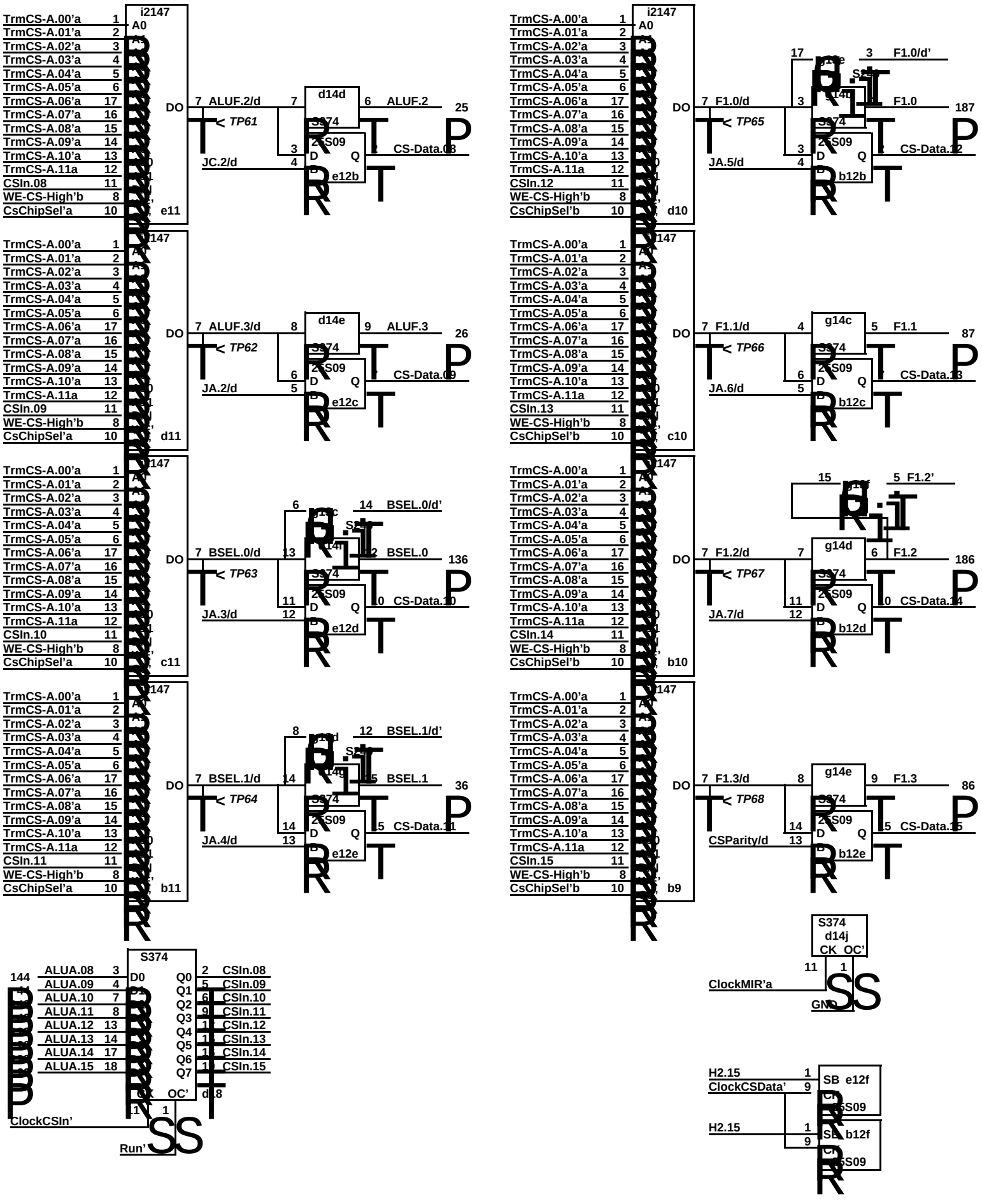

NextInst' 1
RealReturn 9
Abort' 10
StartFault' 8
Restore' 5
ShortFldDisp' 4
APC/APCTask_' 3
RTN 9
JA.7 10
JC.0 4
JC.1' 5
JC.2 3
ExplicitAPC_' 11
BBFA' 10
NxtInNoTsk' 9
Run/b 9
R/W-CS' 11
Cycle0Feed' 10
Suspend' 13
DisableCS-Adr 9
Abort' 10
UseCTask' 4
Cycle0 5
Return' 3
F-R/W-CS 2
JC.0 3
JC.1 5
JC.2' 4
JC.0 5
JC.1 4
JC.2' 2
CSOp' 1
TPC-A.0 11
TPC-A.1 8
TPC-A.2 9
TPC-A.3 10
GND 4
RunningT2 7
Suspend' 13
Abort' 2
EdgeClockFeed' 1
PUb 2
CsRamClkFeed' 9
Cycle0Feed' 12
Cycle0 11
Cycle1 10
Suspend' 2
Cycle1 1
SelAPCTask'
TP29
TaskChange
ExplicitAPC_'
NextInstRTN'
Call'
LoadTPC
APC_TPC
RunningT2
LoadMIR
TPC-SelHiPri'
TP32
RealReturn
RTN
Page_' 12
Return' 13
TP31
LoadPage
NextInst 1
ALUA.05 2
NextInst 4
ALUA.15 5
APC-D.01
APC-D.11
NxtInNoTsk'
NextInst 2
BootWriteLowCS'
LastCycle
EdgeClock/a
EdgeClock/b
Cycle1
RamClock
LastCycle
Cycle0
Clock2'
ClockGrpB'
Cyc1NoSspnd
LastCycle 13
Run/b 12
WriteHighCS' 10
Breakpoint' 9
LoadAPC'
LoadAPC
BootWrLowCS
TaskChange 2
Cyc1NoSspnd 13
EdgeClock/b 1
Cycle0 10
RamClock 11
LoadTPC 9
R/W-CS 4
Cyc1NoSspnd 5
EdgeClock/a 3
APC_TPC 6
Cycle0 5
LoadMIR 1
EdgeClock/a 2
LoadMIR 4
EdgeClock/a 5
LoadMIR 4
Fault' 5
EdgeClock/b 3
RealReturn 10
LastCycle 11
EdgeClock/b 9
Suspend' 10
EdgeClock/a 9
APC_TPC 2
LastCycle 13
EdgeClock/b 1
LoadAPC 9
EdgeClock/a 10
LoadPage 2
LastCycle 13
EdgeClock/a 1
NextInst 10
LastCycle 11
EdgeClock/a 9
ClockCTask'
WriteTPC'
TP30
ClockCSData'
UseTPC'
ClockMIR'a
ClockMIR'b
ClockCIA'
ClockInCTsk'
ClockTPC-A'
ClockCSIn'
ClockAPCTask'
ClockPage'
ClockByteCode'
S163 U116 CO EP c15f CK LD'
S163 U120 CO EP b15f CK LD'
S163 U105 CO EP a16f CK LD'
ClearAPC'
Clock2'
LoadAPC'xfr
Fault' 1
BPC-Refill' 2
StartFault' 4
BPC-Refill' 5
JC.0 10
JC.1 11
CSOp' 9
DisablePage
DisableCS-Adr
TP34
Rtn+Disp'
TP35
Return' 1
SB a13f 158
SB b13f 158
SB c13f 158
XEROX EOD
Project D0
Control Board Data Path Control
File D0cs02.sil
Designer Rosen
Rev Gc
Date 2/19/79
Page 02



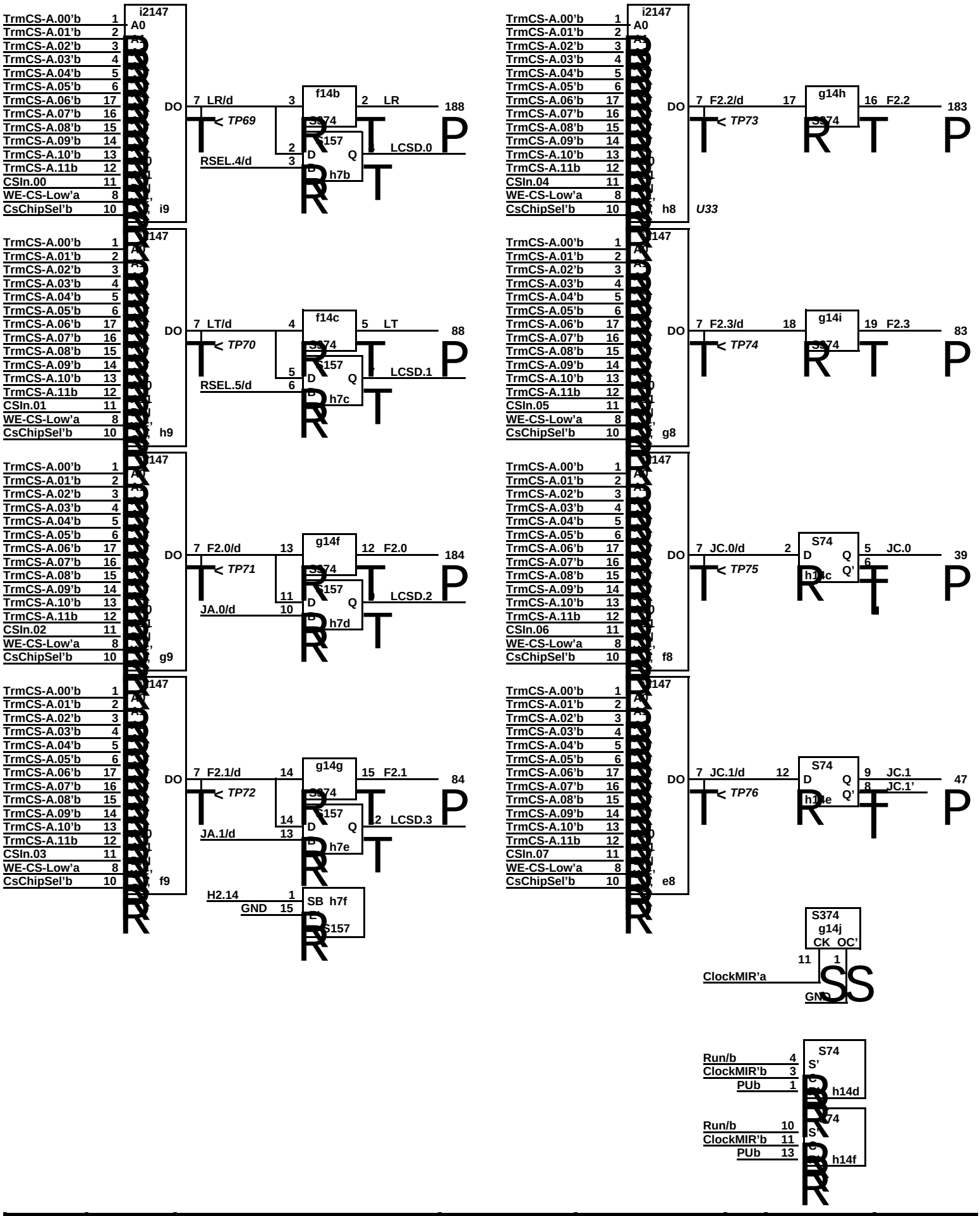
XEROX EOD	Project D0	Control Board R Sources/CS-Adr Extra Mux	File D0cs03.sil	Designer Rosen	Rev Gc	Date 2/19/79	Page 03



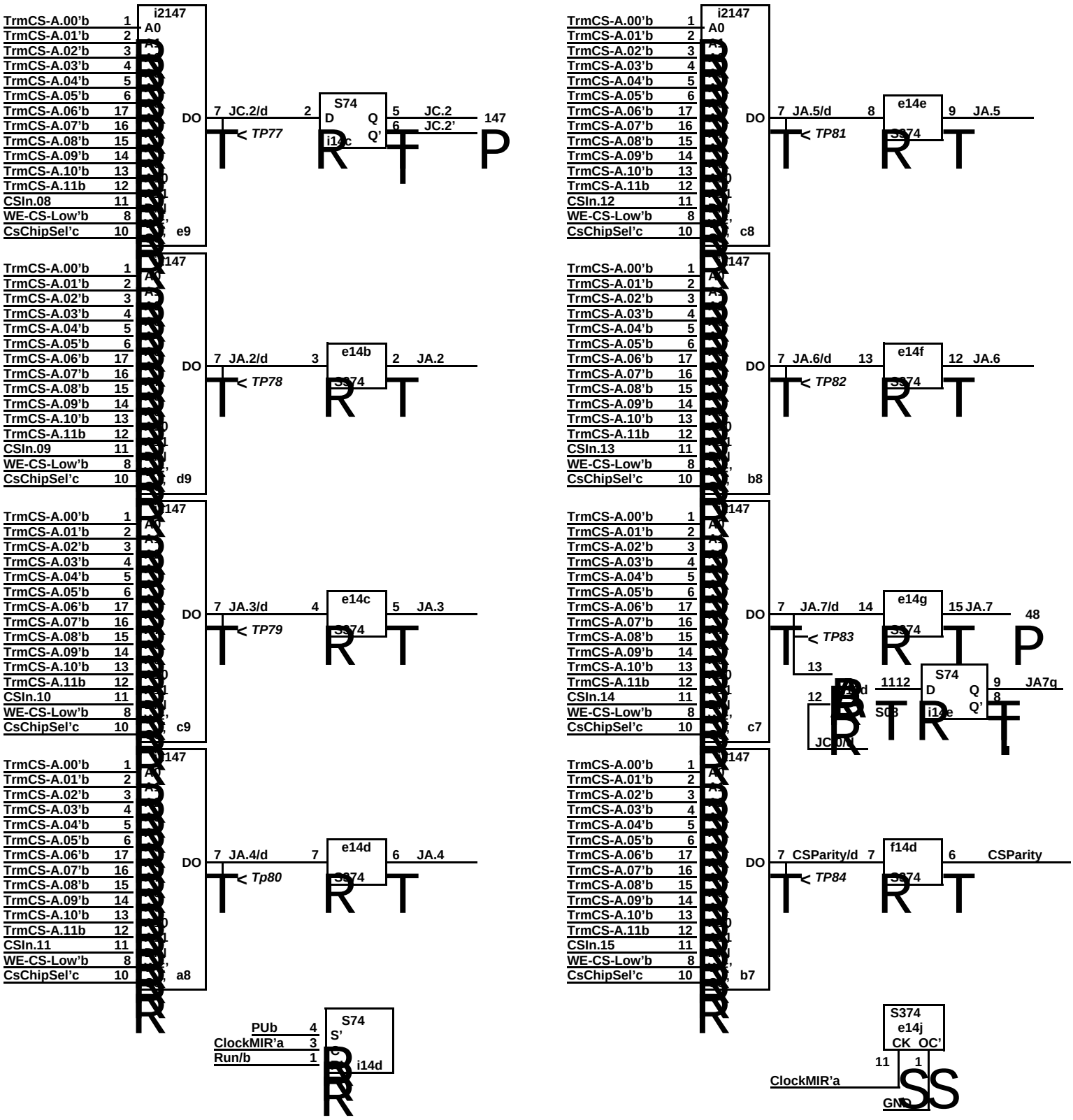
XEROX EOD	Project D0	Control Board Control Store 00:07	File D0cs04.sil	Designer Rosen	Rev Gc	Date 2/19/79	Page 04



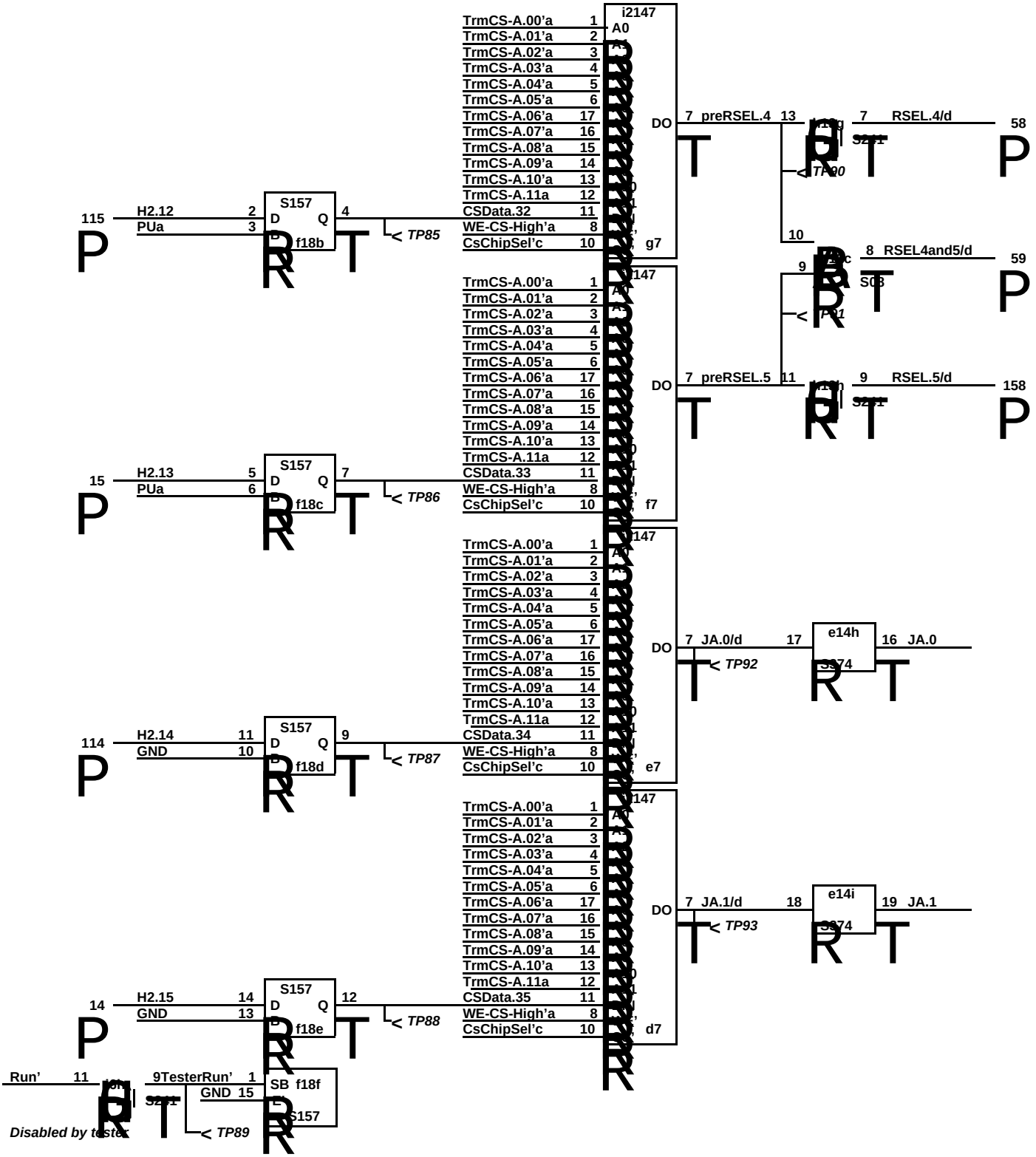
XEROX EOD	Project	Control Board Control Store 08:15	File	Designer	Rev	Date	Page
	D0		D0cs05.sil	Rosen	Gc	2/19/79	05



XEROX EOD	Project D0	Control Board Control Store 16:23	File D0cs06.sil	Designer Rosen	Rev Gc	Date 2/19/79	Page 06



XEROX EOD	Project D0	Control Board Control Store 24:31	File D0cs07.sil	Designer Rosen	Rev Gc	Date 2/19/79	Page 07



XEROX EOD	Project D0	Control Board Control Store 32:35	File D0cs08.sil	Designer Rosen	Rev Gc	Date 2/19/79	Page 08

Spare positions

FPLAT f1 — GND 10; VCC 20

FPLAT g1 — GND 10; VCC 20

60 ohm series plus 220 ohm pullup

16 pin network centered in 20 pin pattern

FPLAT a11

CS-A.00'a 2	VCC 19
CS-A.01'a 3	VCC 18
CS-A.02'a 4	TrmCS-A.00'a 17
CS-A.03'a 5	TrmCS-A.01'a 16
CS-A.04'a 6	TrmCS-A.02'a 15
CS-A.05'a 7	TrmCS-A.03'a 14
CS-A.06'a 8	TrmCS-A.04'a 13
GND 9	TrmCS-A.05'a 12
GND 10	TrmCS-A.06'a 11

FPLAT h1 — GND 10; VCC 20

FPLAT i1 — GND 10; VCC 20

FPLAT a9

CS-A.07'a 2	VCC 19
CS-A.08'a 3	VCC 18
CS-A.09'a 4	TrmCS-A.07'a 17
CS-A.10'a 5	TrmCS-A.08'a 16
CS-A.00'b 6	TrmCS-A.09'a 15
CS-A.01'b 7	TrmCS-A.10'a 14
CS-A.02'b 8	TrmCS-A.00'b 13
GND 9	TrmCS-A.01'b 12
GND 10	TrmCS-A.02'b 11

FPLAT h6 — GND 10; VCC 20

FPLAT a7

CS-A.03'b 2	VCC 19
CS-A.04'b 3	VCC 18
CS-A.05'b 4	TrmCS-A.03'b 17
CS-A.06'b 5	TrmCS-A.04'b 16
CS-A.07'b 6	TrmCS-A.05'b 15
CS-A.08'b 7	TrmCS-A.06'b 14
CS-A.09'b 8	TrmCS-A.07'b 13
GND 9	TrmCS-A.08'b 12
GND 10	TrmCS-A.09'b 11

149 J-TestResult' 13
Cycle0 2
ExcuseMe 3
JC.0 12
DisableCS-Adr 1

BranchBurp' 4 — BranchBurp 5 — < TP94

S260 1

C1RC 6 — BBurp' 3 — PartialCS-A.11' — StartFault' — ExcuseMe'

Run/a

RamClock 4
Cycle1 5
Cyc1RamClk' 6
ExcuseMe 6 — < TP95
PUb 1

12CS-A.11' 103

60 ohm series plus 220 ohm pullup

WriteLowCS' 10
BootWriteLowCS' 9
WE-CS-Low 8 — 21

WriteHighCS' 13
BootWriteHighCS' 12
WE-CS-High 11 — 121

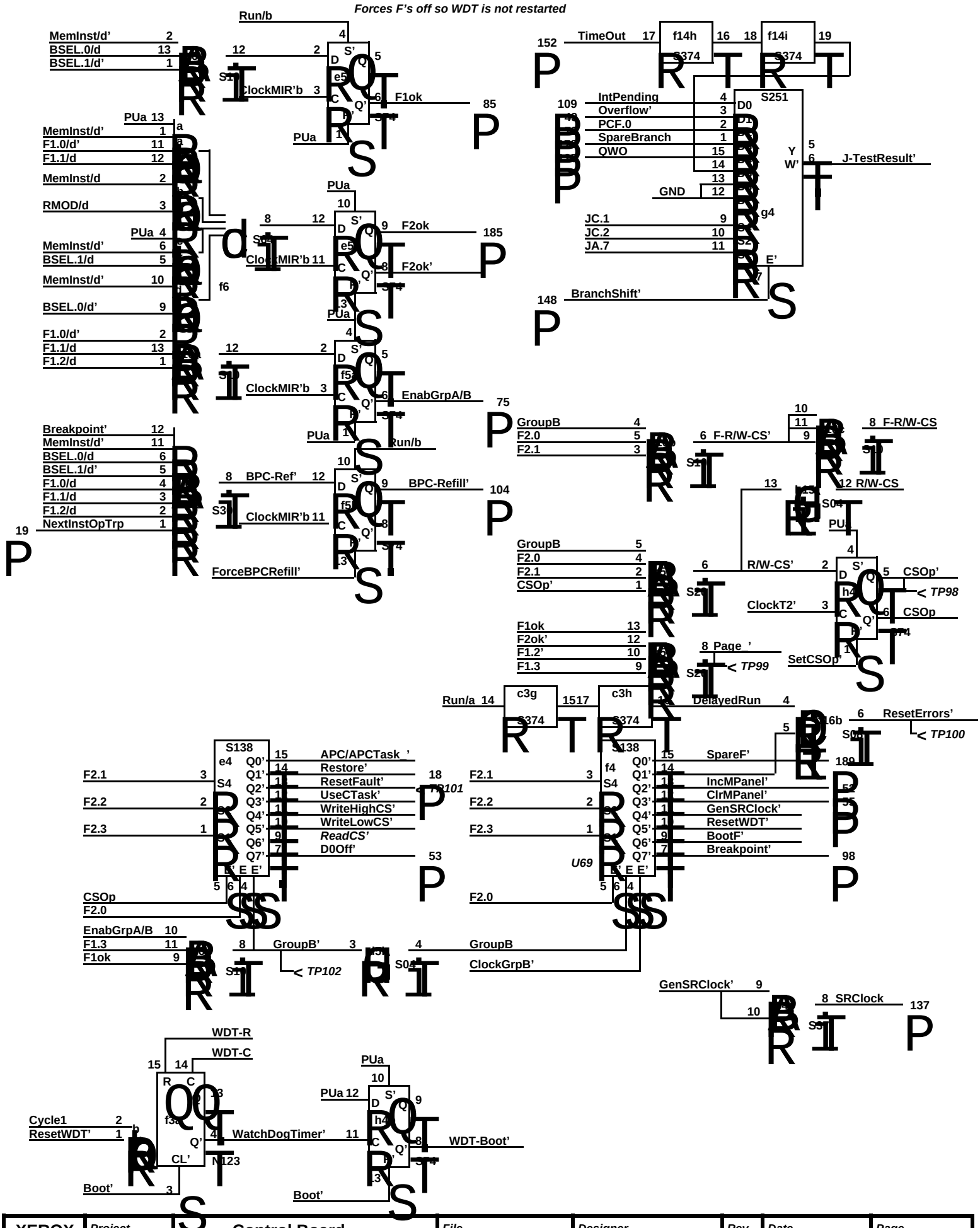
Prevents Glitches on WriteHighCS from inadvertantly causing write strobes
EarlyCycle1

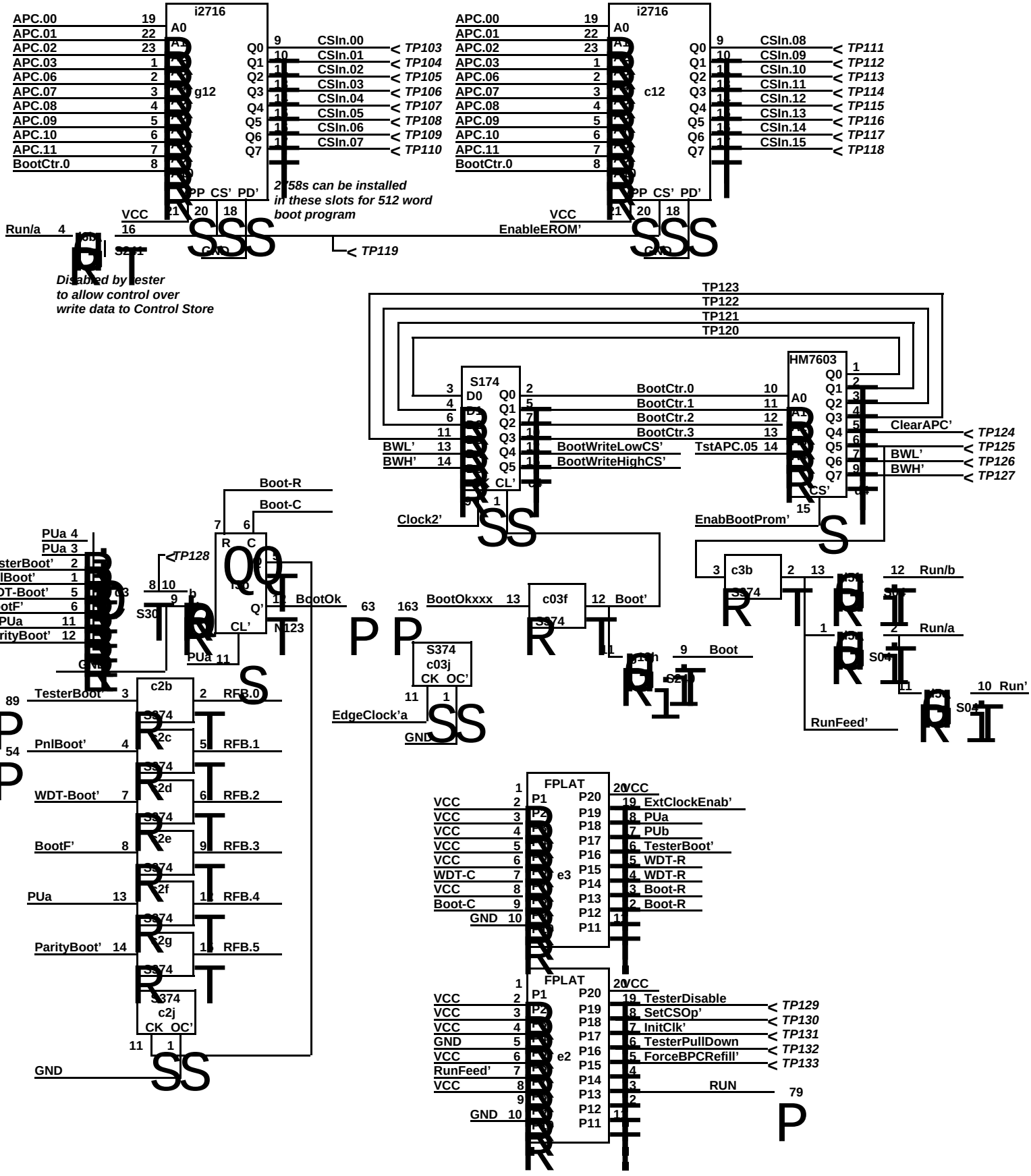
< TP96
< TP97

FPLAT a12

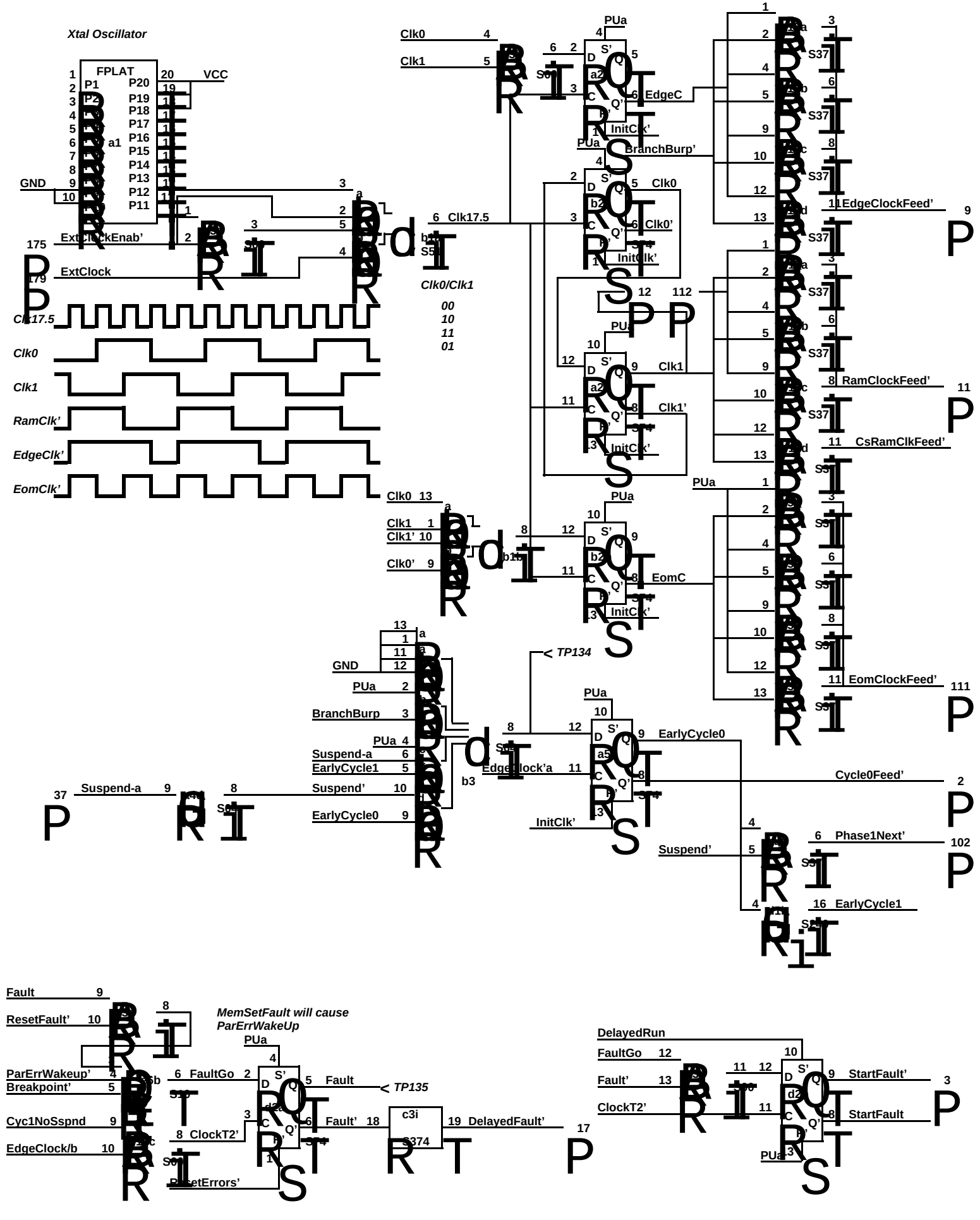
CS-A.11a 2	VCC 19
CS-A.11b 3	VCC 18
CS-A.10'b 4	TrmCS-A.11a 17
WEL'a 5	TrmCS-A.11b 16
WEL'b 6	TrmCS-A.10'b 15
WEH'a 7	WE-CS-Low'a 14
WEH'b 8	WE-CS-Low'b 13
GND 9	WE-CS-High'a 12
10	WE-CS-High'b 11

XEROX EOD	Project D0	Control Board Control Store Address&WE	File D0cs09.sil	Designer Rosen	Rev Gc	Date 2/19/79	Page 09

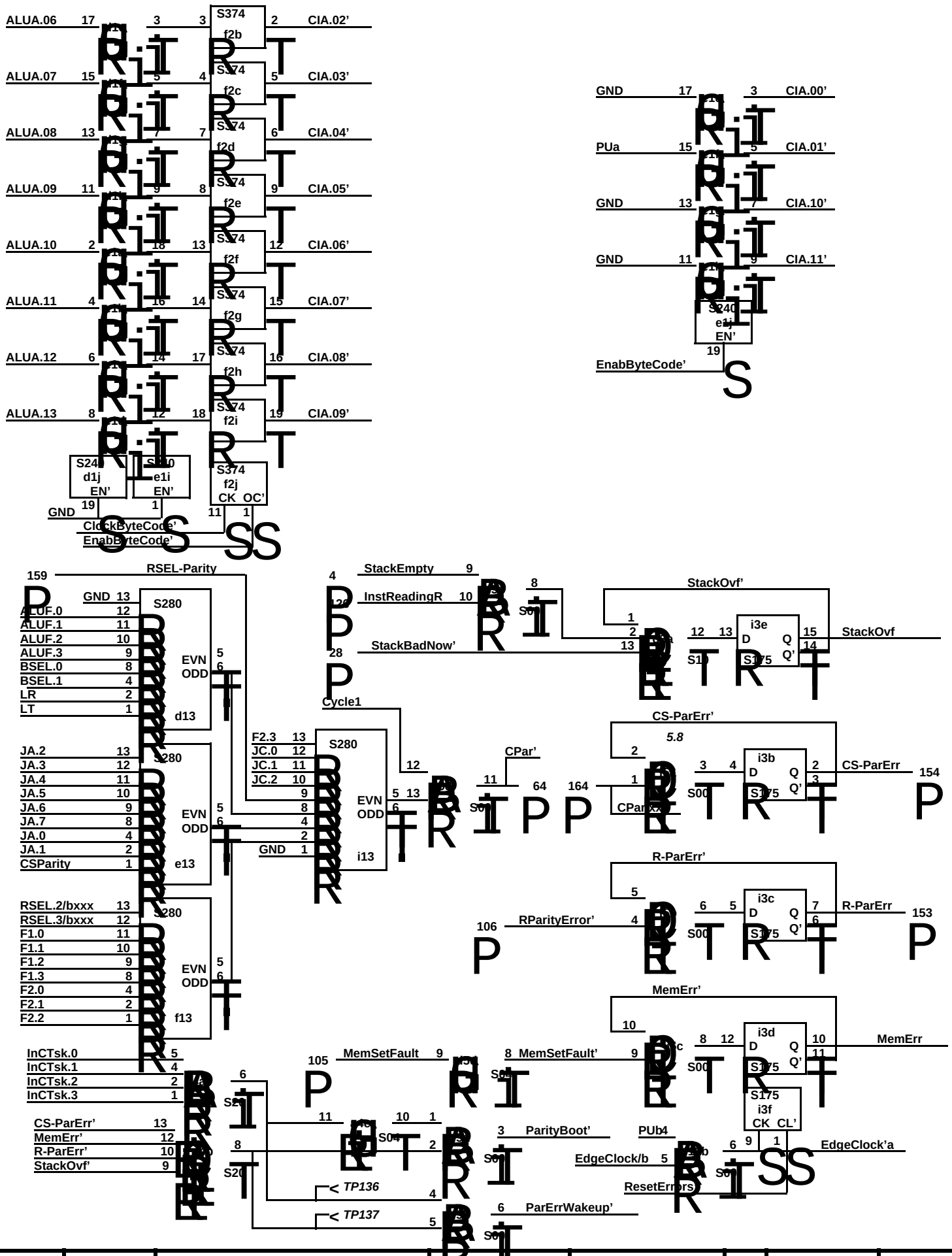

Forces F's off so WDT is not restarted
Run/b
MemInst/d'
BSEL.0/d
BSEL.1/d'
ClockMIR'b
F1ok
PUa
MemInst/d'
F1.0/d'
F1.1/d
MemInst/d
RMOD/d
MemInst/d'
BSEL.1/d
MemInst/d'
BSEL.0/d'
F1.0/d'
F1.1/d
F1.2/d
F2ok
F2ok'
f6
Breakpoint'
MemInst/d'
BSEL.0/d
BSEL.1/d'
F1.0/d
F1.1/d
F1.2/d
NextInstOpTrp
BPC-Ref'
BPC-Refill'
ForceBPCRefill'
EnabGrpA/B
Run/b
TimeOut
f14h
f14i
S374
IntPending
Overflow'
PCF.0
SpareBranch
QWO
GND
S251
J-TestResult'
JC.1
JC.2
JA.7
BranchShift'
GroupB
F2.0
F2.1
F-R/W-CS
F-R/W-CS'
R/W-CS
R/W-CS'
CSOp'
CSOp
ClockT2'
F1ok
F2ok'
F1.2'
F1.3
Page
SetCSOp'
Run/a
c3g
c3h
DelayedRun
ResetErrors'
S138
APC/APCTask_'
Restore'
ResetFault'
UseCTask'
WriteHighCS'
ReadCS'
D0Off'
SpareF'
IncMPanel'
ClrMPanel'
GenSRClock'
ResetWDT'
BootF'
Breakpoint'
U69
CSOp
F2.0
EnabGrpA/B
F1.3
F1ok
GroupB'
GroupB
ClockGrpB'
GenSRClock'
SRClock
WDT-R
WDT-C
Cycle1
ResetWDT'
WatchDogTimer'
Boot'
WDT-Boot'
TP98
TP99
TP100
TP101
TP102
XEROX
EOD
Project
D0
Control Board
F Decodes
File
D0cs10.sil
Designer
Rosen
Rev
Gc
Date
2/19/79
Page
10



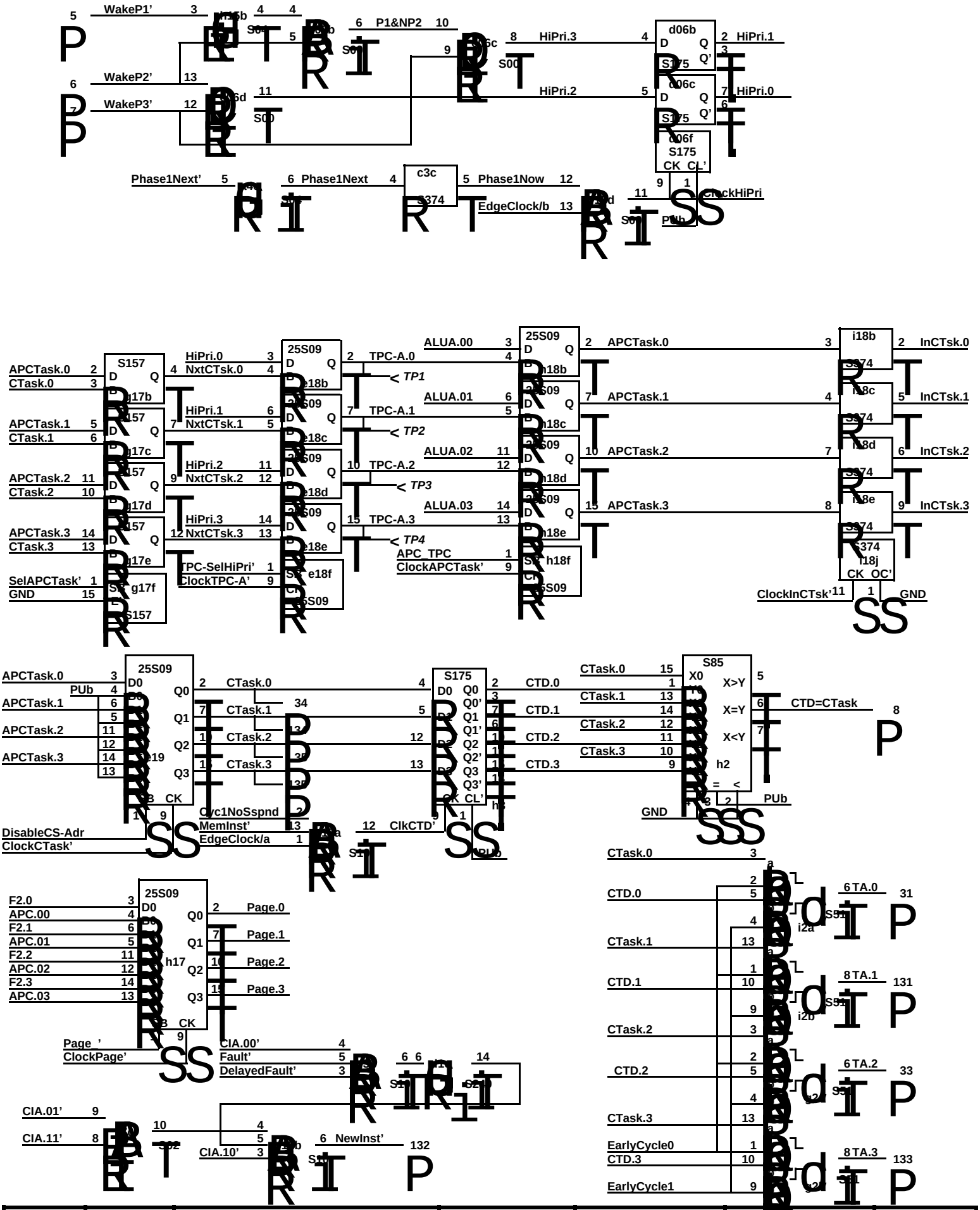
XEROX PARC/CSL	Project D0	Control Board Boot	File D0cs11.sil	Designer Rosen	Rev Gc	Date 7/18/80	Page 11



XEROX EOD	Project D0	Control Board Clock Generator	File D0cs12.sil	Designer Rosen	Rev Gc	Date 2/19/79	Page 12



XEROX EOD	Project D0	Control Board ByteCode, Parity	File D0cs13.sil	Designer Rosen	Rev Gc	Date 2/19/79	Page 13



XEROX EOD	Project D0	Control Board Page, Task Logic, NewInst	File D0cs14.sil	Designer Rosen	Rev Gc	Date 3/8/79	Page 14

Rev E to Rev F 3/8/78 Brian Rosen

1) The Clock Drivers on page 12 were moved from c1/d1 to a18/b18 to eliminate waveform distortions due to refelections at the connector that caused false clocking on some boards. This necesitated moving the TPC-A multiplexor (page 1) from b18 to g17, and the Wake-up encoder S00 from a18 to c06. The wake-up lines now have long stubs on this board. The HiPri register was also moved up next to the S00 encoder (from e01 to d06).

2) The S30 at g6 that makes BPC-Ref' (page 10) had Breakpoint' added to it. This prevents the BPC-Refill trap from occuring when the sucessor of a breakpointed instruction points to an instruction which has NextInst or Nextop specified.

3) The trap location for Fault and BPC refill were reversed by changin the term on CS-A.11 from BPC-Refill' to StartFault' (S20 at a6 on page 9). Faults trap to 1, BPC refill traps to 0. This forces a nextinst/nextop which both BPC refills and Faults to hit the fault handler rather than the BCP handler.

4) The EPROM sockerts were changed to allow 2716s or 2758s to be plugged in. This removes all dependancy on the +12/-5 supplies for booting, and allows a 1k boot program. This change also affected the bit tested to determine end of boot load (from APC.00 to APC.05, thus affecting TstAPC.00 on page 3 and page 11)

5) A new Clock was added for the EOM board (ROS printer). This clock, EomClock, is a 35ns (nominal) squarewave, with a clock driver. See page 12.

6) Final testability changes were made, they include: a) A new signal, TesterDisable which is an independent pullup resistor on a new plat at e2 (page 11). This signal enables the S241 on page 3 which allows tester control of TstAPC.05, Enable BootProm, EnabCIA. b)another new signal, also an independent pullup (page 11) which allows tester to force CSOp to set. c) an S51 at b1 now lets the tester turn off the oscillater with a new signal-ExtClockEnab'. This signal is pulled up on the e3 plat instead of ExtClock'. c)the clock generator flip flops can be initialized by the InitClk' signal, which is pulled up on the e2 plat.

7) a minor improvement was achieved by eliminating the S32 at d6. Only one section was used (SRData, page 10) and an unused S32 section was available in the e16 S32. d6 is now empty

Rev F to Rev G 4/17/78 Brian Rosen

1) The chip enables for the TPC rams (control sections on pages 1 and 2) were run through an S241 controlled by DisableTester to allow tester control of APC inputs

2) The Run/a signal was run through another tester controlled S241 gate to allow tester control of the EPROMs (page 11)

3) The select input of the data in mux for bits 32:35 of the control store (page 8) was modified to run through another S241 gate to allow tester control of the data input to these 4 RAMs.

4) A new pull down resistor was added to the e2 plat (page 11) creating the signal TesterPullDown. This is the control input to the tester S241 (page 3)

5) The signal ChipSelect' (an input to all 2147 RAM chips, pages 4:8) was broken up into 3 separate nets, eachj fed from an S410 gate at i6 (page 3, nets CsChipSel'a, CsChipSel'b, and CsChipSel'c)

6) An adder, S283 was added between CIA and the TPC ram inputs (page 1) to make the return address CIA+1 (carries propogate throug 4 bits only). New chip is at c1.

7) The clock term for CTD (page 13) needed to have MemInst' as an input. Added a new gate (e15a) to make this term.

Rev G to Rev H 9/8/78 Brian Rosen

1) The Abort' term on ClockTPC-A' (g15.11) page 2 is erroneous, it was removed.

2) The Cycle1 term on RunningT2 came very late for some qualifier terms. It was changed to Cycle0Feed' thus cutting two gate delays

3) The Complement of the actual BranchBurp signal is needed for new clock driver scheme (see note 4 below). Added an invertor to BranchBurp using a4.3 and a4.4 creating BranchBurp'. The signal from b6.3 (page 9) had it name changed to BBurp'

4) Clock Drivers (page 12) were changed from S32s to S37s. This changed all inputs on a18, b18 and c5.

5) Cycle0Feed' is too late. The S37 that created this signal (page 12) was deleted. Cycle0Feed' now come from a5.8
this affected the name of the signal at b3.5 (was EarlyCycle1, now Cycle0Feed')
This EarlyCycle0 is also used on a10 (page 9) and i2/g2 (page 13). The next revision (I) will remove some of these loads
For now, they are all Cycle0Feed'

Rev H to Rev I - 11/18/78, C. Thacker

1) The register ByteCode is added (f2,d1,e1, pg13). This register holds ALUA[6:13]' for one cycle following NextInst, so that the bytecode can be written into TPC by the subsequent RETURN. This allows task switches between bytecodes.

2) The signal SRData (buffered H2.15) has been deleted. This requires a backplane change (pg 4,5,10).

3) The branch logic on pg 10 is changed to add IntPending (in place of Disp999), QWO, and a SpareBranch.

4) The signal NxtInNoTsk' is generated in c6a (pg2). This signal is true if a task switch will NOT occur in the RETURN following a NextInst. This signal determines the source of APC data during NextInst.
5) The signal NxtInstRTN' is generated in i17c (pg2). This signal will be asserted by all RETURNs following NextInsts, and will cause ByteCode+1 rather than CIA+1 to be written into TPC.
6) The function decoder on pg 10 is changed to bring out SpareF', and rename DispCnt' and DispClr' to be IncMPanel' and ClrMPanel'
7) The generation of RUN(pg11) is different. The feed signal from d4.6 is latched, RUN is generated on platform e2.
(NOTE: e2 is changed to 18pins). PwrBoot' is generated in e16d.
8) CSOP (pg10) is clocked by clockT2' (used to be called ClkFault', pg 12).
9) EarlyCycle1 (pg 12) was added to reduce loading on Cycle0Feed'.
10) Clk1 is brought to the backplane (E12 -> E112) so that a delay can be inserted to reduce the width of RamClock.
11) a5.13 (pg 12) is connected to InitClk' rather than to PUa.
12) Stack overflow logic is added on pg 13.
13) NewInst (used to be an F) is generated on pg14.
14) Added TimeOut branch condition (pg10) and brought R-ParErr and CS-ParErr to the edge connector (pg 13).

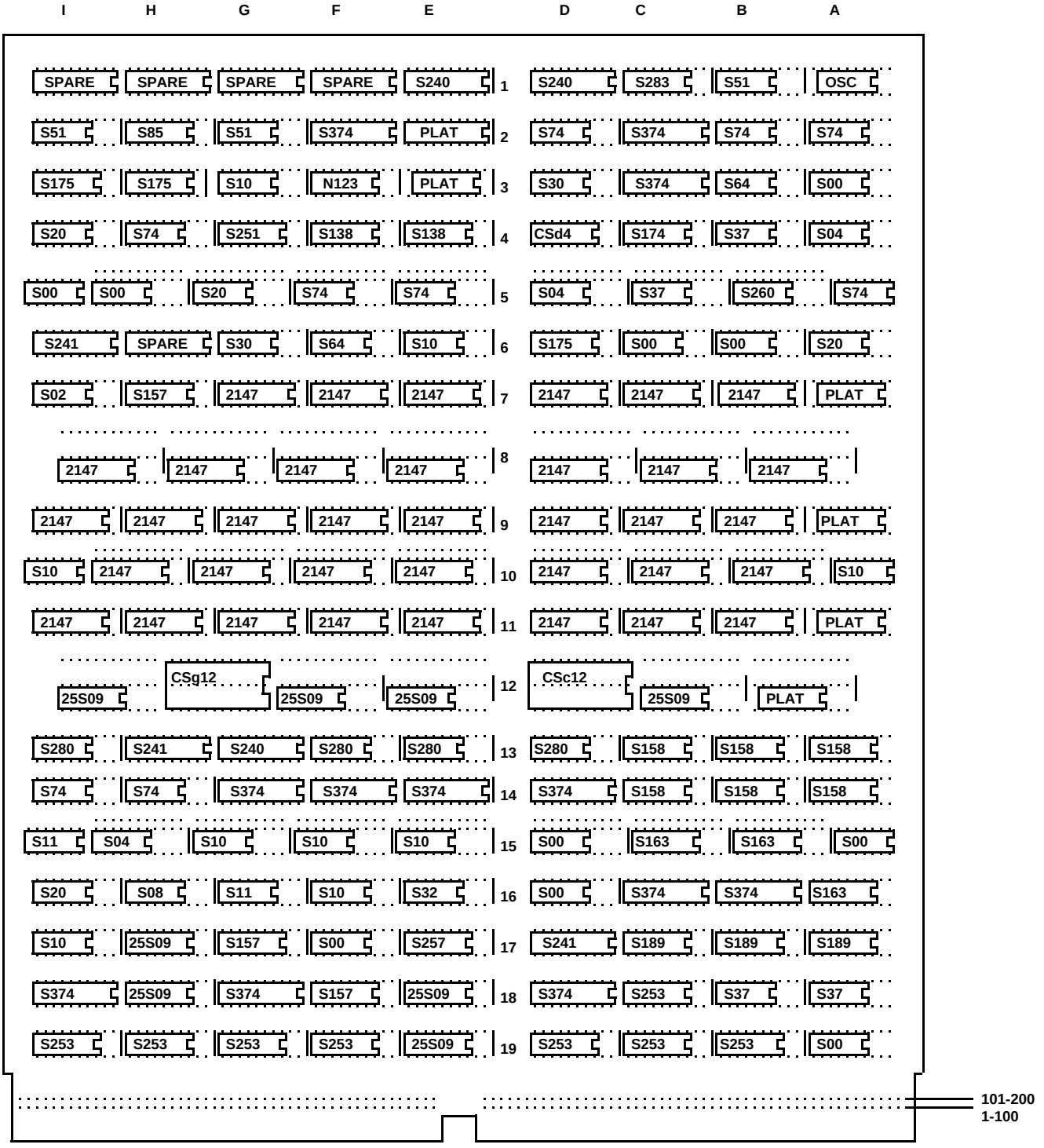
Changes to revision Ga (2/18/79 - CT)

1) Changed all plats to 20 pins on logic diagrams to cause ROUTE to do no trace cuts.
2) Added synchronizer on TimeOut (pg 10)
3) Changed D0Off' to E53, ClrMPanel' to E55 (pg 10).
4) Added spare IC's in positions f1, g1, h1, i1, h6.

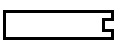
Rev Ga to rev Gb (3/8/79 - CT)

1) Added g3b, d1c on pg 14. This change keeps NewInst from occurring when the first microinstruction of a bytecode is aborted.

Rev Gb to rev Gc (7/17/80 - CT) Eliminated signal PwrBoot', changed RFB register clocking (pg 11).



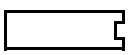
20pins: A



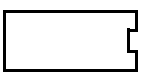
16pins: B

14pins: C

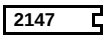
22pins: D



24 pins: E



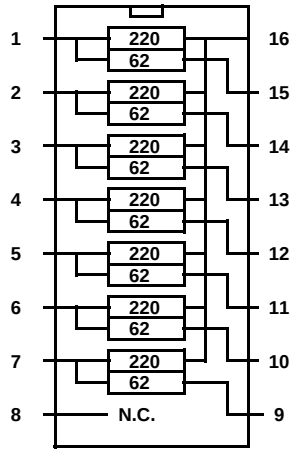
18 pins: F



Note: The short vertical lines indicate filter capacitor locations. (123 Total)

XEROX	Project		File	Designer	Rev	Date
CSL	D0	Module Layout- D0 Control Store	D0csLayout.sil	Rosen	Gc	7/18/80

Plats in locations: a7, a9, a11, a12



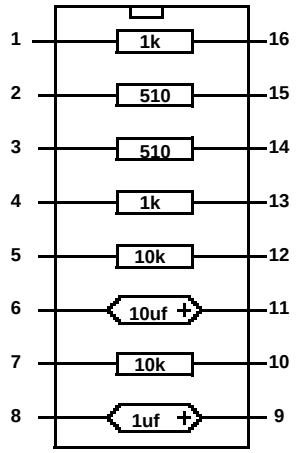
all resistors 1/8 watt

Note: Bourns has made a custom network for this platform.

16 pin platforms plugged into the middle of the 20 pin pattern

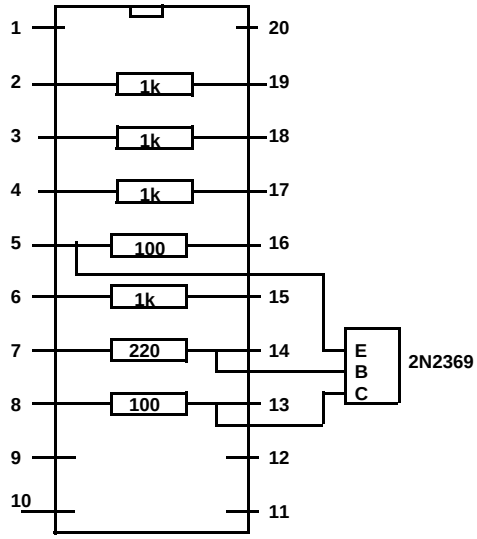
Pin 1 of plat goes in pin 2 of pattern

Plat in location e3



all resistors 1/4 watt
all capacitors Tantalum

Plat in location e2



all resistors 1/4 watt

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