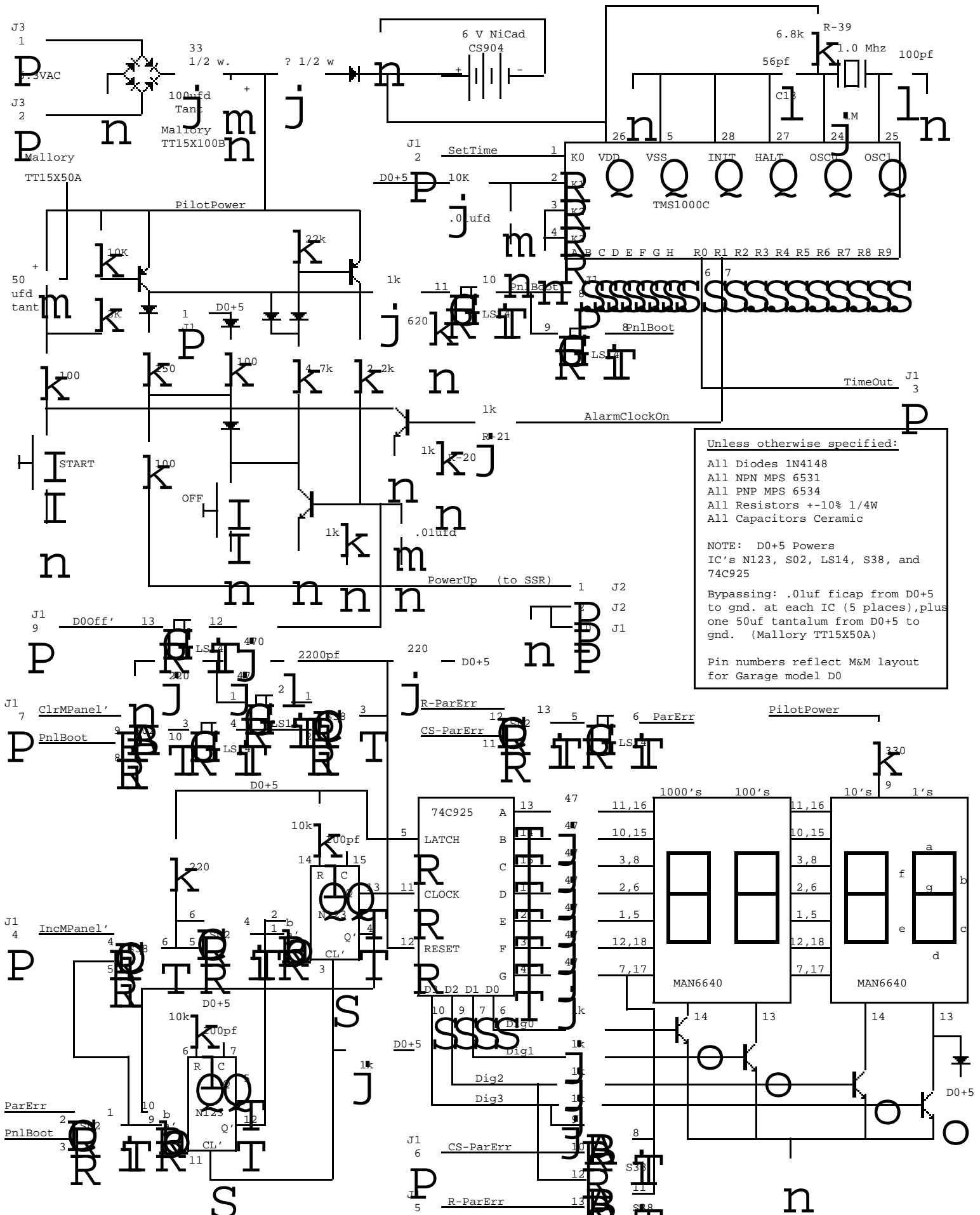


BACKPANEL ADD-DELETE LIST

CUT TRACE J-1.4 - GROUND

ADD THE FOLLOWING WIRES:

3.47 TO 5.147
5.147 TO 6.147
6.147 TO 7.147
7.147 TO 8.147
8.147 TO 9.147
9.147 TO 10.147
10.147 TO 11.147
11.147 TO 12.147
12.147 TO 13.147
13.147 TO 14.147
14.147 TO 15.147
15.147 TO 16.147
4.47 TO 5.47
5.47 TO 6.47
6.47 TO 7.47
7.47 TO 8.47
8.47 TO 9.47
9.47 TO 10.47
19.47 TO 11.47
11.47 TO 12.47
12.47 TO 13.47
13.47 TO 14.47
14.47 TO 15.47
15.47 TO 16.47
1.89 TO 3.49
2.75 TO 4.77
3.172 TO 4.79
1.4 TO 2.6
1.14 TO 1.138
1.28 TO 2.85
1.125 TO 2.16
1.126 TO 3.18
1.109 TO 3.8
1.132 TO 3.5
1.113 TO 1.13



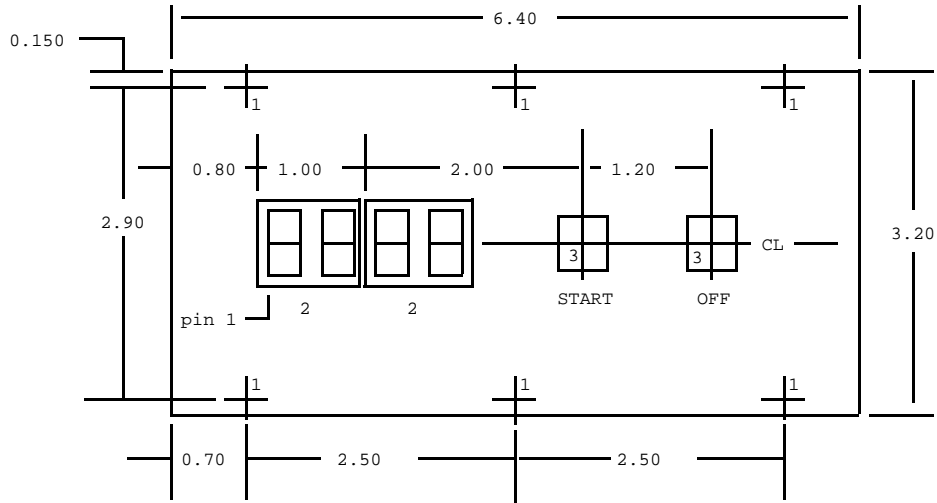
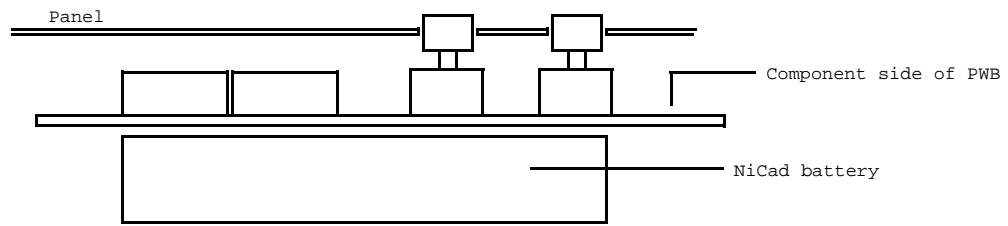
Unless otherwise specified:

- All Diodes 1N4148
- All NPN MPS 6531
- All PNP MPS 6534
- All Resistors +/-10% 1/4W
- All Capacitors Ceramic

NOTE: D0+5 Powers IC's N123, S02, LS14, S38, and 74C925

Bypassing: .01uF ficap from D0+5 to gnd. at each IC (5 places), plus one 50uF tantalum from D0+5 to gnd. (Mallory TT15X50A)

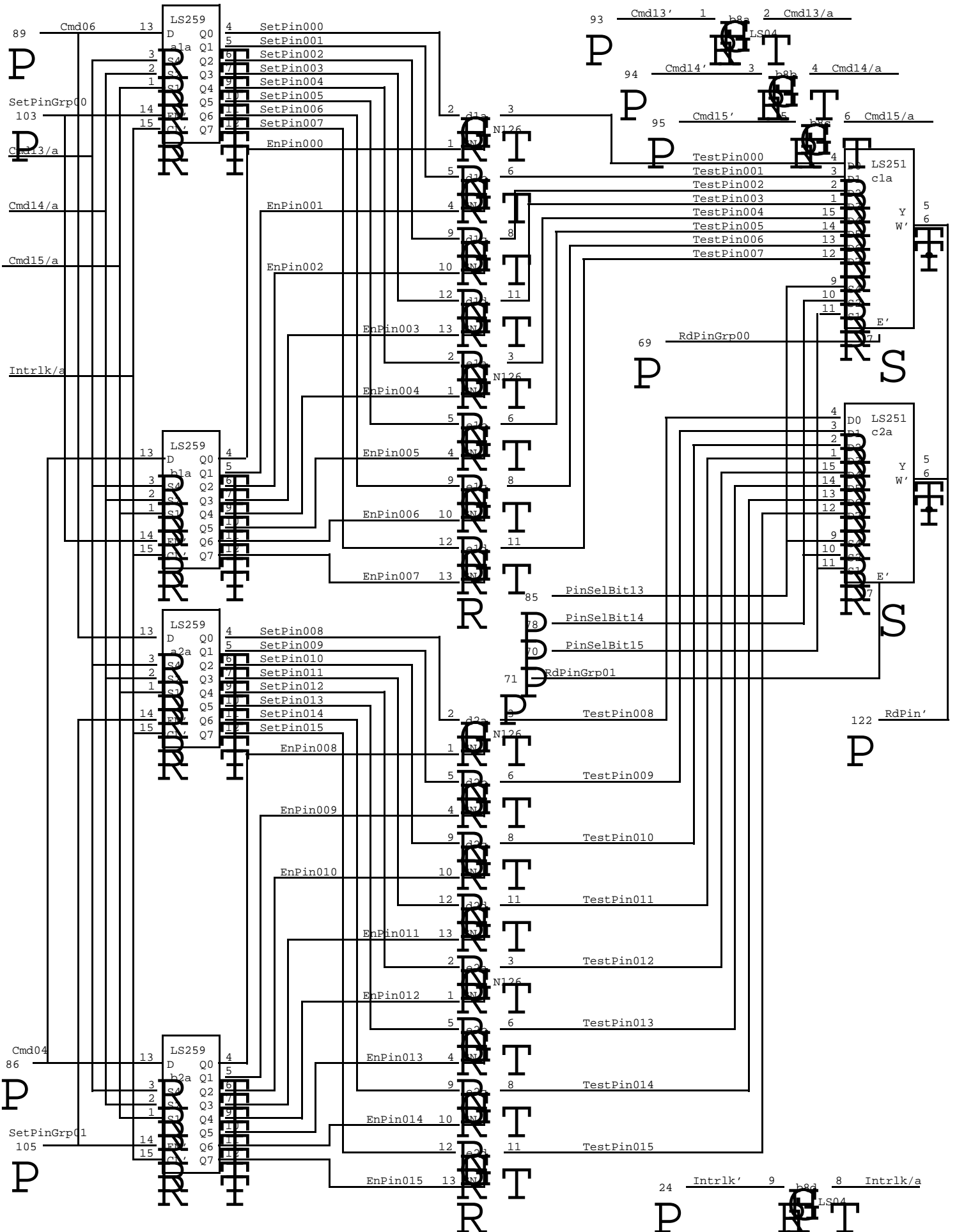
Pin numbers reflect M&M layout for Garage model D0

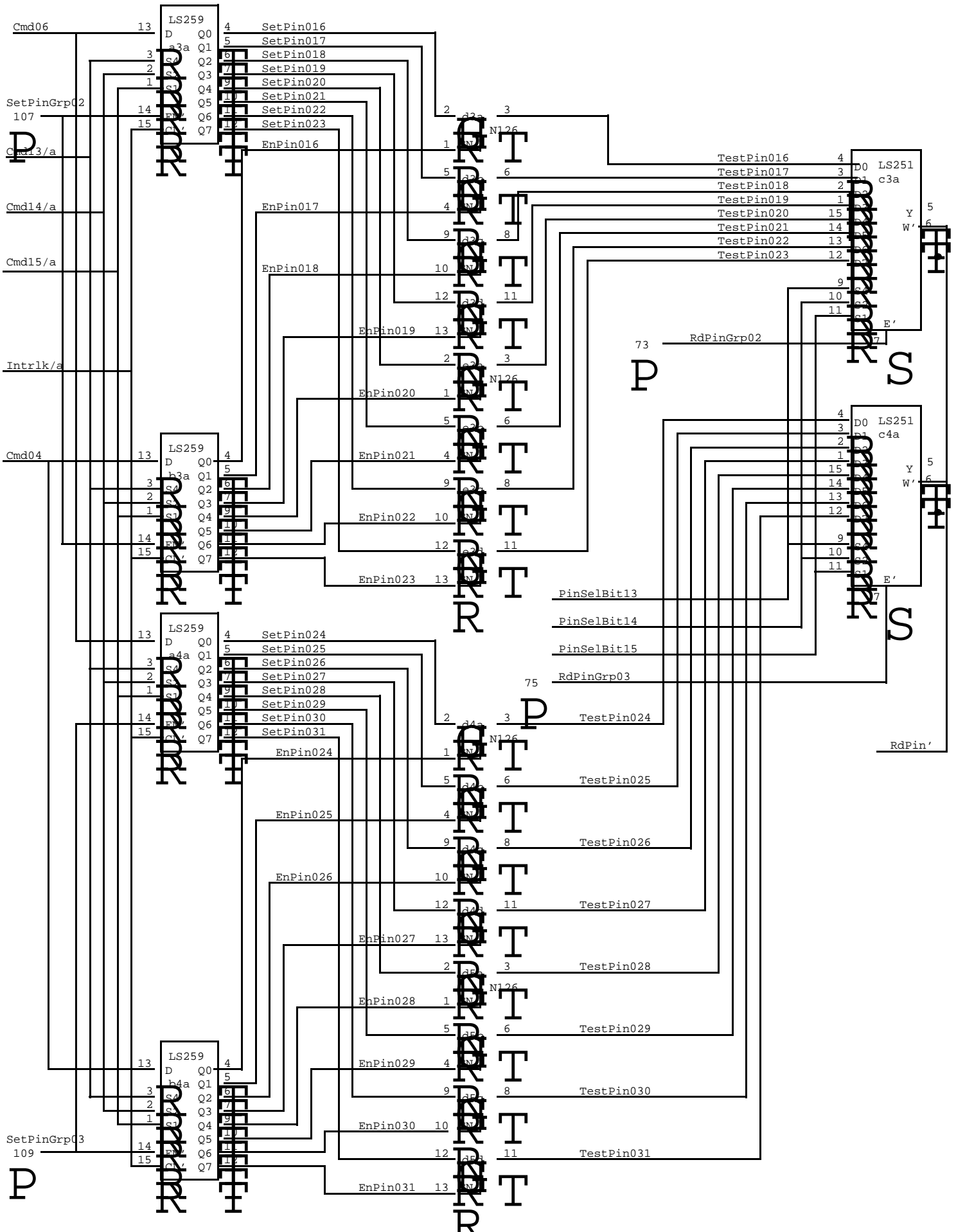


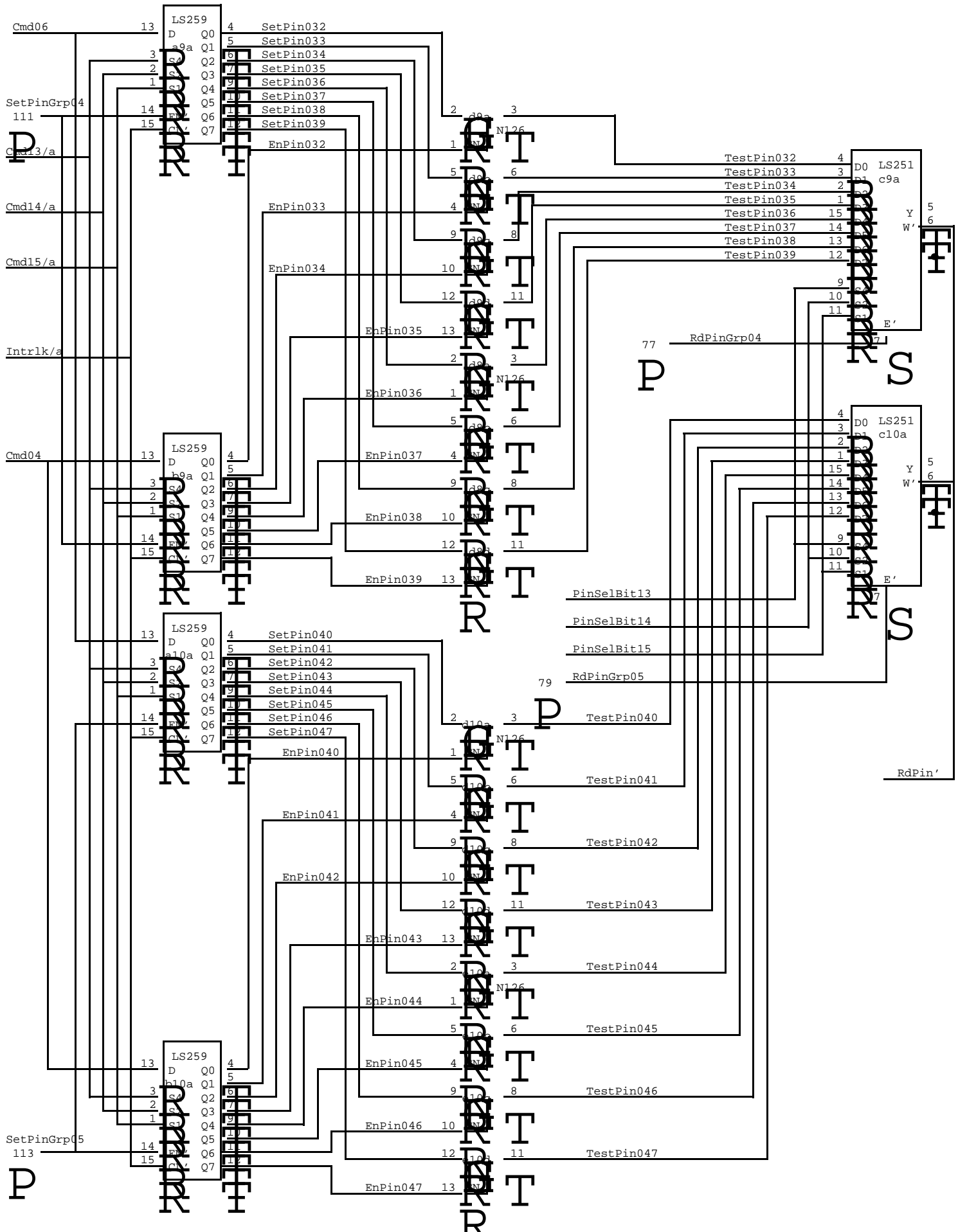
Notes:

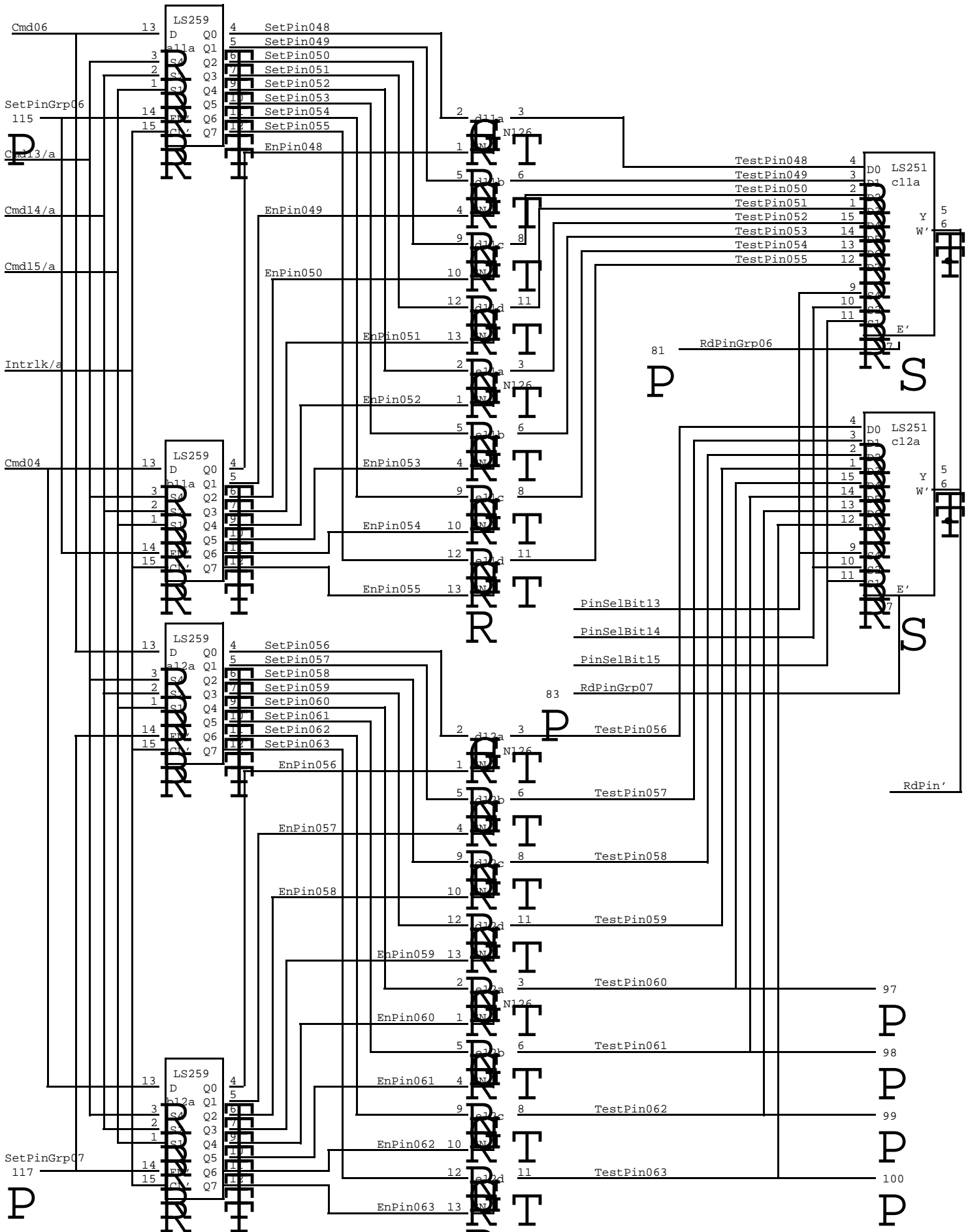
- 1) Mounting holes .188 dia, 6 places
- 2) 7-segment displays are Monsanto MAN6640. Package is 18 pins, 2 rows on .6 centers. Pin 1 is as shown.
- 3) START and OFF are C&K 8221 Momentary contact buttons with .465 square button.
- 4) J1, J2, and J3 in the schematic are not connectors, but are closely spaced groups of holes suitable for connecting discrete wires.
- 5) The TMS 1000C is a 28-pin DIP. Pin-to-pin spacing is .100, row to row spacing is .600.
- 6) The NiCad battery will be attached to the board with two cable clamps secured to the mounting screws.

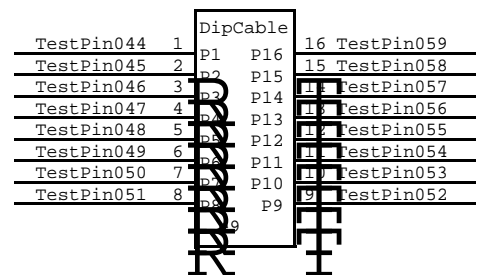
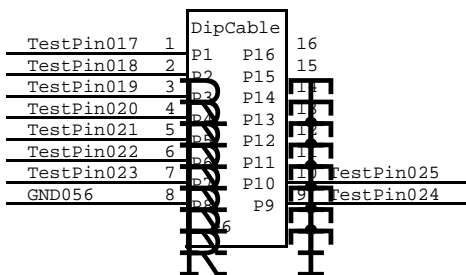
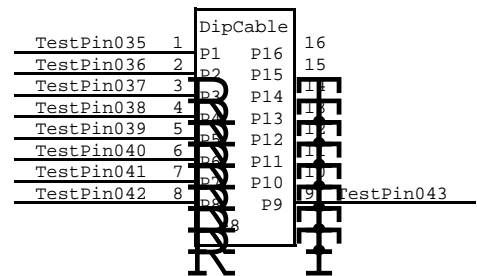
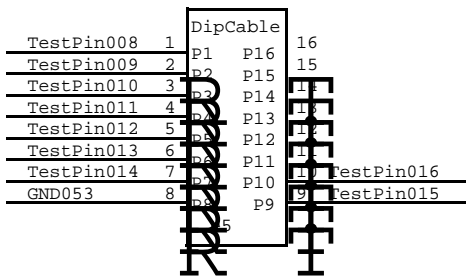
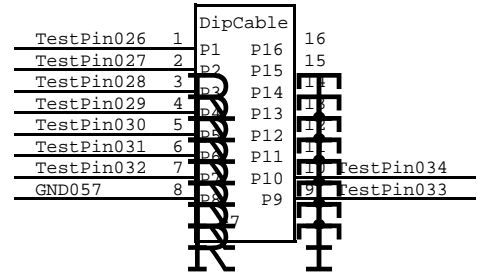
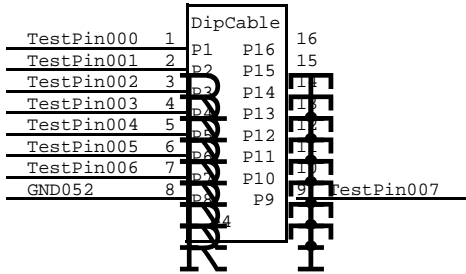
XEROX EOD	Project D0	Maintainance Panel	File D0MP02.sil	Designer Rosen	Rev Ga	Date 3/7/79	Page 02
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D0 Tester Connector Pin Assignment

DIP CONN	D0 CONNECTOR PIN from			
	MODULE			
	B	C	D	E
e4--1	2	102	52	152
2	3	103	53	153
3	4	104	54	154
4	5	105	55	155
5	6	106	56	156
6	7	107	57	157
7	8	108	58	158
9	9	109	59	159
e5--1	11	111	61	161
2	12	112	62	162
3	13	113	63	163
4	14	114	64	164
5	15	115	65	165
6	16	116	66	166
7	17	117	67	167
9	18	118	68	168
10	19	119	69	169
e6--1	21	121	71	171
2	22	122	72	172
3	23	123	73	173
4	24	124	74	174
5	25	125	75	175
6	26	126	76	176
7	27	127	77	177
9	28	128	78	178
10	29	129	79	179

DIP CONN	D0 CONNECTOR PIN from			
	MODULE			
	B	C	D	E
e7--1	31	131	81	181
2	32	132	82	182
3	33	133	83	183
4	34	134	84	184
5	35	135	85	185
6	36	136	86	186
7	37	137	87	187
9	38	138	88	188
10	39	139	89	189
e8--1	41	141	91	191
2	42	142	92	192
3	43	143	93	193
4	44	144	94	194
5	45	145	95	195
6	46	146	96	196
7	47	147	97	197
8	48	148	98	198
9	49	149	99	199
e9--1				
2				
3				
4	T	T	T	T
5	E	E	E	E
6	S	S	S	S
7	T	T	T	T
9				
10	C	C	C	C
11	L	L	L	L
12	I	I	I	I
13	P	P	P	P
14				
15				
16				

The D0 Tester modules C, D, and E are electrically identical to module B. The only difference is in the logical identity of the signals and the backpanel wiring. The following table lists the changes in signal names for each module. Backpanel pin connections have been prepared, and are filed under the name D0TesterBP1.bravo.

SIGNAL NAME	MODULE			
	B	C	D	E
SetPinGrp	00-07	08-15	16-23	24-31
RdPinGrp	00-07	08-15	16-23	24-31
SetPin	000-063	064-127	128-191	192-255
EnPin	000-063	064-127	128-191	192-255
TestPin	000-063	064-127	128-191	192-255
Cmd	13/a-15/a	13/b-15/b	13/c-15/c	13/d-15/d
Intrlk/	a	b	c	d

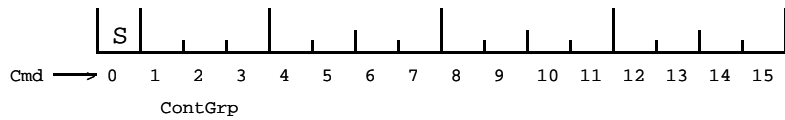
Module Signal Names

D0 Tester Command Summary

8/29/77

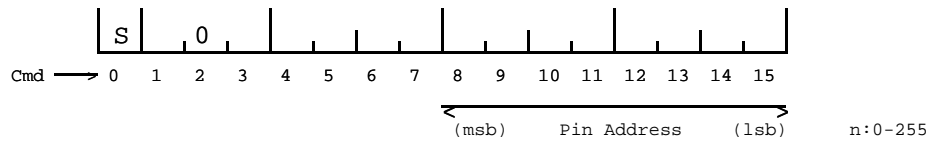
CARTER TSENG

UTILOUT (177016B):



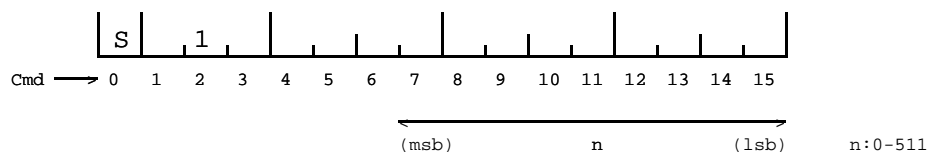
- 0 : Pin Control (Read & Set)
- 1 : Clock Control
- 2 : Load RAM Address
- 3 : Load RAM Data
- 4 : Load Data Byte A & B (Alto to D0)
- 5 : Read Data Nibble a,b,c & d (D0 Output or internal)
- 6 & 7 : (not used)

PIN CONTROL:



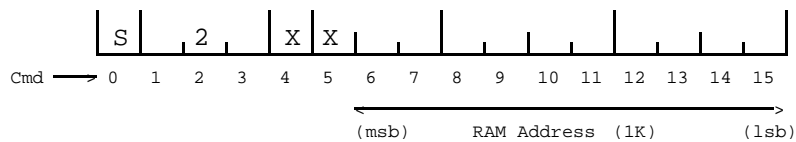
- bit 4 : Enable Pin n drive
- bit 5 : Set pin n to bit 6
- bit 6 : pin n drive state
- bit 7 : Read pin n by UTILIN04

CLOCK CONTROL



- bit 4 : to boot
- bit 5 : to run n clockstake precedence over bit 6)
- bit 6 : to run n instructions
- n>255:to run clock continuously

LOAD RAM ADDRESS



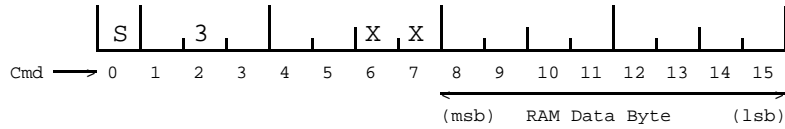
X: not used

D0 Tester Command Summary (Conti.)

8/29/77

CARTER TSENG

LOAD RAM DATA



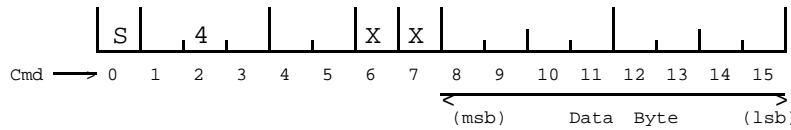
bit 4 : load data to most significant byte of output reg.
 bit 5 : load data to least significant byte of output reg.

4	5	Function
0	0	X
0	1	B
1	0	A
1	1	AB



Byte → A B

LOAD DATA BYTE



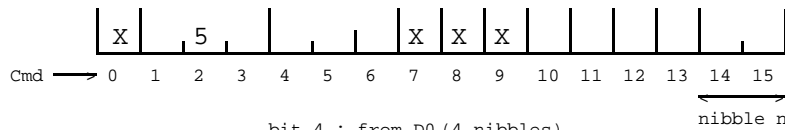
bit 4 : load data to most significant byte of output reg.
 bit 5 : load data to least significant byte of output reg.

4	5	Function
0	0	X
0	1	B
1	0	A
1	1	AB



Byte → A B

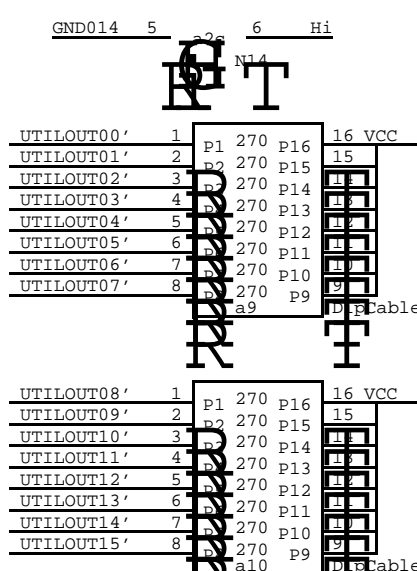
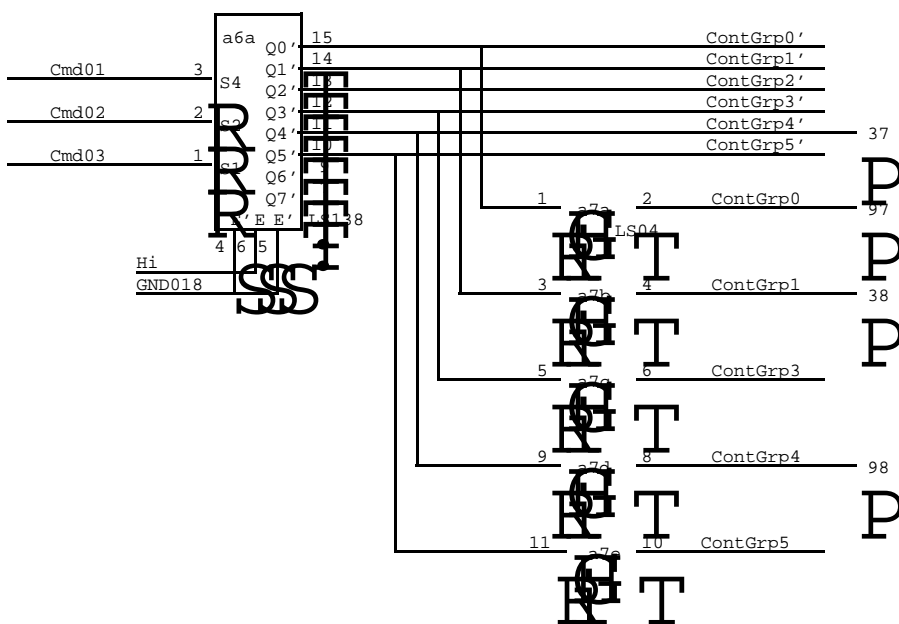
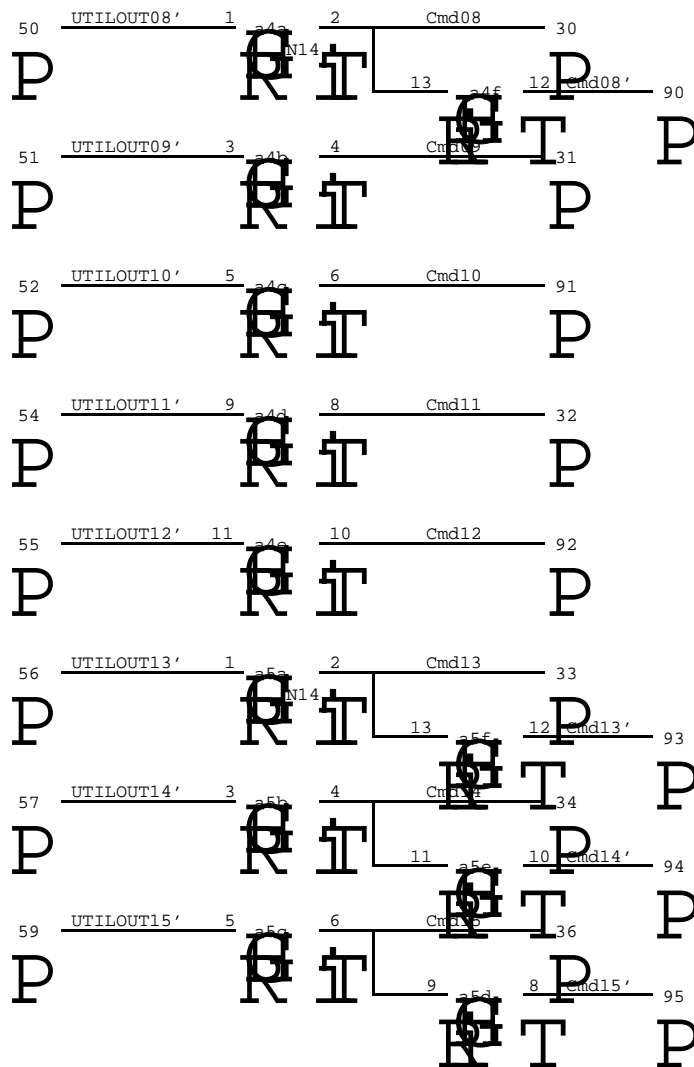
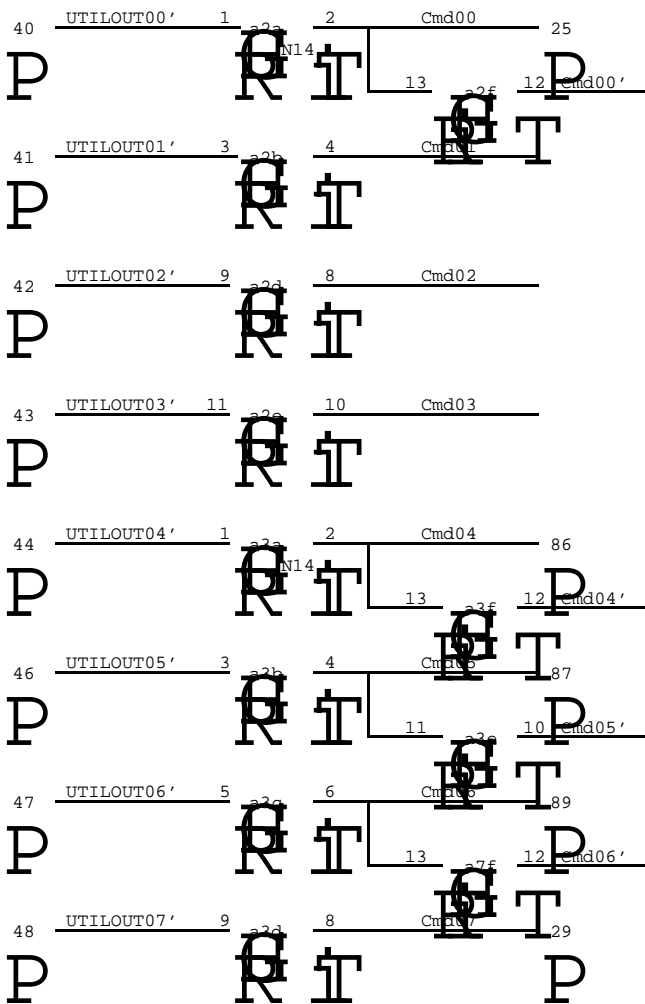
READ DATA NIBBLE



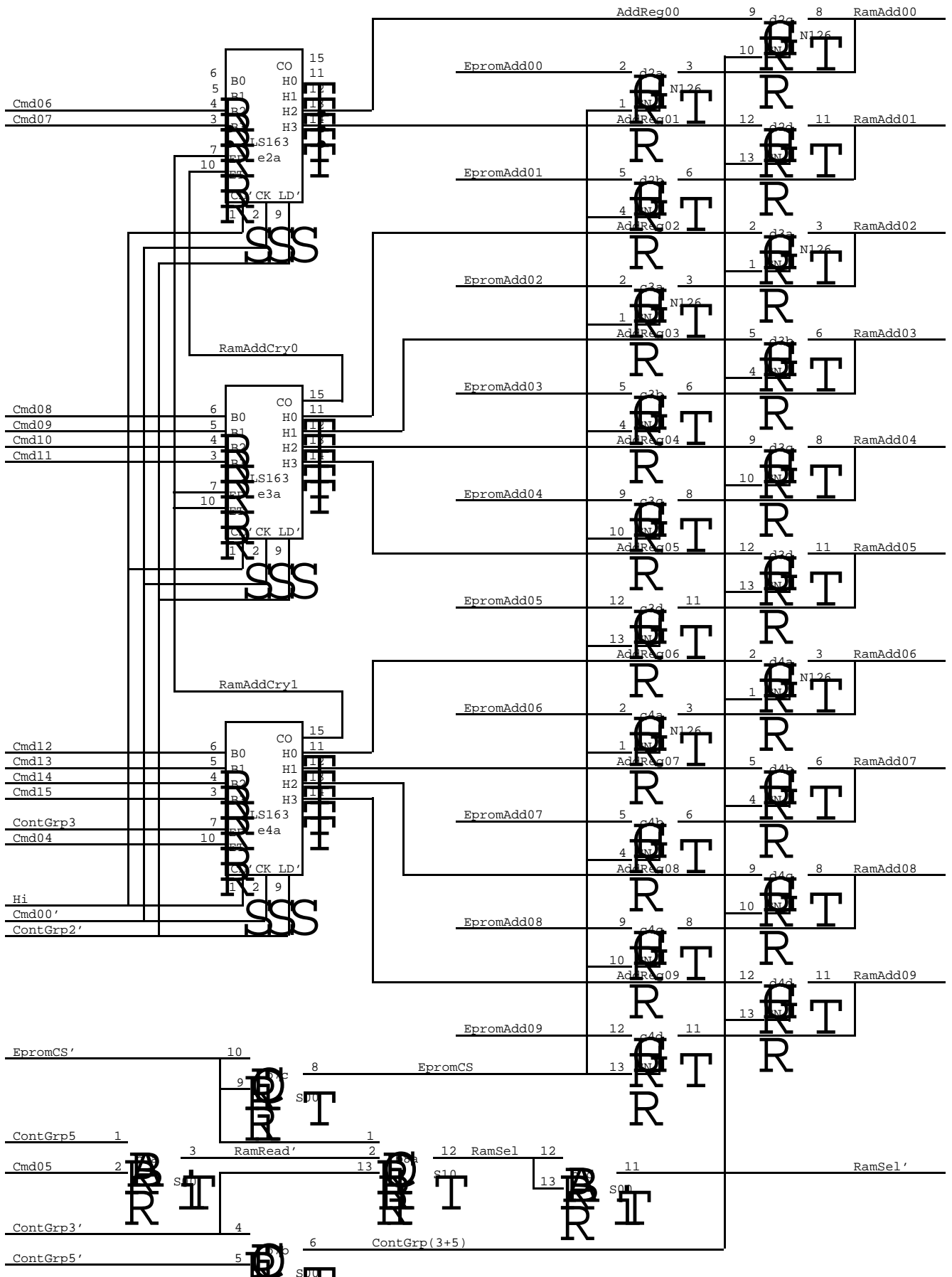
bit 4 : from D0 (4 nibbles)
 bit 5 : from RAM Data (4 nibbles)
 bit 6 : from RAM Address (3 nibbles)
 bit 10 : Turn around test on UTILIN[00]
 bit 11 : Turn around test on UTILIN[01]
 bit 12 : Turn around test on UTILIN[02]
 bit 13 : Turn around test on UTILIN[03]

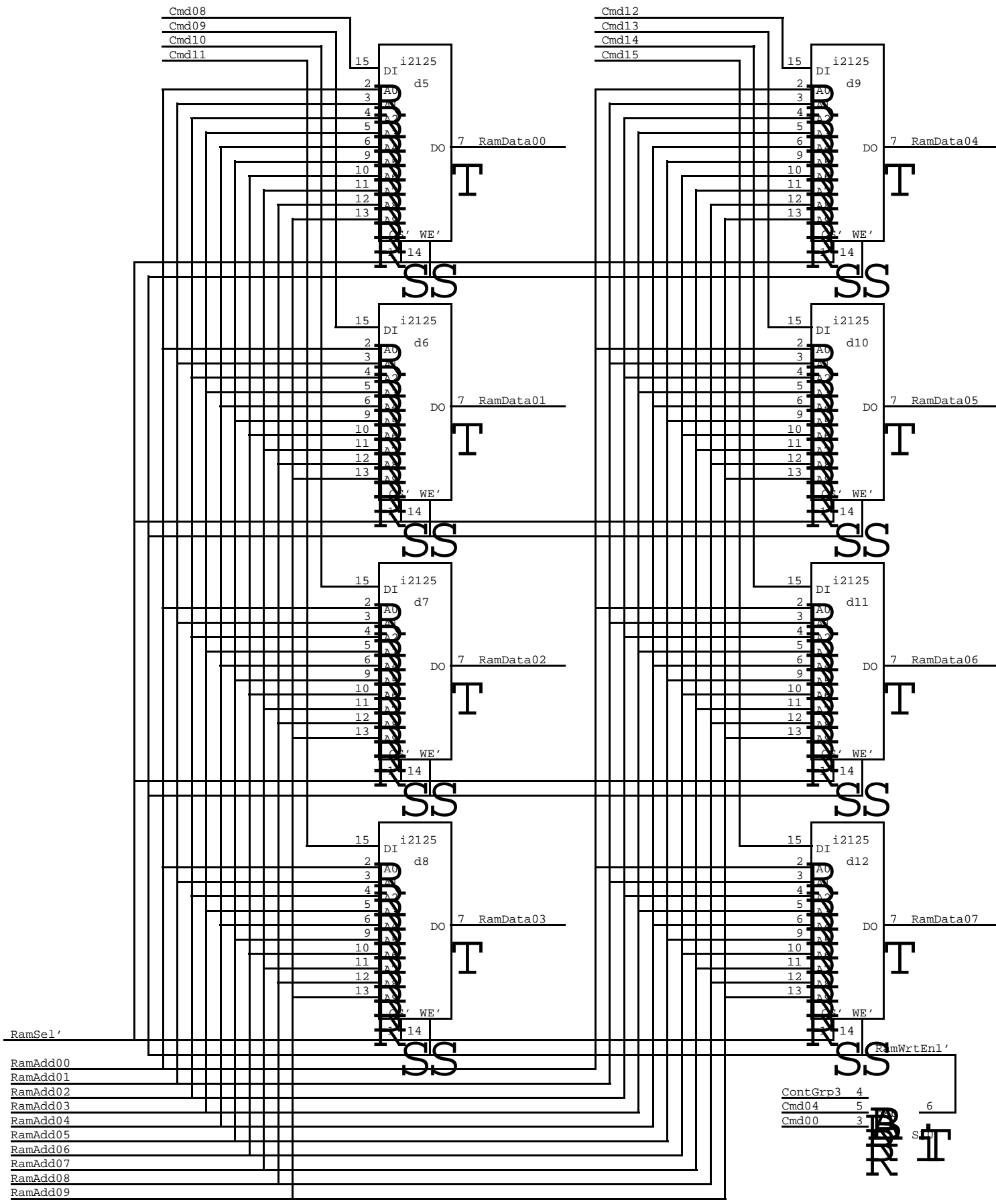


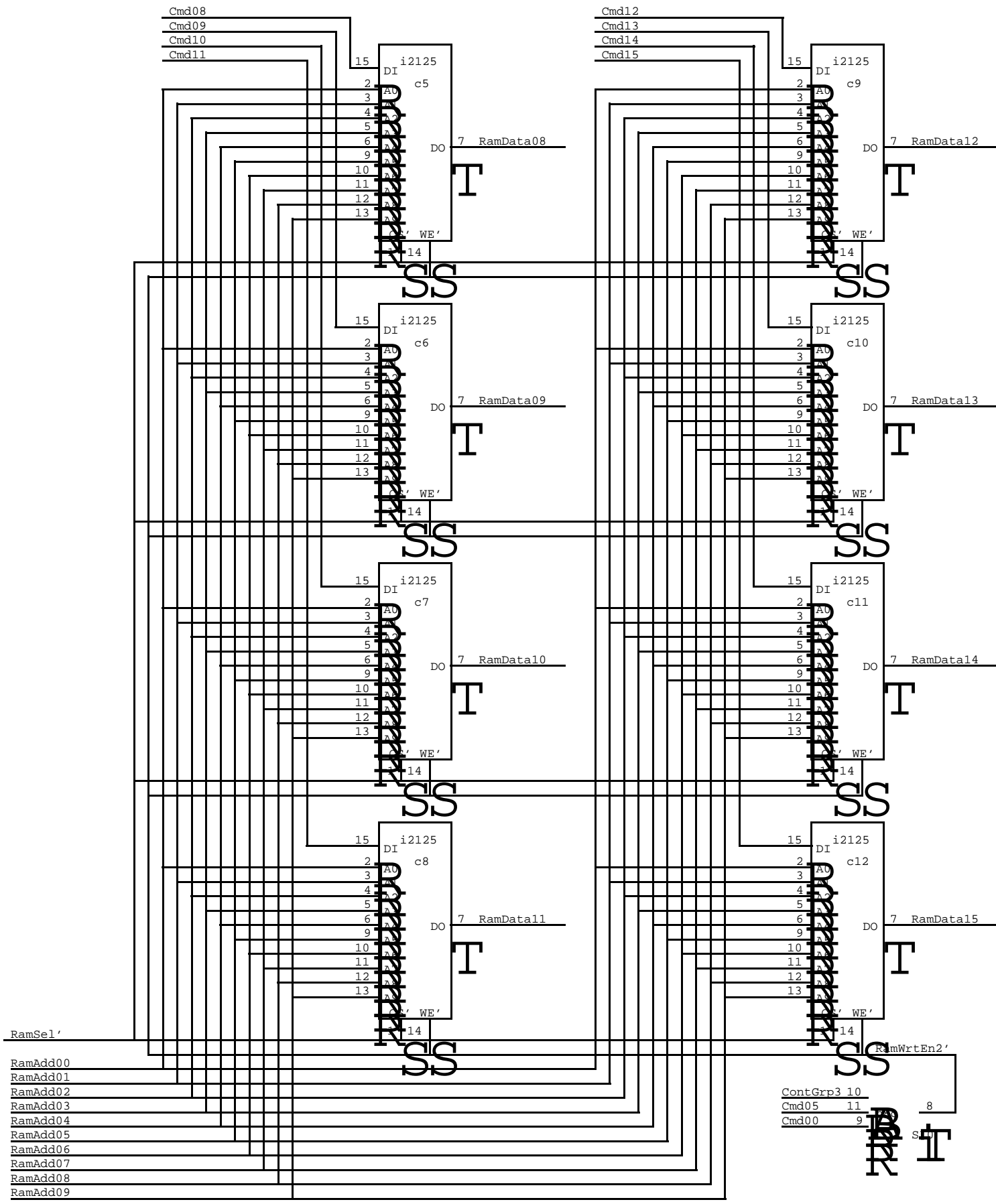
nibble → 0 1 2 3
 (4 bits)

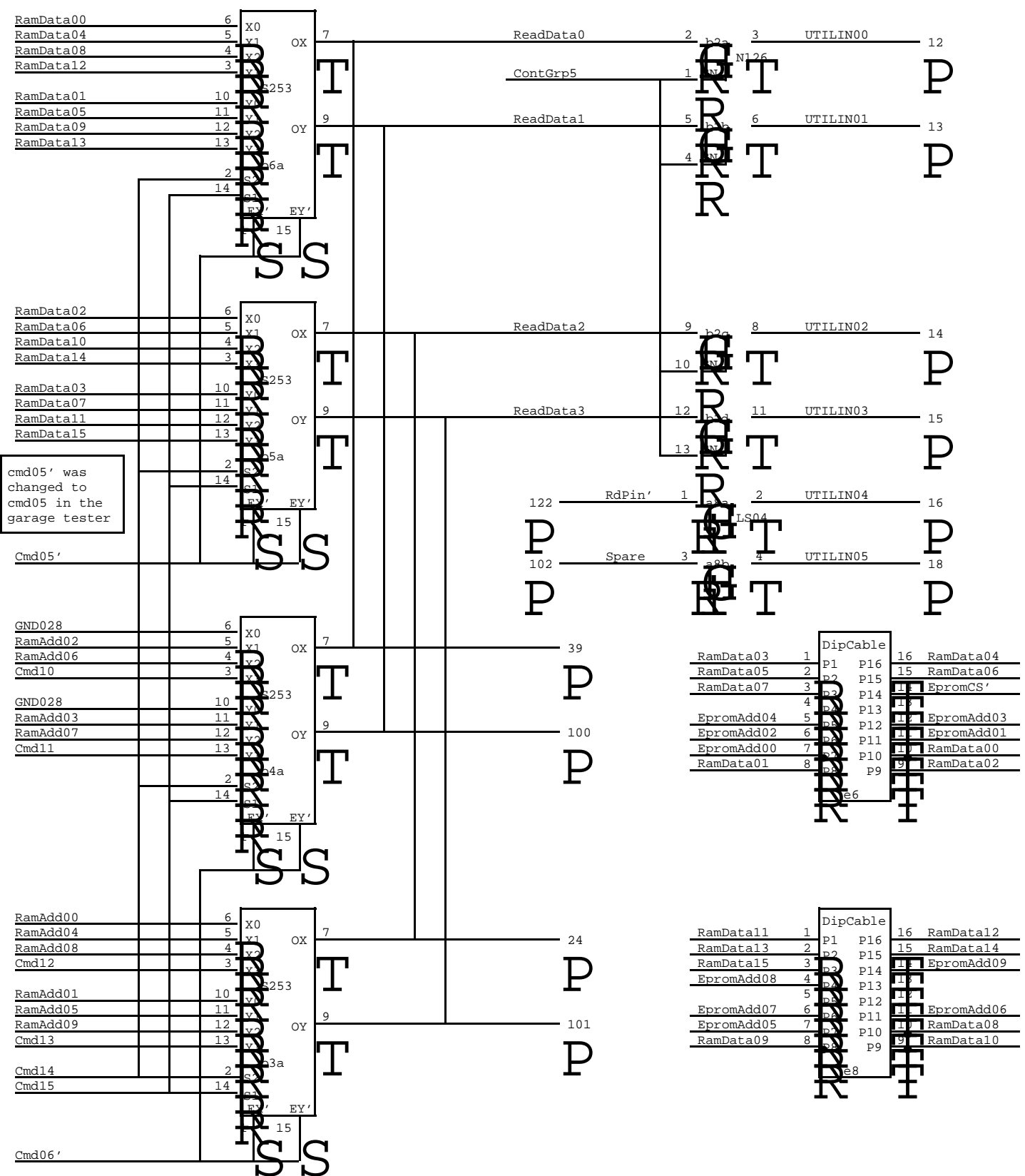


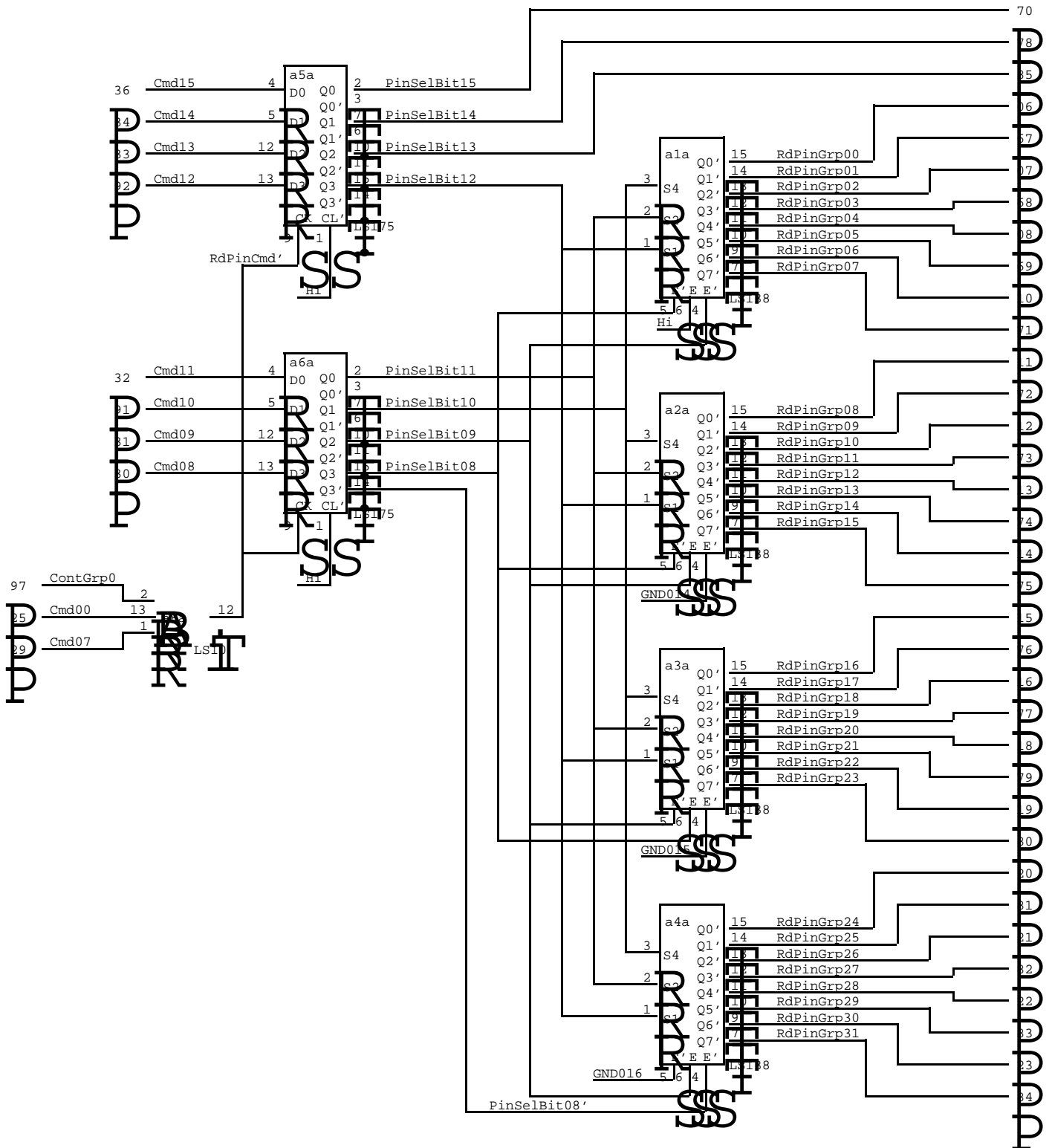
DipCable used as pseudo name for SPLAT to get by Gobble.

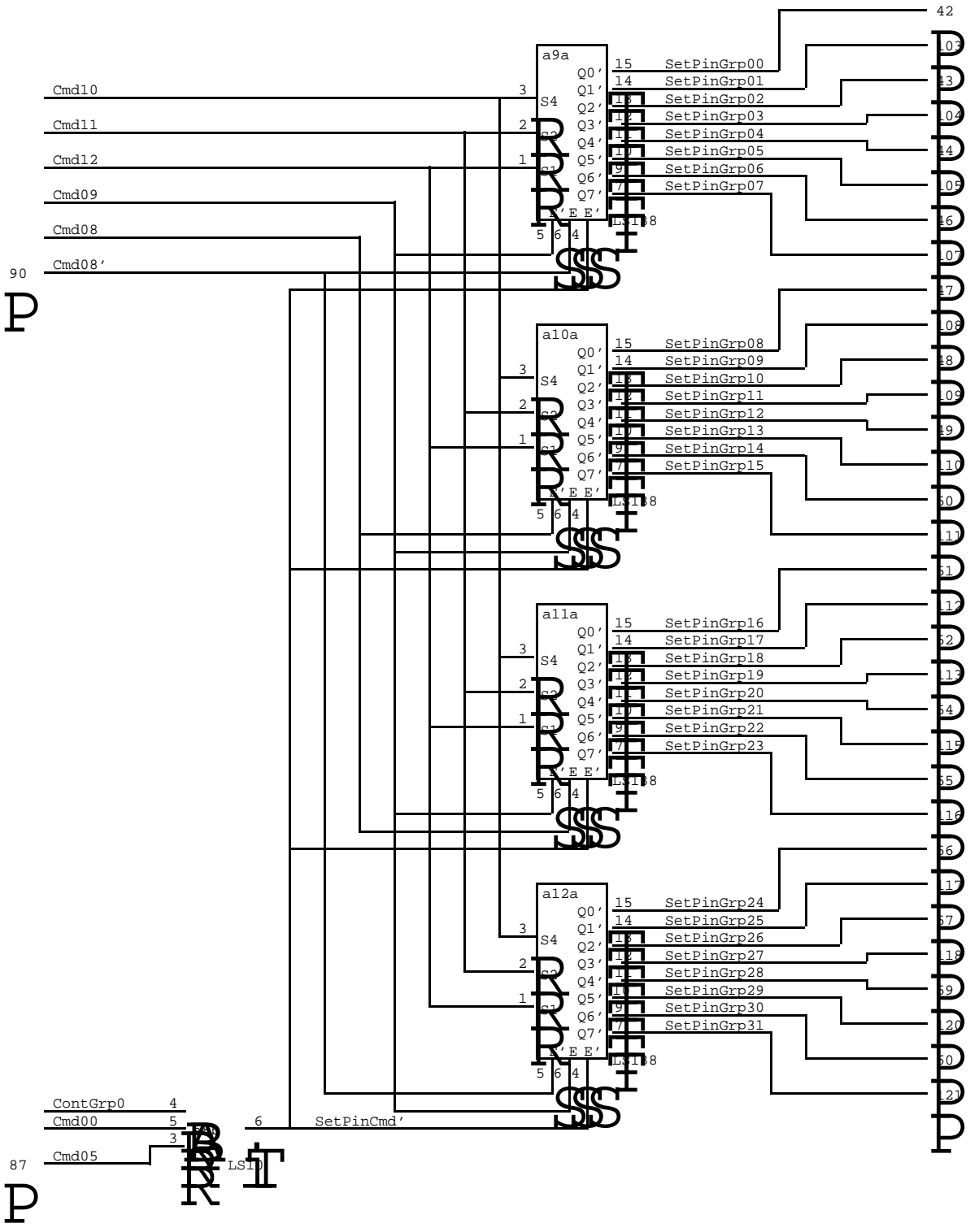


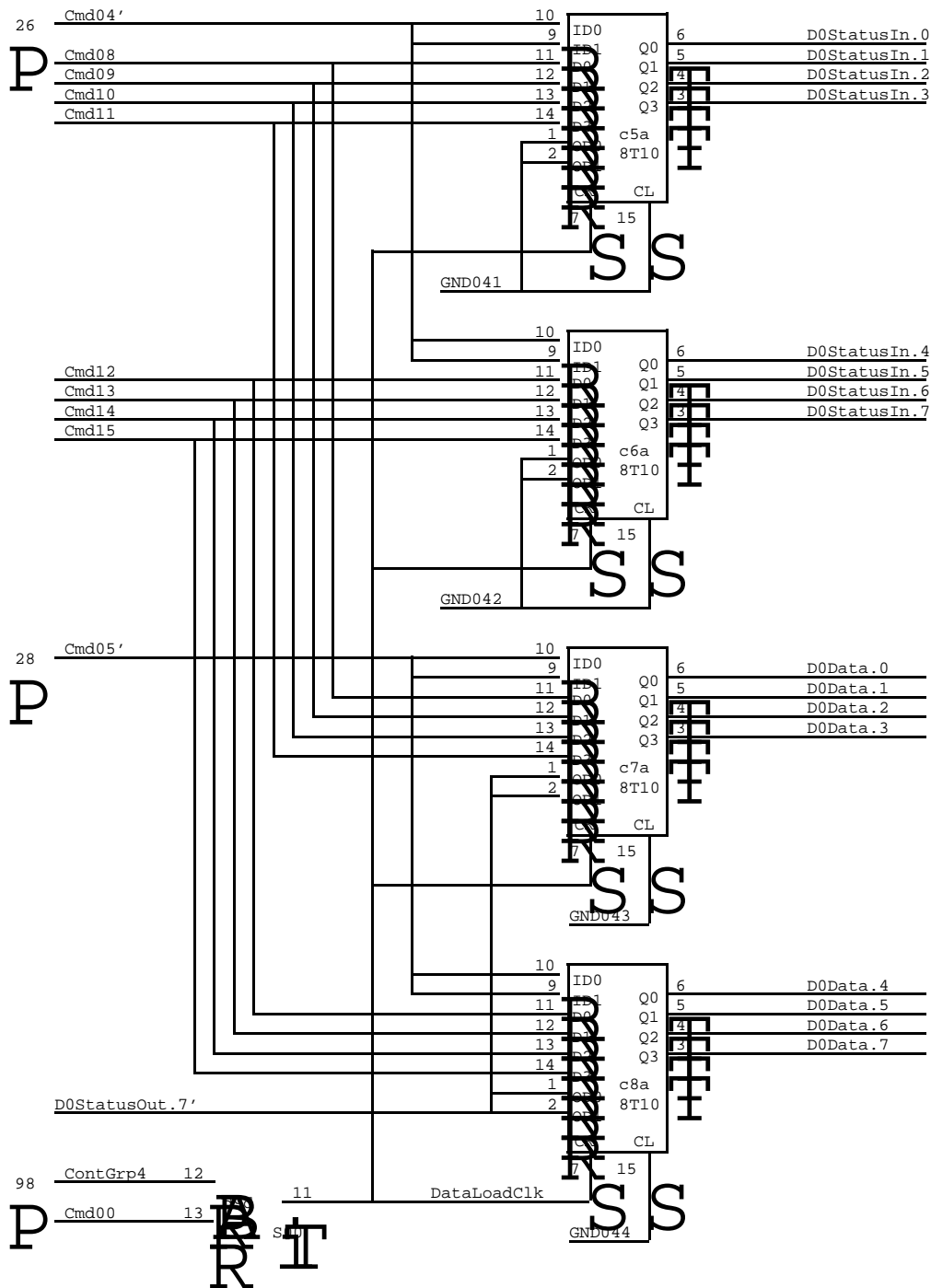


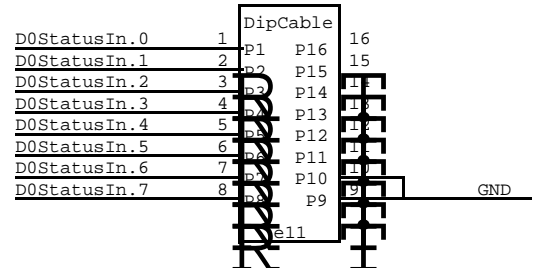
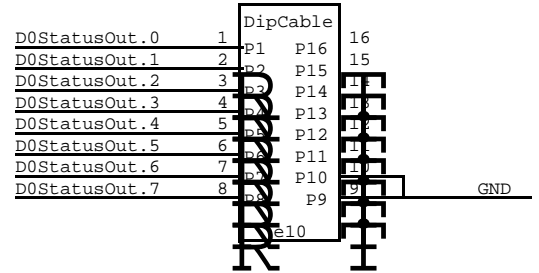
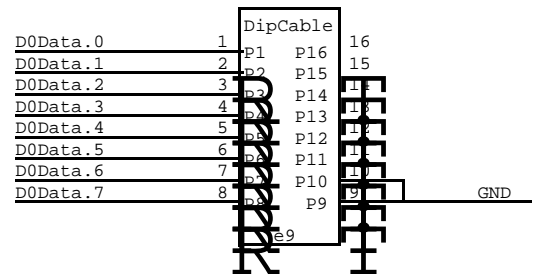
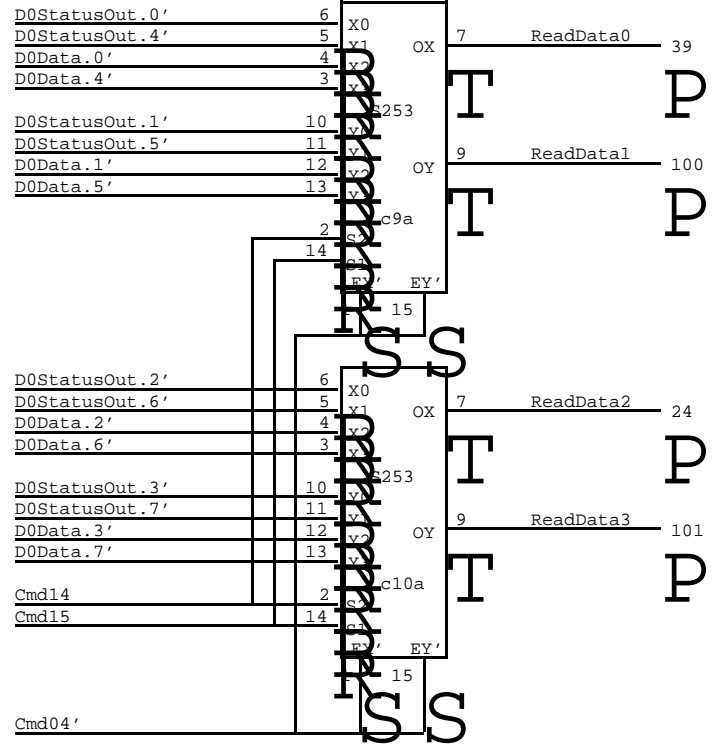
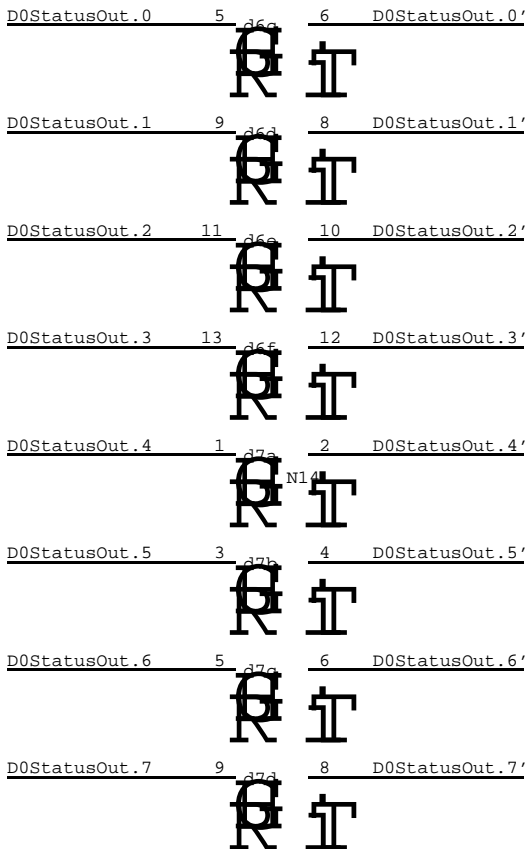
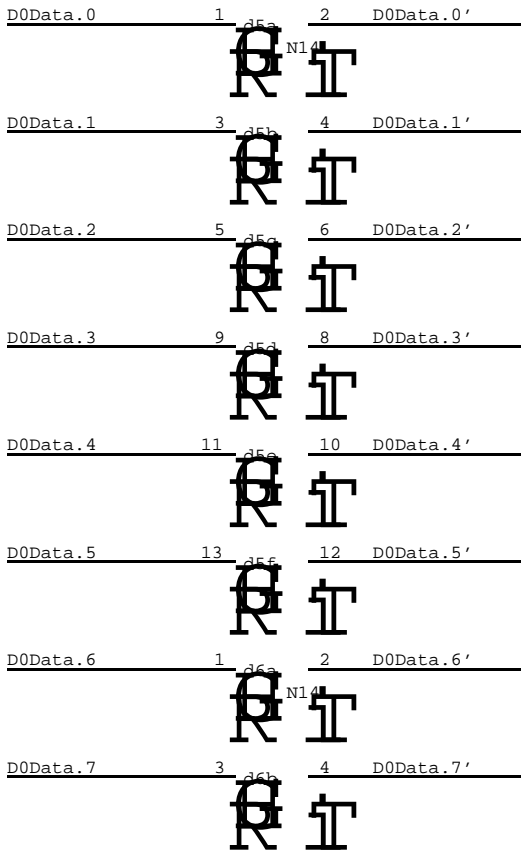


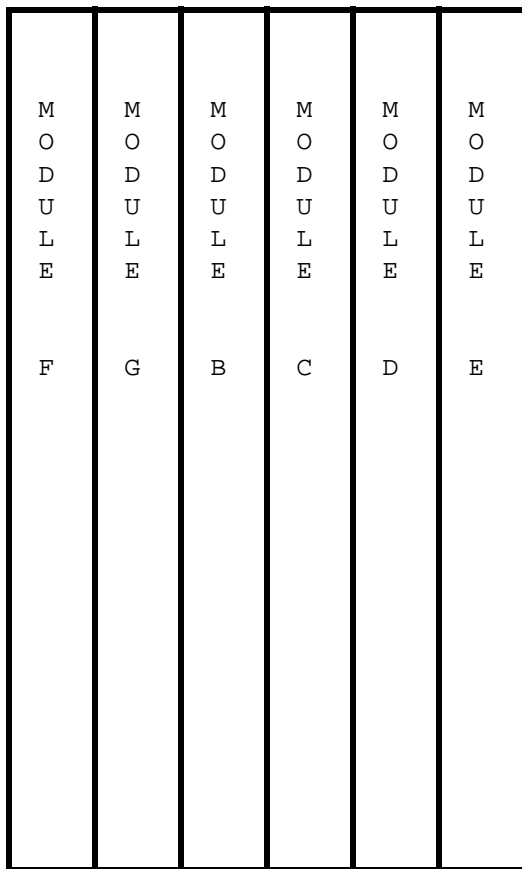




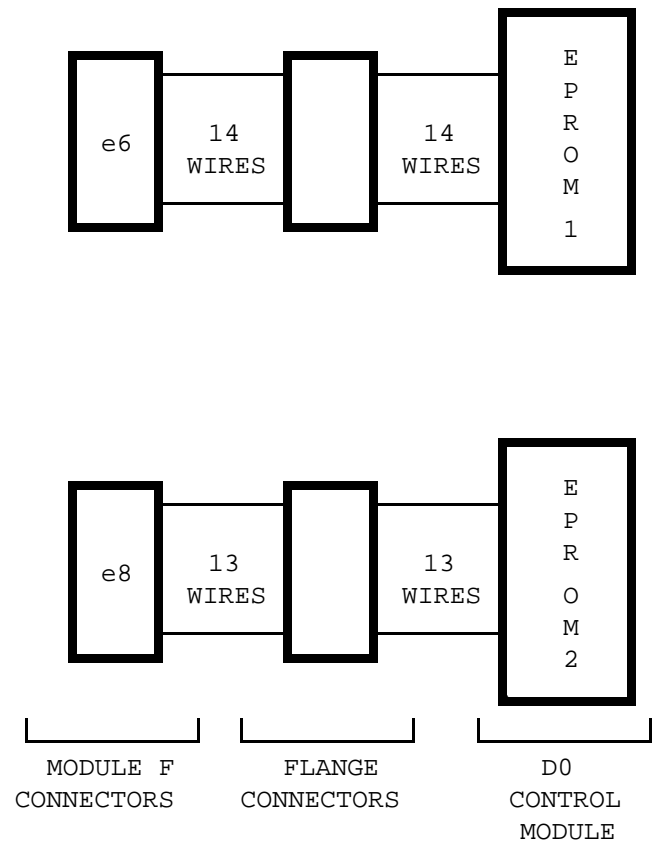








Tester Module Arrangement in Card Cage



Eprom Simulator Cabling

2
1
0
1
2

6
5
4
3
2
1

A

LS 259	@	#	\$	%	~	&	*	(!)	!	!	@
-----------	---	---	----	---	---	---	---	---	---	---	---	---	---

B

LS 259	@	#	\$	%	~	&	LS 04	(!)	!	!	@
-----------	---	---	----	---	---	---	----------	---	---	---	---	---	---

C

LS 251	@	#	\$	%	~	&	*	(!)	!	!	@
-----------	---	---	----	---	---	---	---	---	---	---	---	---	---

D

N26	@	#	\$	%	~	&	*	(!)	!	!	@
-----	---	---	----	---	---	---	---	---	---	---	---	---	---

E

N26	@	#	DIP CABLE	DIP CABLE	DIP CABLE	DIP CABLE	DIP CABLE	DIP CABLE	!)	!	!	@
-----	---	---	--------------	--------------	--------------	--------------	--------------	--------------	---	---	---	---	---

D0 TESTER CARD B,C,D,E
COMPONENT SIDE

2
1
0
1
2

6
5
4
3
2
1
0

A

!	@	#	\$	%	~	&	*	(!)	!	!	@
•	NI4	NI4	NI4	NI4	SN74 •S 138	SN74 •LS04	SN74 •LS04	898-3 -270	898-3 -270	•	•	•	A

B

!	@	#	\$	%	~	&	*	(!)	!	!	@
•	NI26	SN74 •253	SN74 •253	SN74 •253	SN74 •253	SN74 •S00	SN74 •S10	•	•	•	•	•	B

C

!	@	#	\$	%	~	&	*	(!)	!	!	@
•	•	NI26	NI26	I •225	I •225	I •225	I •225	I •2125	I •2125	I •225	I •225	I •225	C

D

!	@	#	\$	%	~	&	*	(!)	!	!	@
•	NI26	NI26	NI26	I •2125	I •2125	I •2125	I •2125	I •225	I •2125	I •2125	I •2125	I •2125	D

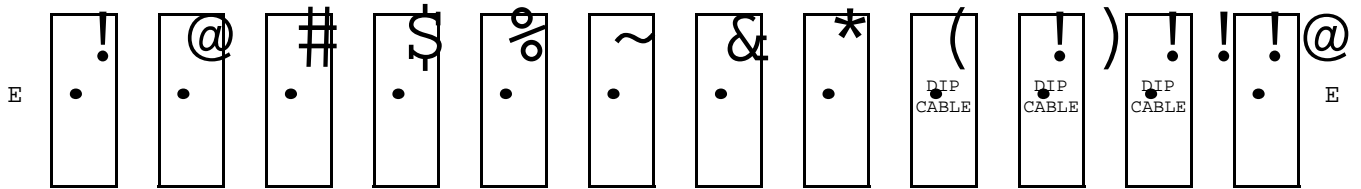
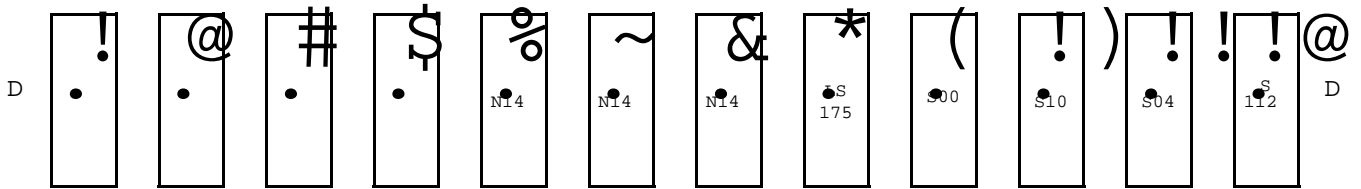
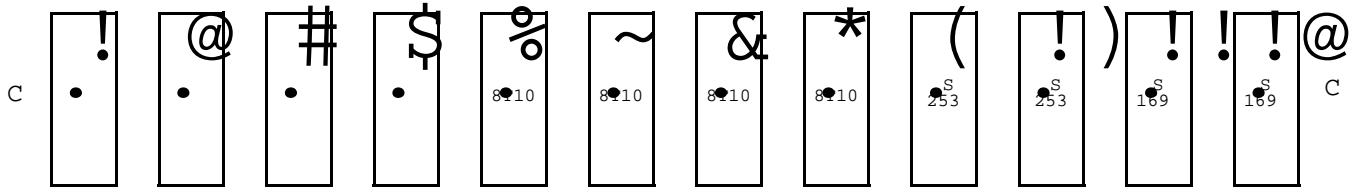
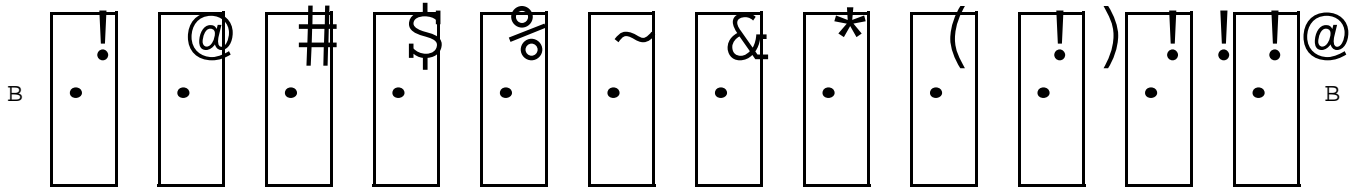
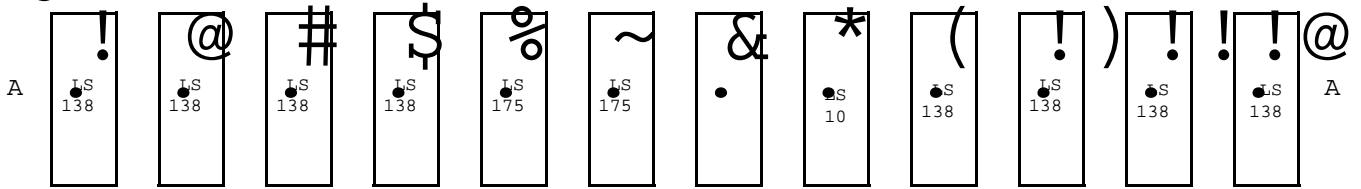
E

!	@	#	\$	%	~	&	*	(!)	!	!	@
•	SN74 •S 163	SN74 •S 163	SN74 •S 163	•	Dip Cable	•	Dip Cable	•	•	•	•	•	E

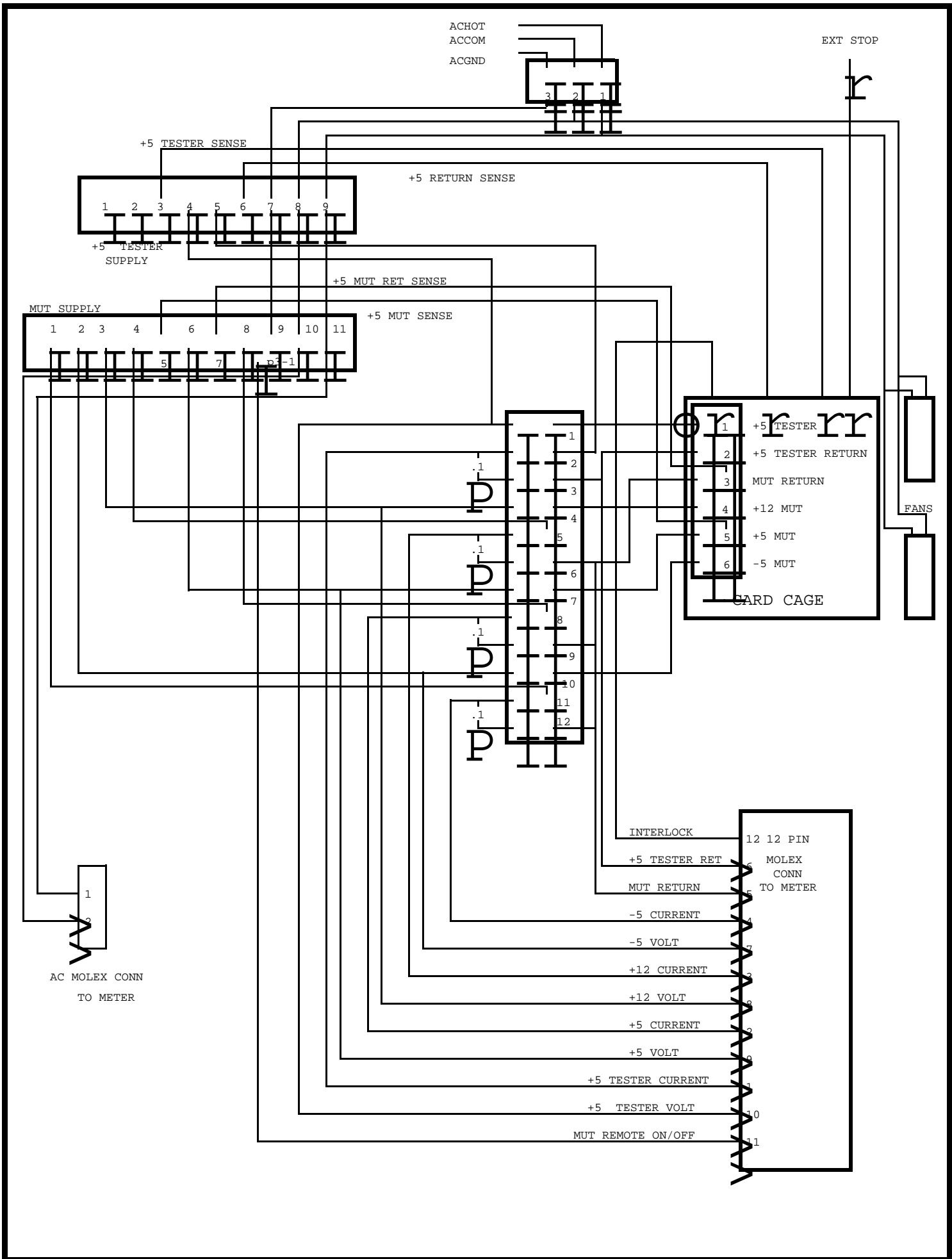
D0 TESTER CARD F
COMPONENT SIDE

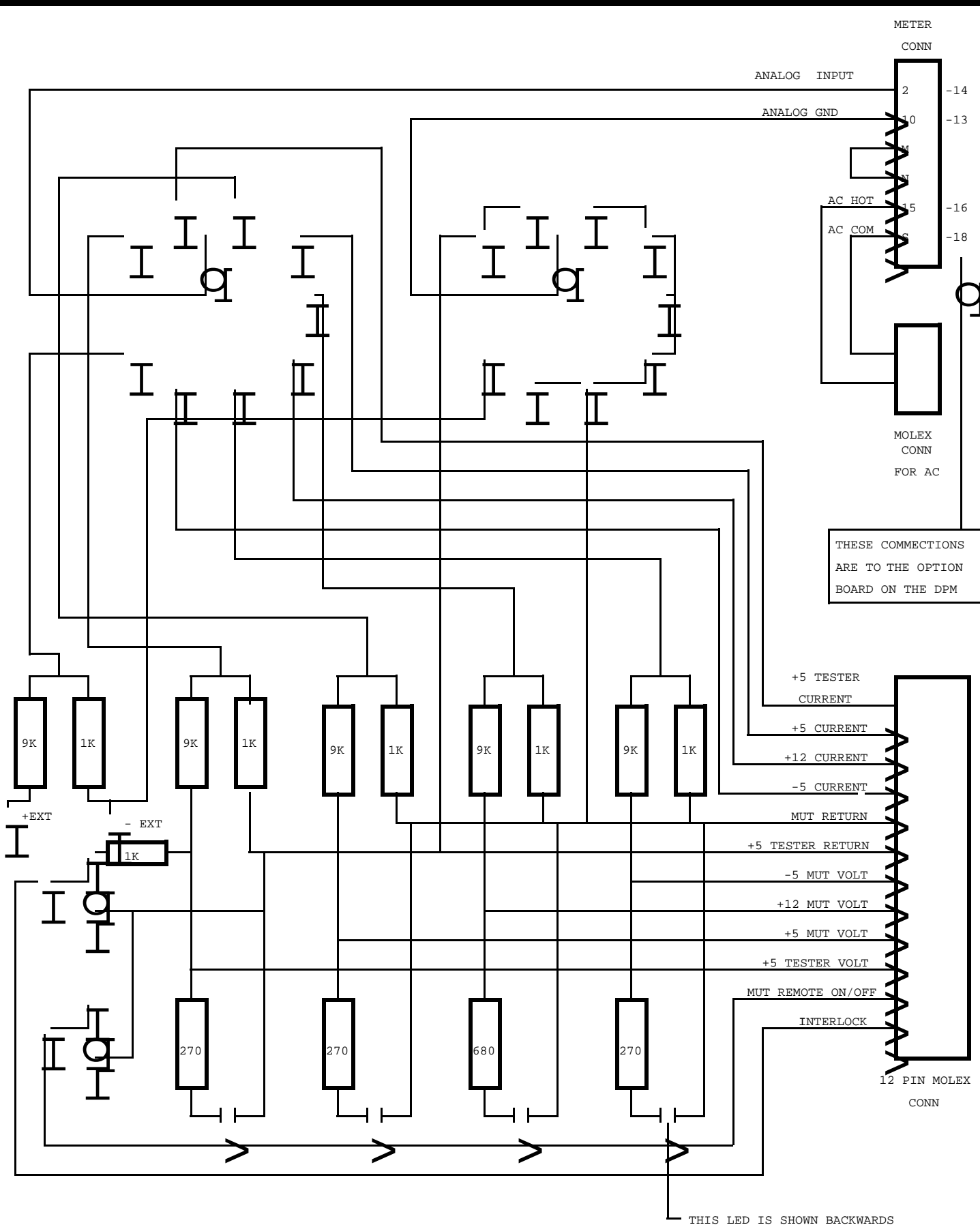
2
1
0
1
2

6
5
4
3
2
1



D0 TESTER G BOARD
COMPONENT SIDE





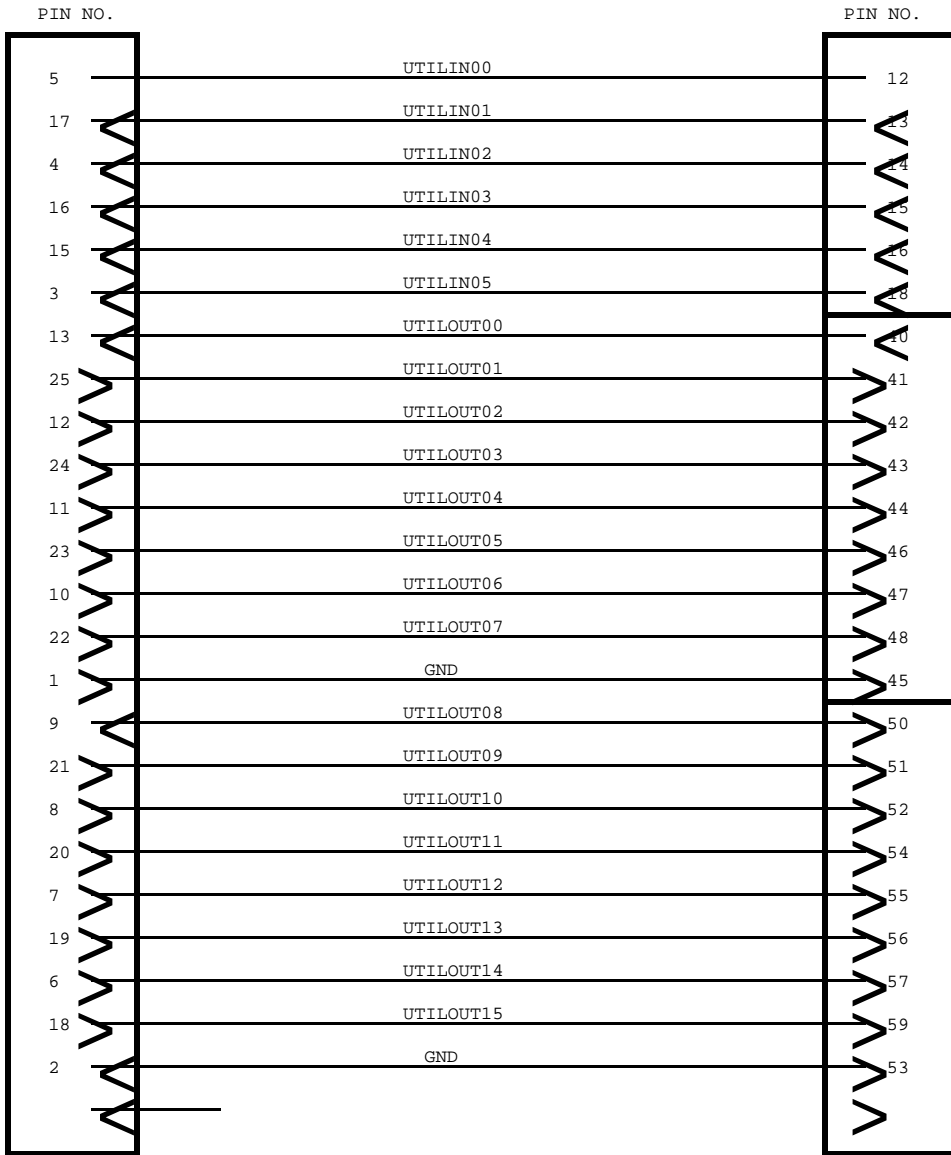
THESE CONNECTIONS ARE TO THE OPTION BOARD ON THE DPM

THIS LED IS SHOWN BACKWARDS

METER CIRCUITRY

DB 25-P

F BRD EDGE CONN



THE ABOVE IS A DIAGRAM OF THE INTERNAL CABLING OF THE UTILIN AND UTILOUT BITS FROM THE F BRD EDGE CONN VIA BERG CONNS TO THE DB25-P FOR THE ALTO THAT IS LOCATED ON THE D0TESTER INTERFACE PLATE.