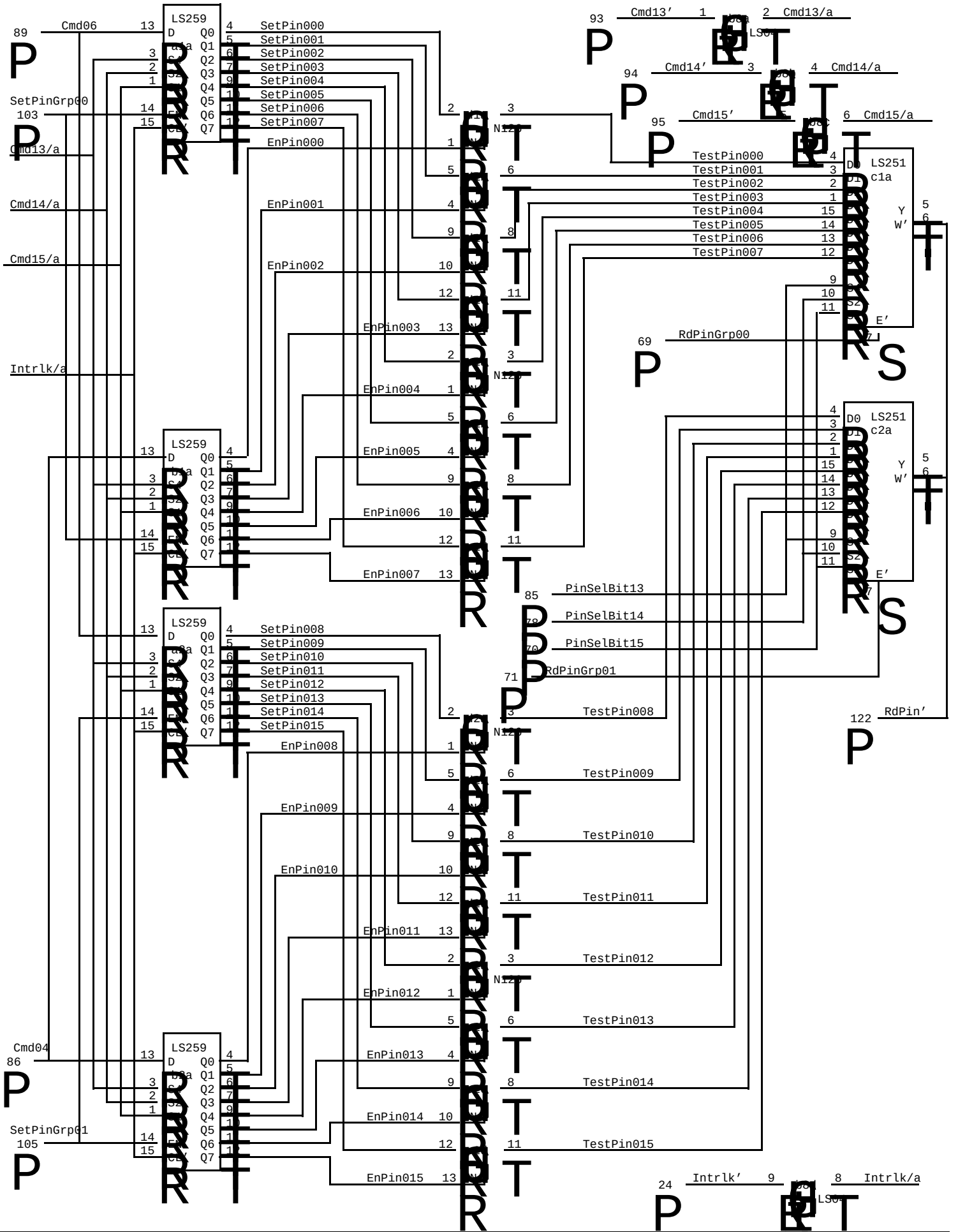
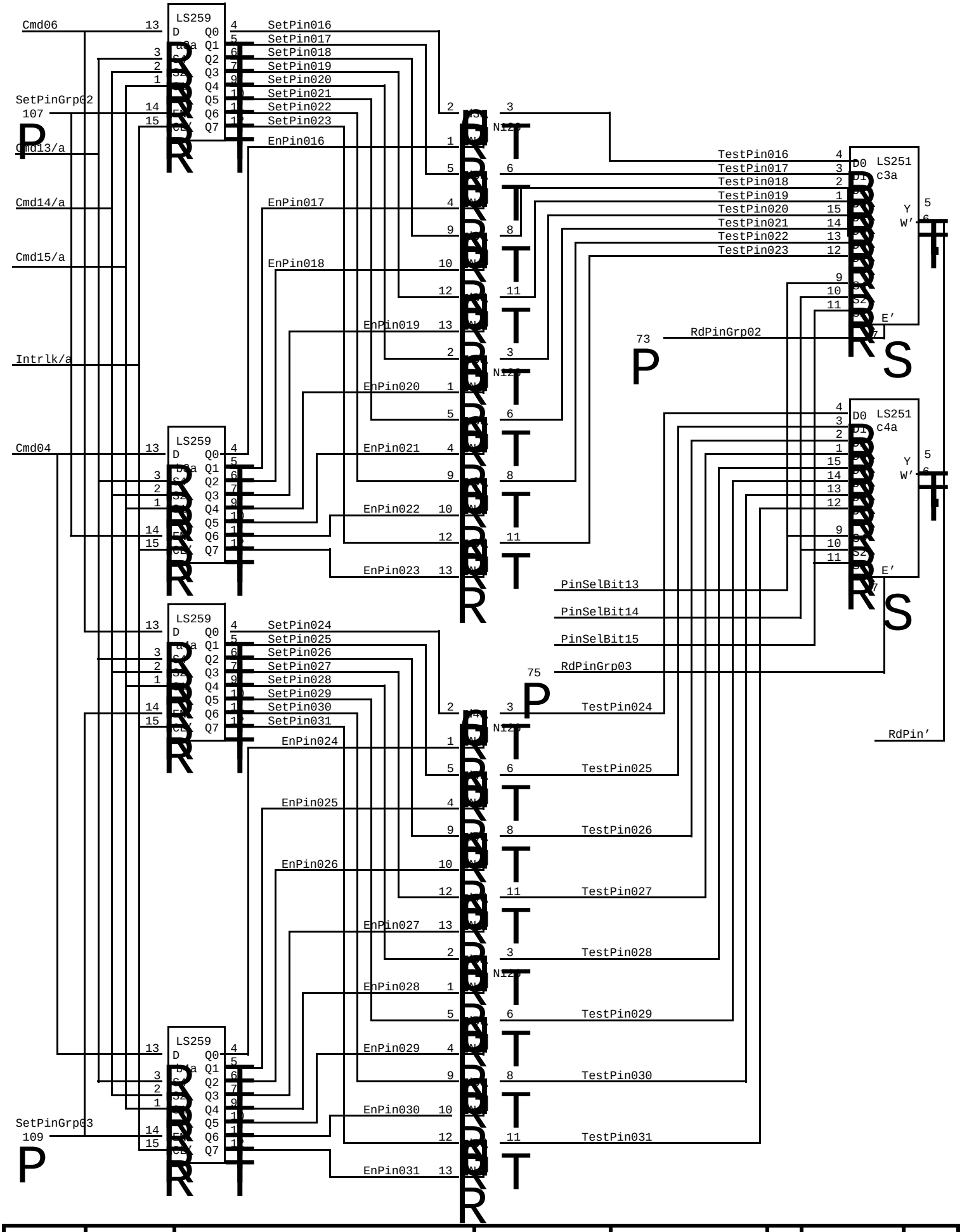
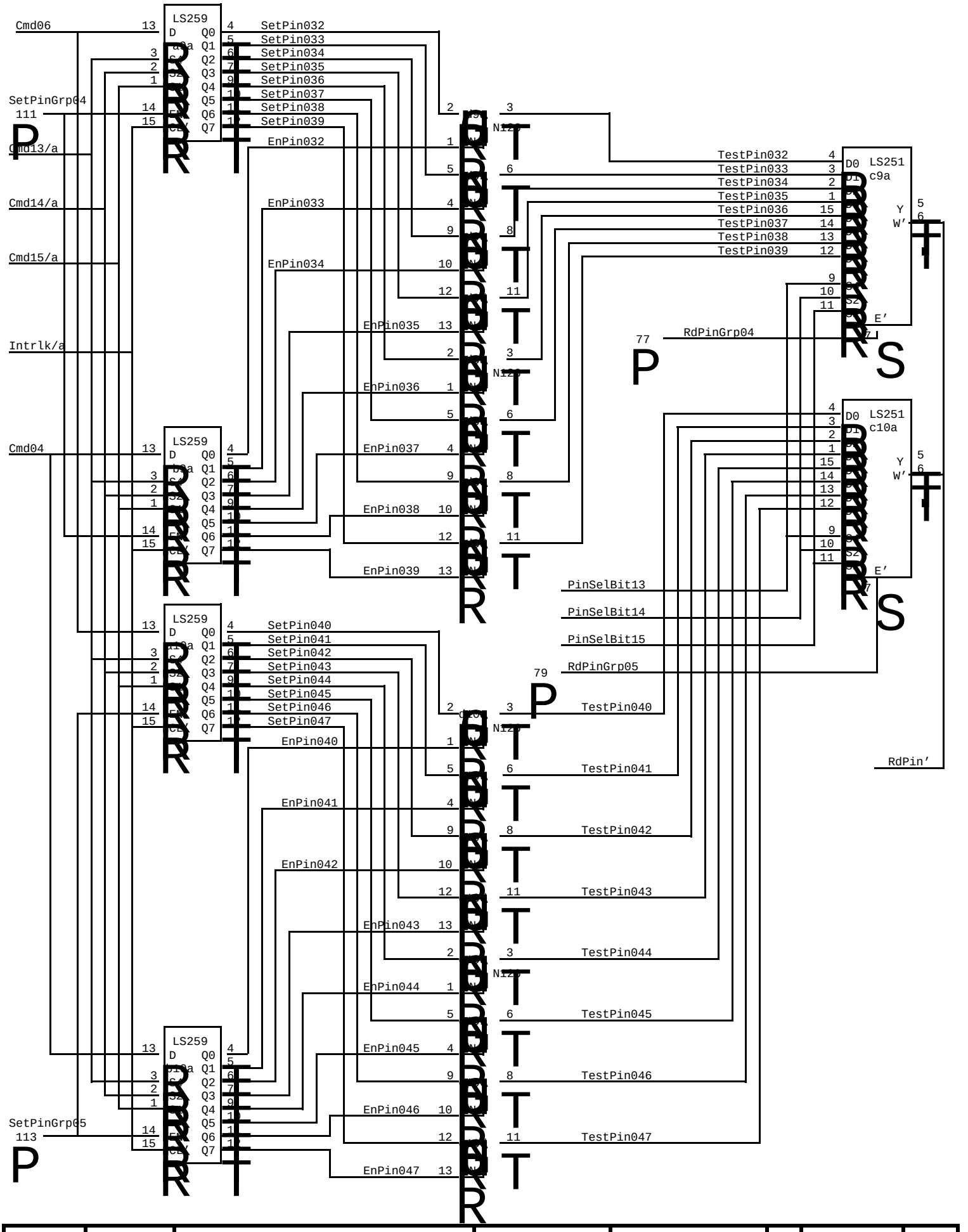
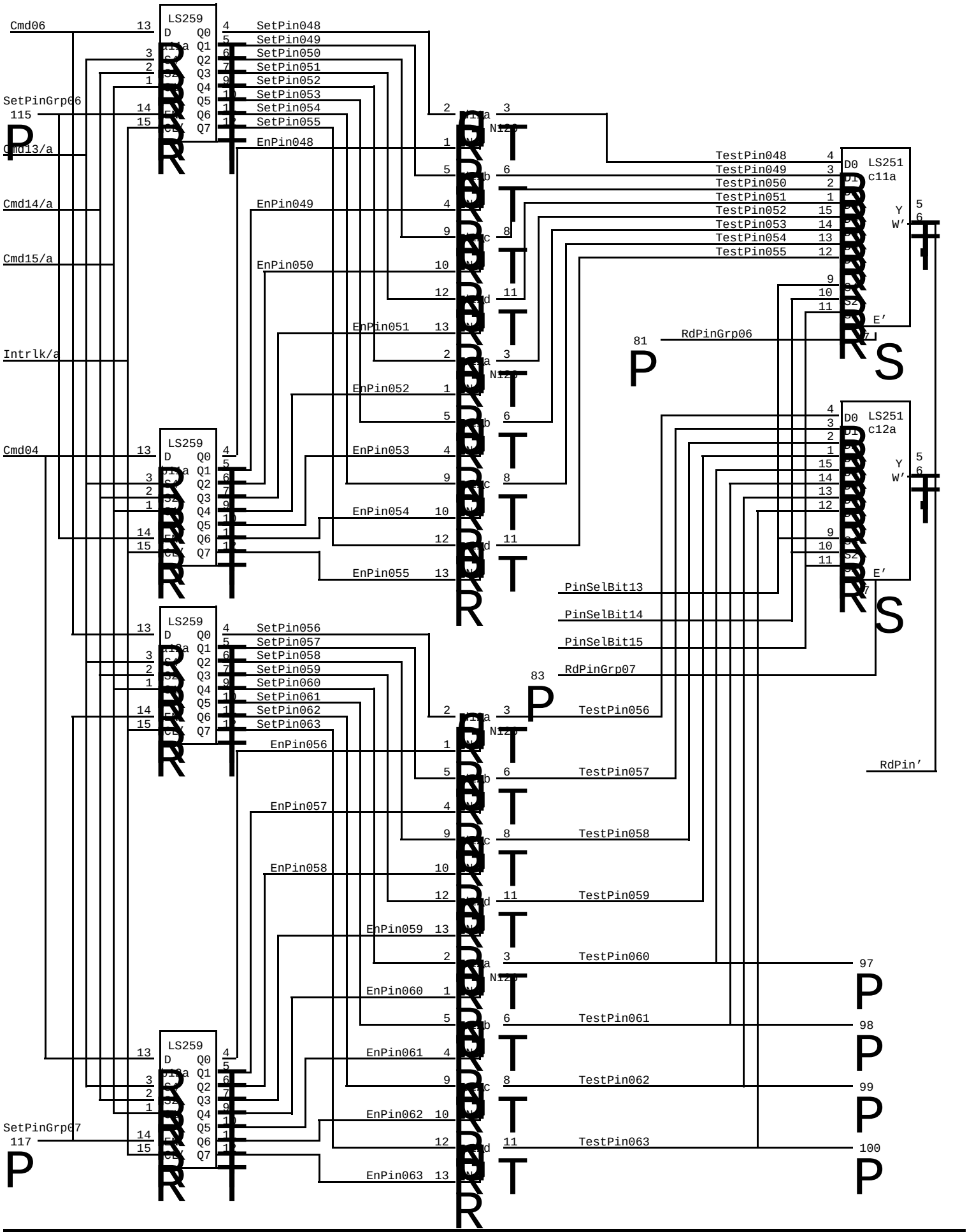

LS259
LS251
Cmd06
Cmd13/a
Cmd14/a
Cmd15/a
Intrlk/a
Cmd04
SetPinGrp00
SetPinGrp01
SetPin000
SetPin001
SetPin002
SetPin003
SetPin004
SetPin005
SetPin006
SetPin007
SetPin008
SetPin009
SetPin010
SetPin011
SetPin012
SetPin013
SetPin014
SetPin015
EnPin000
EnPin001
EnPin002
EnPin003
EnPin004
EnPin005
EnPin006
EnPin007
EnPin008
EnPin009
EnPin010
EnPin011
EnPin012
EnPin013
EnPin014
EnPin015
TestPin000
TestPin001
TestPin002
TestPin003
TestPin004
TestPin005
TestPin006
TestPin007
TestPin008
TestPin009
TestPin010
TestPin011
TestPin012
TestPin013
TestPin014
TestPin015
RdPinGrp00
RdPinGrp01
RdPin'
PinSelBit13
PinSelBit14
PinSelBit15
Cmd13'
Cmd13/a
Cmd14'
Cmd14/a
Cmd15'
Cmd15/a
Intrlk'
Intrlk/a
LS04
XEROX
EOD
Project
D0
D0Tester Pin Selection Logic 000 thru 015
File
D0TesterB01.sil
Designer
J.F.Cameron
Rev
D
Date
9/21/77
Page
01



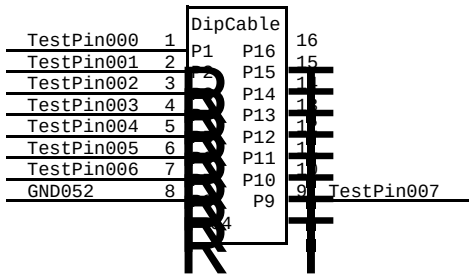
XEROX EOD	Project D0	D0Tester Pin Selection Logic 016 thru 031	File D0TesterB02.sil	Designer C. TSENG	Rev D	Date 9/21/77	Page 02

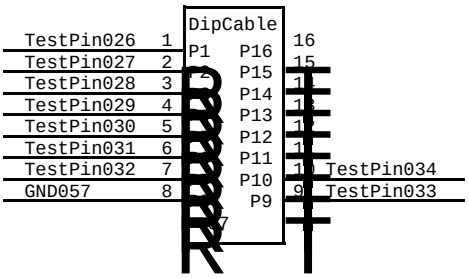


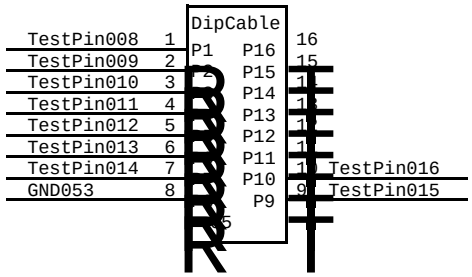
XEROX EOD	Project D0	D0Tester Pin Selection Logic 032 thru 047	File D0TesterB03.sil	Designer C. TSENG	Rev D	Date 9/21/77	Page 03

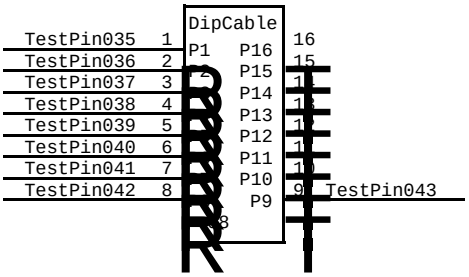


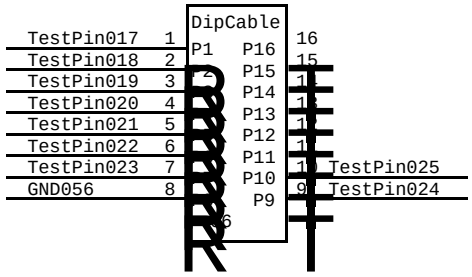
XEROX EOD	Project D0	D0Tester Pin Selection Logic 048 thru 063	File D0TesterB04.sil	Designer C. TSENG	Rev D	Date 9/21/77	Page 04

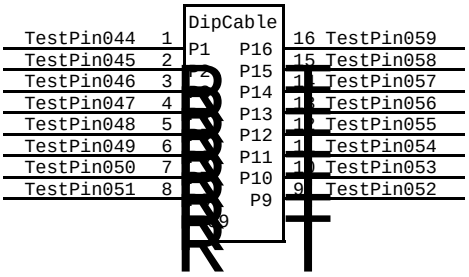












XEROX EOD	Project D0	D0Tester Dip Connector	File D0TesterB05.sil	Designer C. Tseng	Rev D	Date 9/21/77	Page 05

D0 Tester Connector Pin Assignment

DIP CONN	D0 CONNECTOR PIN from MODULE B	C	D	E
e4--1	2	102	52	152
2	3	103	53	153
3	4	104	54	154
4	5	105	55	155
5	6	106	56	156
6	7	107	57	157
7	8	108	58	158
9	9	109	59	159
e5--1	11	111	61	161
2	12	112	62	162
3	13	113	63	163
4	14	114	64	164
5	15	115	65	165
6	16	116	66	166
7	17	117	67	167
9	18	118	68	168
10	19	119	69	169
e6--1	21	121	71	171
2	22	122	72	172
3	23	123	73	173
4	24	124	74	174
5	25	125	75	175
6	26	126	76	176
7	27	127	77	177
9	28	128	78	178
10	29	129	79	179

DIP CONN	D0 CONNECTOR PIN from MODULE B	C	D	E
e7--1	31	131	81	181
2	32	132	82	182
3	33	133	83	183
4	34	134	84	184
5	35	135	85	185
6	36	136	86	186
7	37	137	87	187
9	38	138	88	188
10	39	139	89	189
e8--1	41	141	91	191
2	42	142	92	192
3	43	143	93	193
4	44	144	94	194
5	45	145	95	195
6	46	146	96	196
7	47	147	97	197
8	48	148	98	198
9	49	149	99	199
e9--1				
2				
3				
4	T	T	T	T
5	E	E	E	E
6	S	S	S	S
7	T	T	T	T
9				
10	C	C	C	C
11	L	L	L	L
12	I	I	I	I
13	P	P	P	P
14				
15				
16				

The D0 Tester modules C, D, and E are electrically identical to module B. The only difference is in the logical identity of the signals and the backpanel wiring. The following table lists the changes in signal names for each module. Backpanel pin connections have been prepared, and are filed under the name D0TesterBP1.bravo.

SIGNAL NAME	MODULE			
	B	C	D	E
SetPinGrp	00-07	08-15	16-23	24-31
RdPinGrp	00-07	08-15	16-23	24-31
SetPin	000-063	064-127	128-191	192-255
EnPin	000-063	064-127	128-191	192-255
TestPin	000-063	064-127	128-191	192-255
Cmd	13/a-15/a	13/b-15/b	13/c-15/c	13/d-15/d
Intrlk/	a	b	c	d

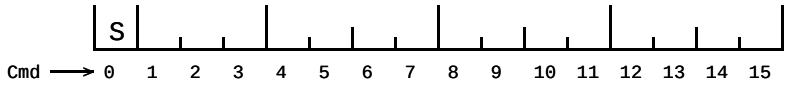
Module Signal Names

D0 Tester Command Summary

8/29/77

CARTER TSENG

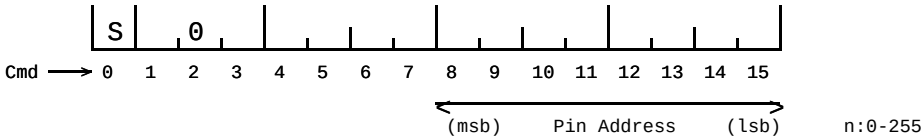
UTILOUT (177016B):



ContGrp

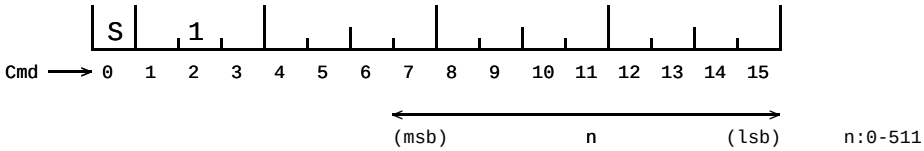
0 : Pin Control **(Read & Set)**
1 : Clock Control
2 : Load RAM Address
3 : Load RAM Data
4 : Load Data Byte A & B (Alto to D0)
5 : Read Data Nibble a,b,c & d (D0 Output or internal)
6 & 7 : (not used)

PIN CONTROL:



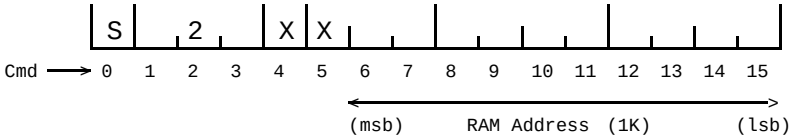
bit 4 : Enable Pin n drive
bit 5 : Set pin n to bit 6
bit 6 : pin n drive state
bit 7 : Read pin n by UTILIN04

CLOCK CONTROL



bit 4 : to boot
bit 5 : to run n clocks(take precedence over bit 6)
bir 6 : to run n instructions
n>255:to run clock continuously

LOAD RAM ADDRESS



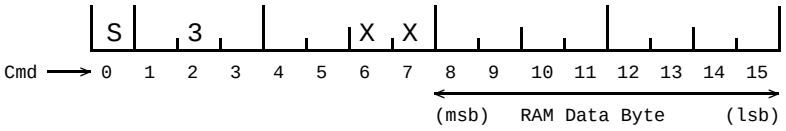
X: not used

D0 Tester Command Summary (Conti.)

8/29/77

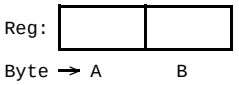
CARTER TSENG

LOAD RAM DATA

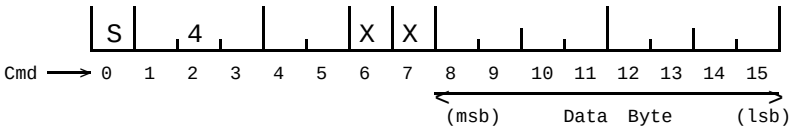


bit 4 : load data to most significant byte of output reg.
bit 5 : load data to least significant byte of output reg.

4	5	Function
0	0	X
0	1	B
1	0	A
1	1	AB

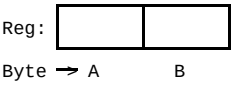


LOAD DATA BYTE

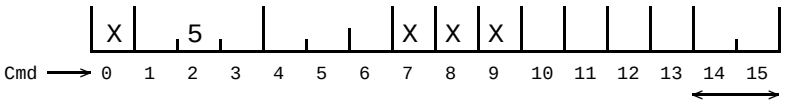


bit 4 : load data to most significant byte of output reg.
bit 5 : load data to least significant byte of output reg.

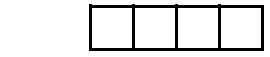
4	5	Function
0	0	X
0	1	B
1	0	A
1	1	AB

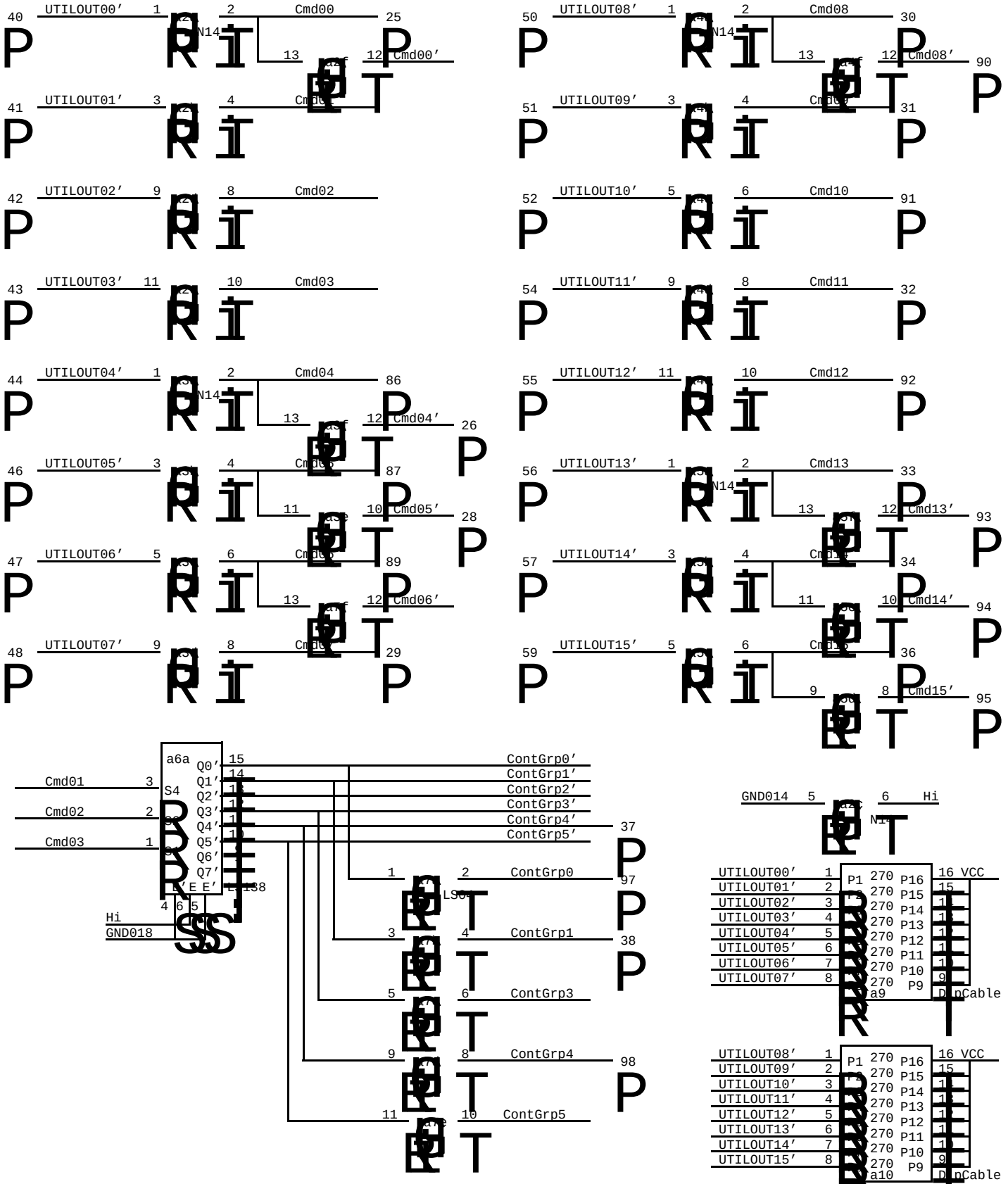


READ DATA NIBBLE



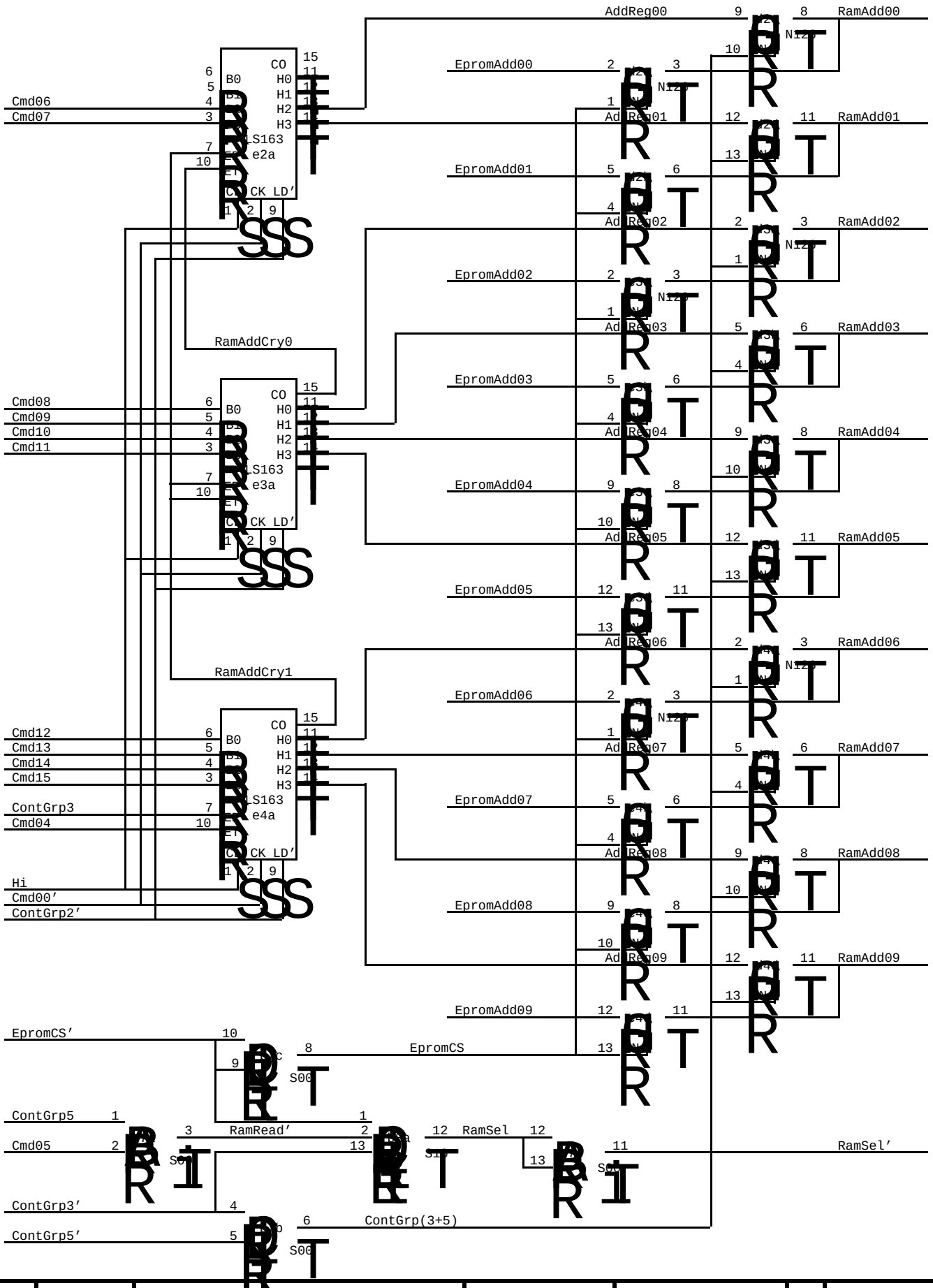
bit 4 : from D0 (4 nibbles)
bit 5 : from RAM Data (4 nibbles)
bit 6 : from RAM Address (3 nibbles)
bit 10 : Turn around test on UTILIN[00]
bit 11 : Turn around test on UTILIN[01]
bit 12 : Turn around test on UTILIN[02]
bit 13 : Turn around test on UTILIN[03]



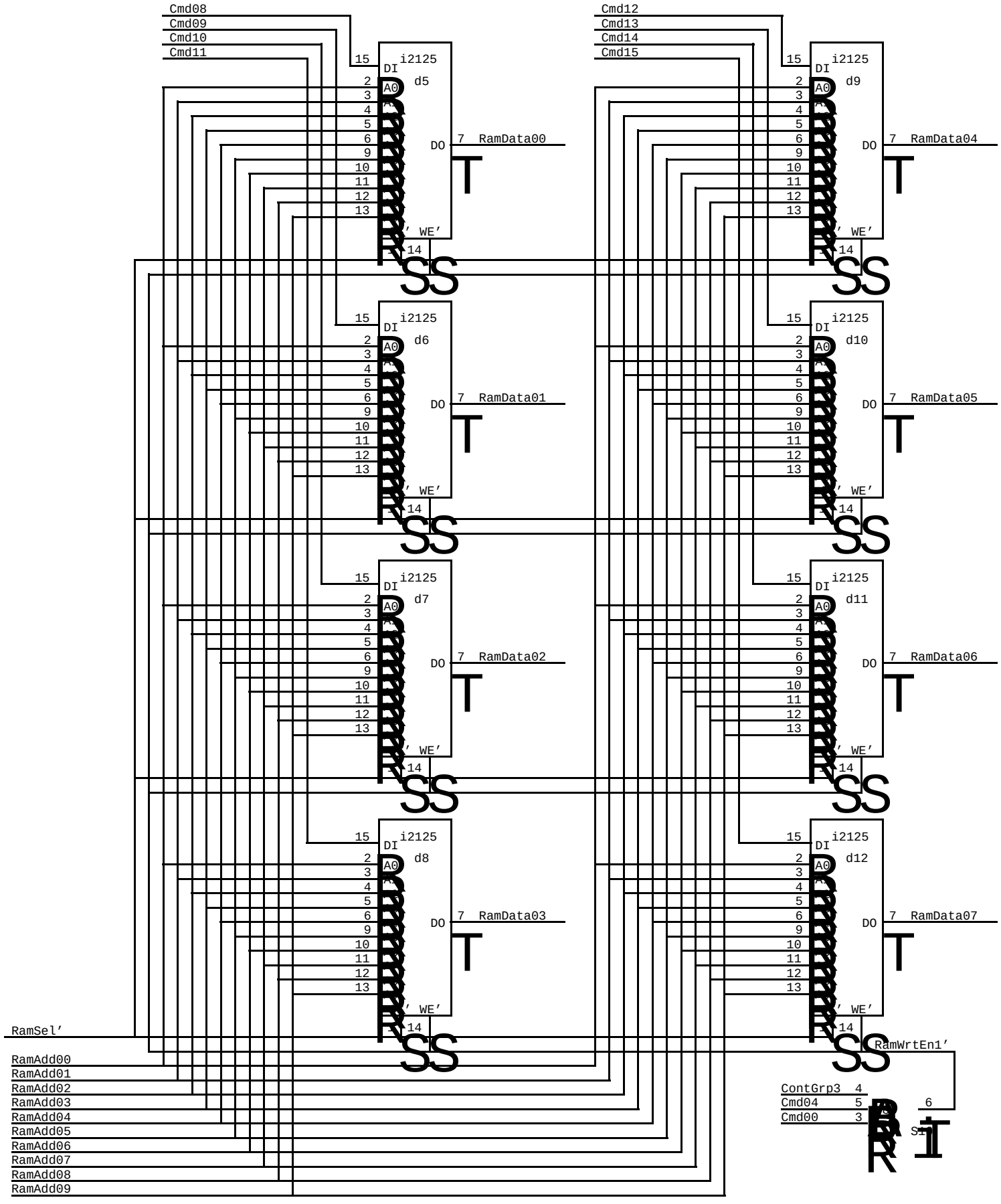


DipCable used as pseudo name for SPLAT to get by Gobble.

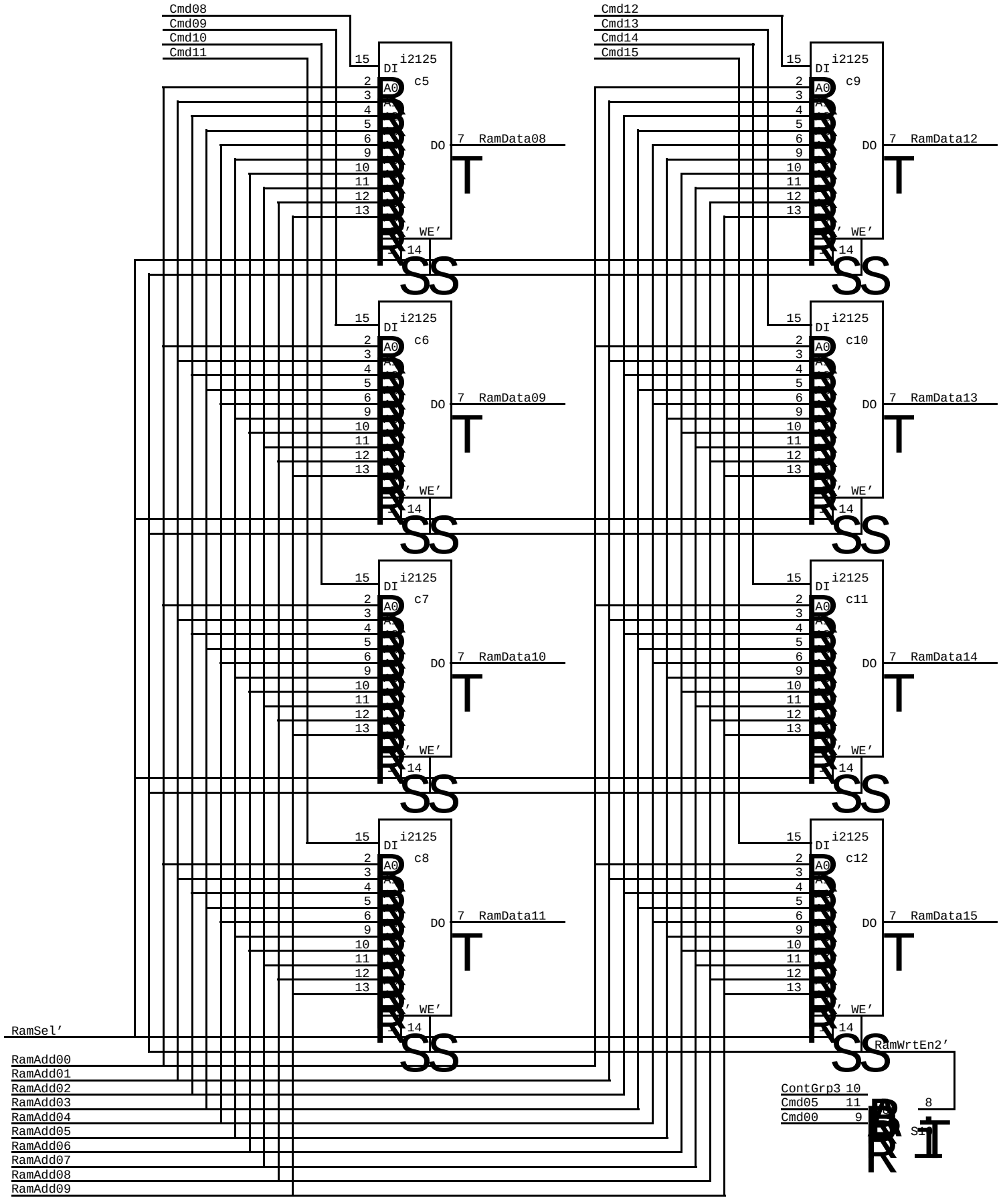
XEROX EOD	Project D0	D0Tester Alto Input	File D0TesterF01.sil	Designer J.F.Cameron	Rev D	Date 11/10/77	Page 01



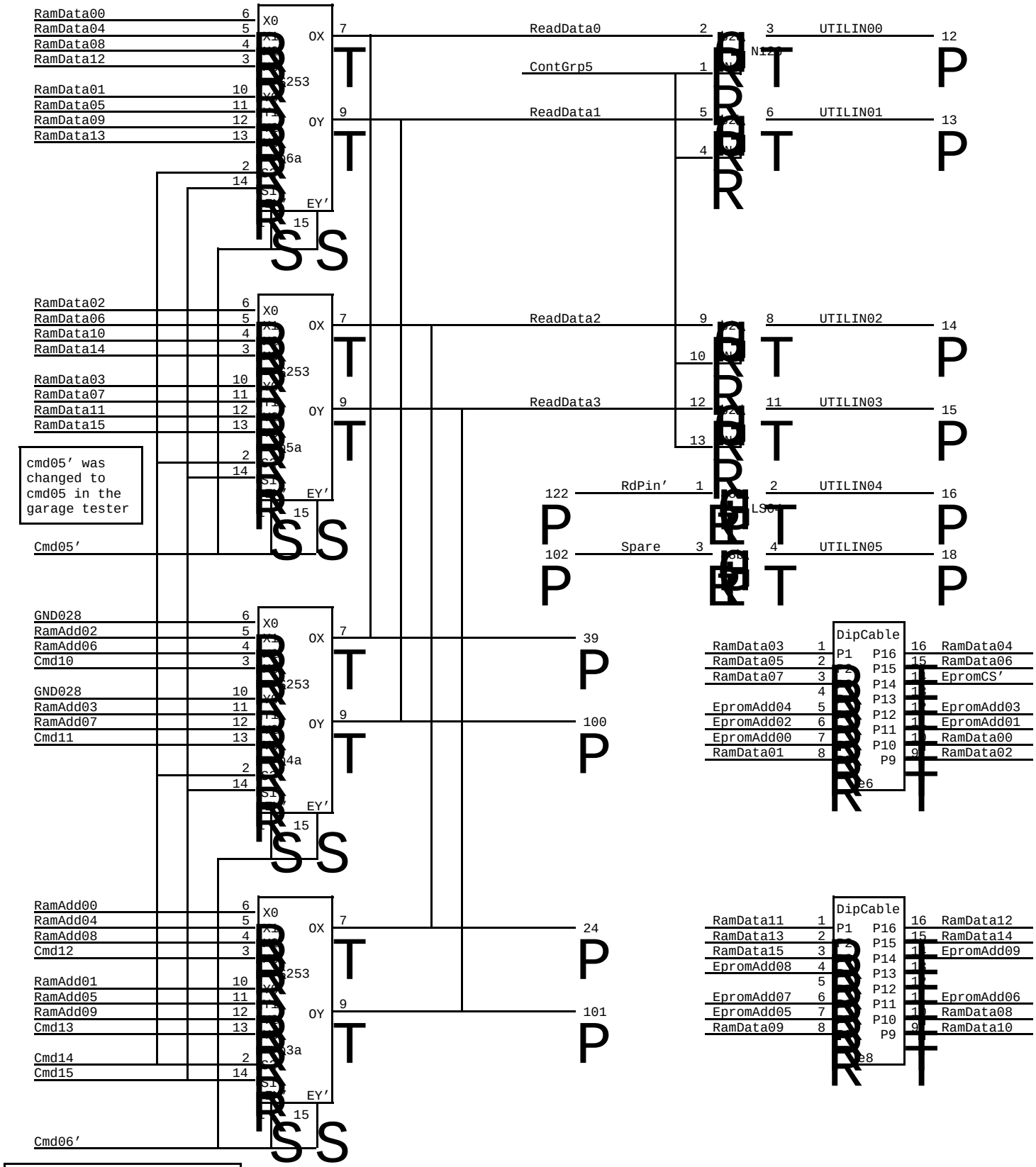
XEROX EOD	Project D0	D0Tester Ram Address and Selection	File D0TesterF02.sil	Designer J. F. Cameron	Rev D	Date 9/21/77	Page 02



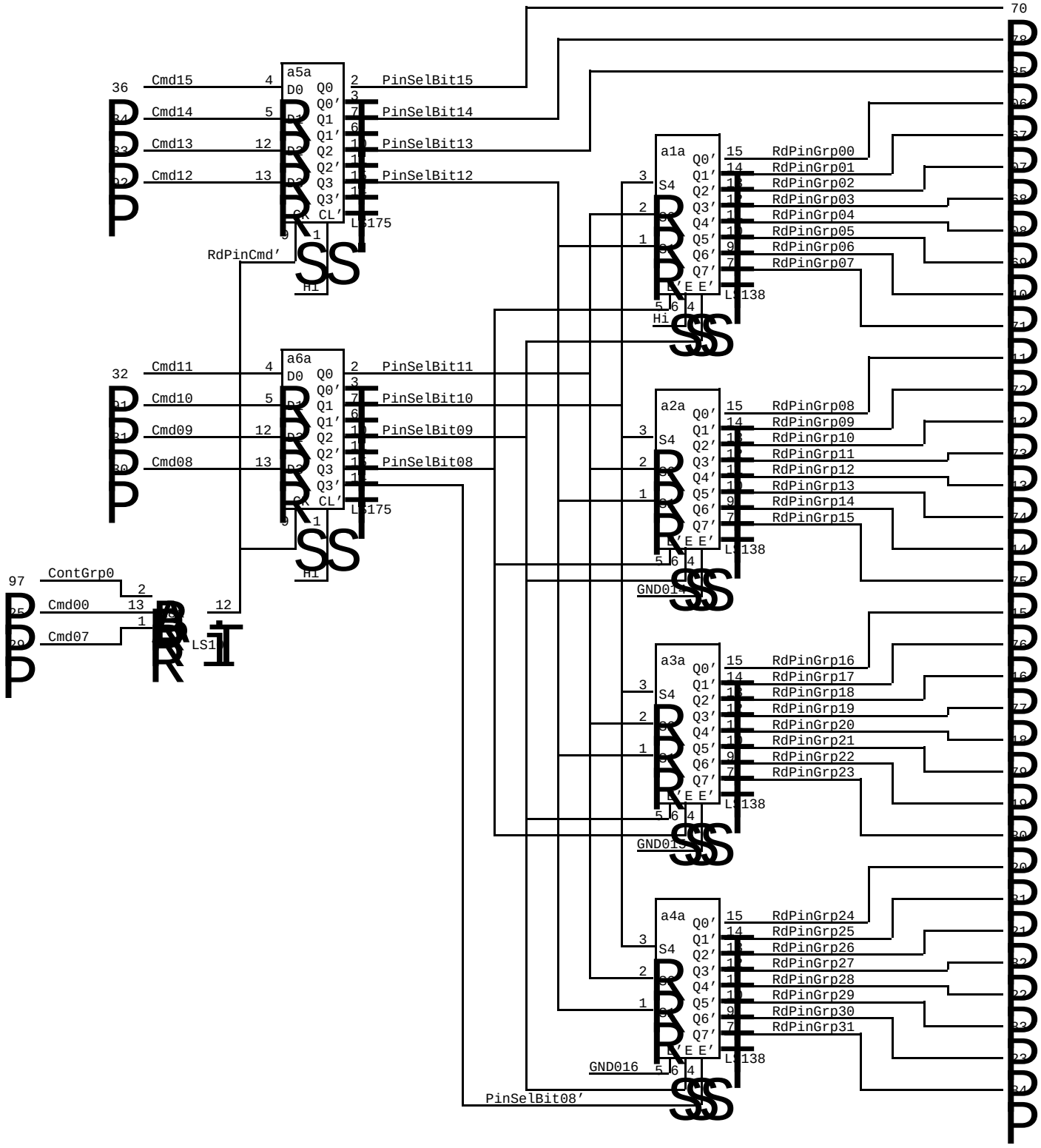
XEROX EOD	Project D0	D0Tester RAM Store Bank One	File D0TesterF03.sil	Designer J.F.Cameron	Rev D	Date 9/6/77	Page 03



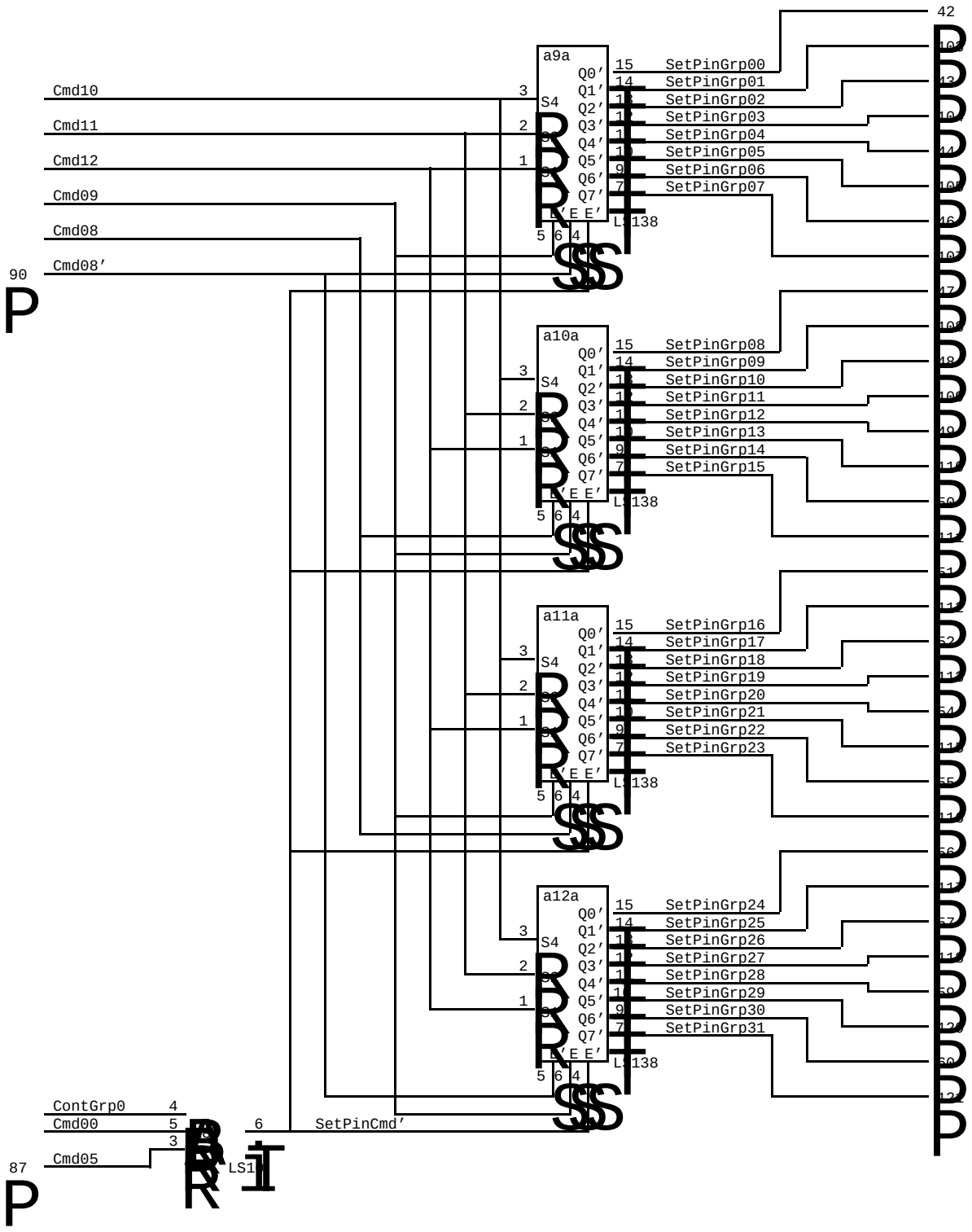
XEROX EOD	Project D0	D0Tester RAM Store Bank One	File D0TesterF04.sil	Designer J.F.Cameron	Rev D	Date 9/6/77	Page 04



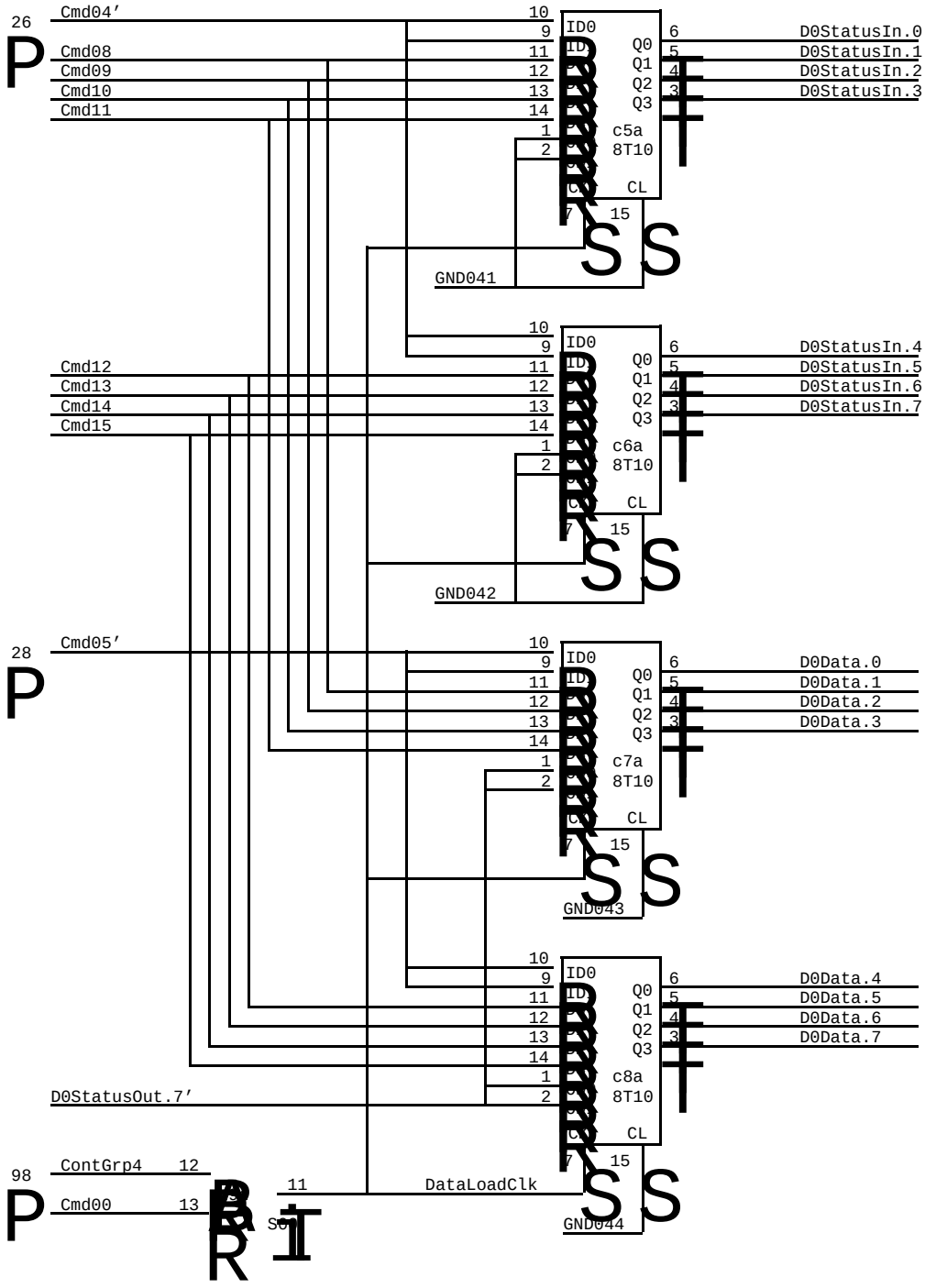
XEROX EOD	Project D0	D0Tester Data Transfer, Read Nibble	File D0TesterF05.sil	Designer J.F.Cameron	Rev D	Date 11/10/77	Page 05



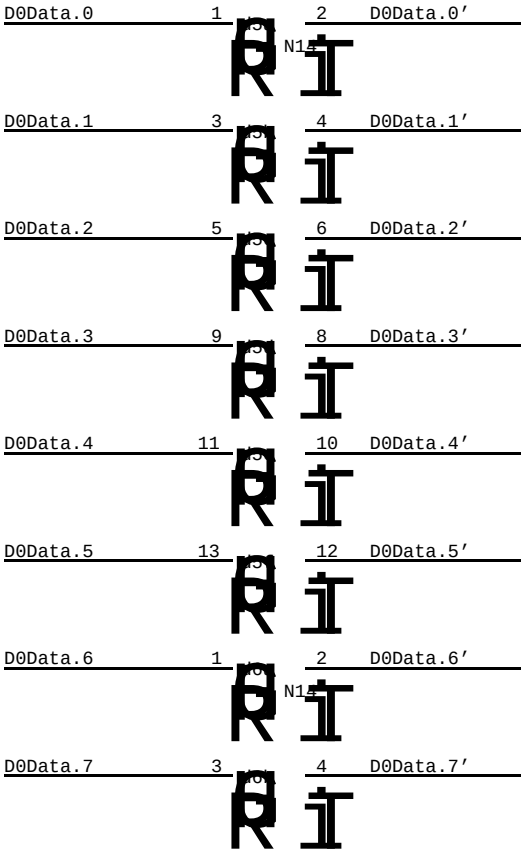
XEROX EOD	Project D0	D0Tester Pin Control, Read Control Group	File D0TesterG01.sil	Designer J.F.Cameron	Rev D	Date 9/19/77	Page 01

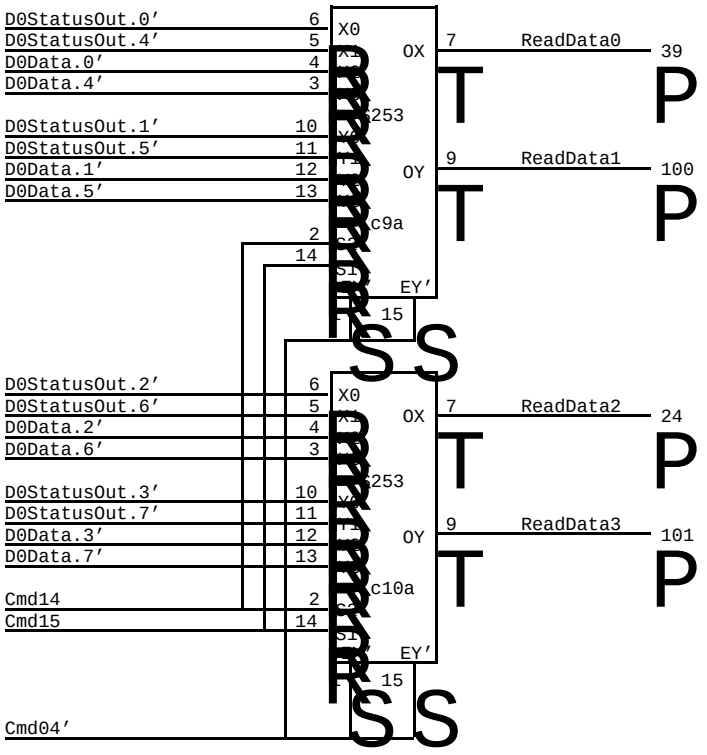


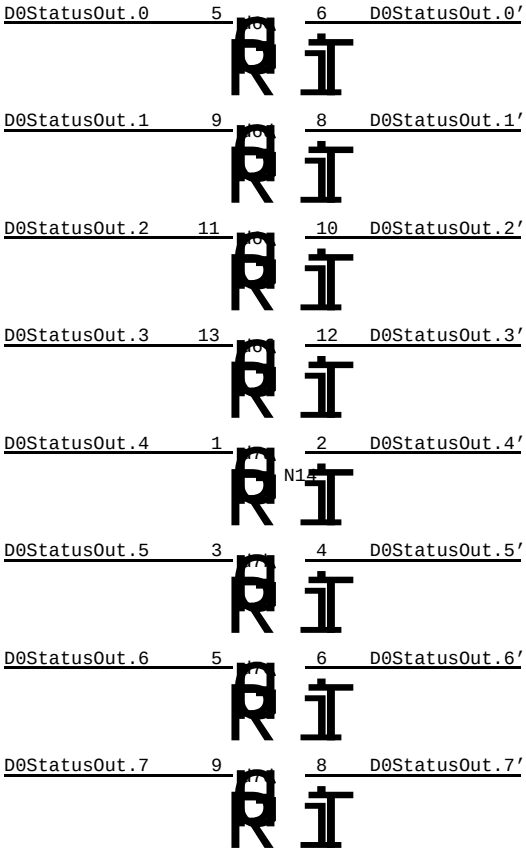
XEROX EOD	Project D0	D0Tester Pin Control, Set Pin Group	File D0TesterG02.sil	Designer J.F.Cameron	Rev D	Date 9/19/77	Page 02

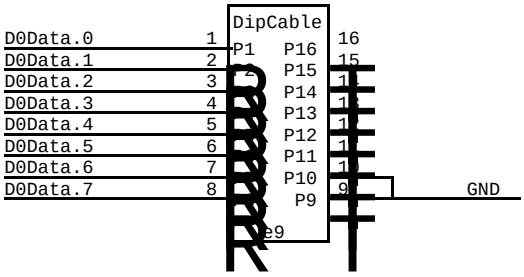


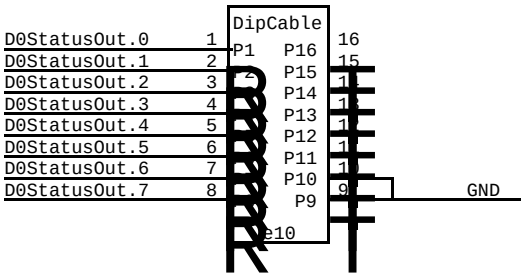
XEROX EOD	Project D0	D0Tester Data Transfer, Alto to D0	File D0TesterG03.sil	Designer J.F.Cameron	Rev D	Date 11/10/77	Page 03

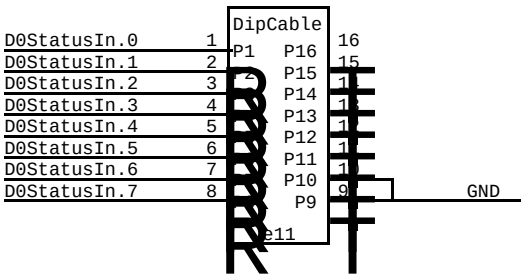




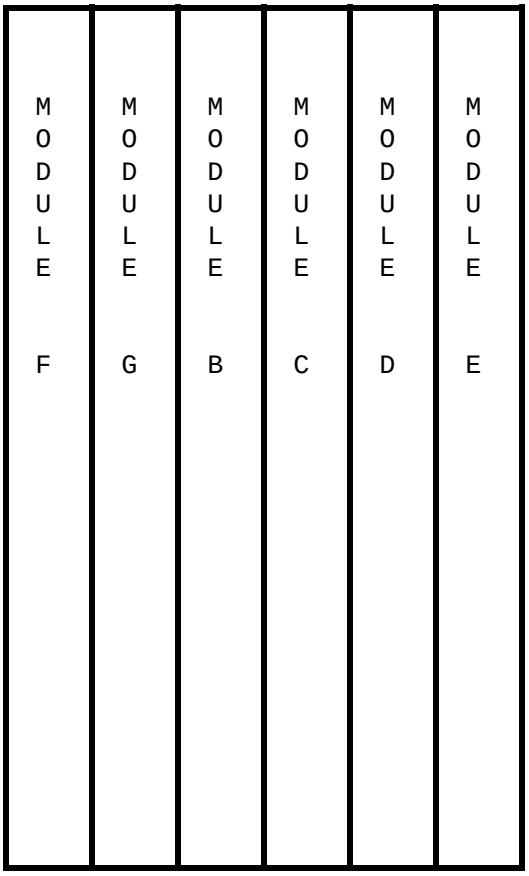




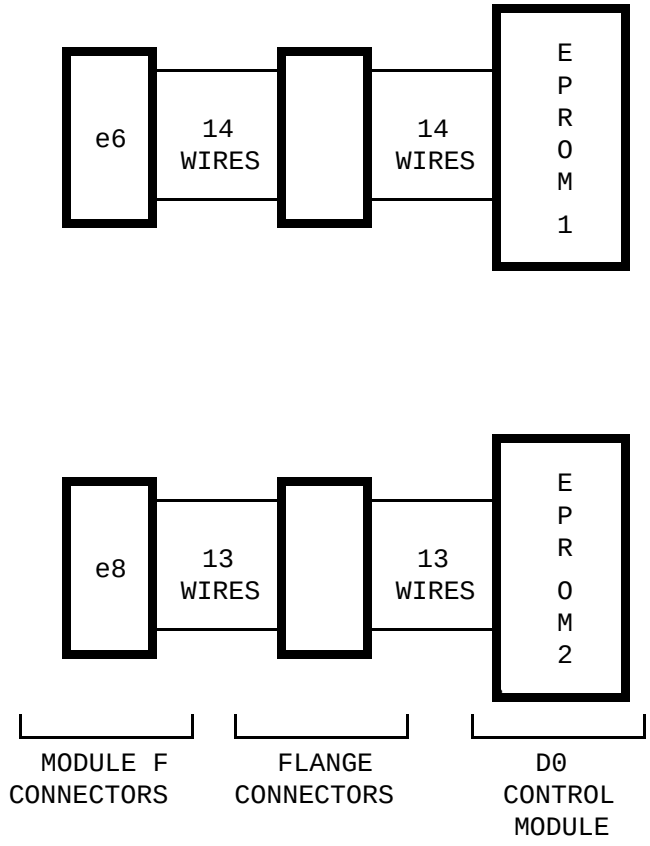




XEROX EOD	Project D0	D0Tester Data Transfer, Read Nibble	File D0TesterG04.sil	Designer J.F.Cameron	Rev D	Date 11/10/77	Page 04

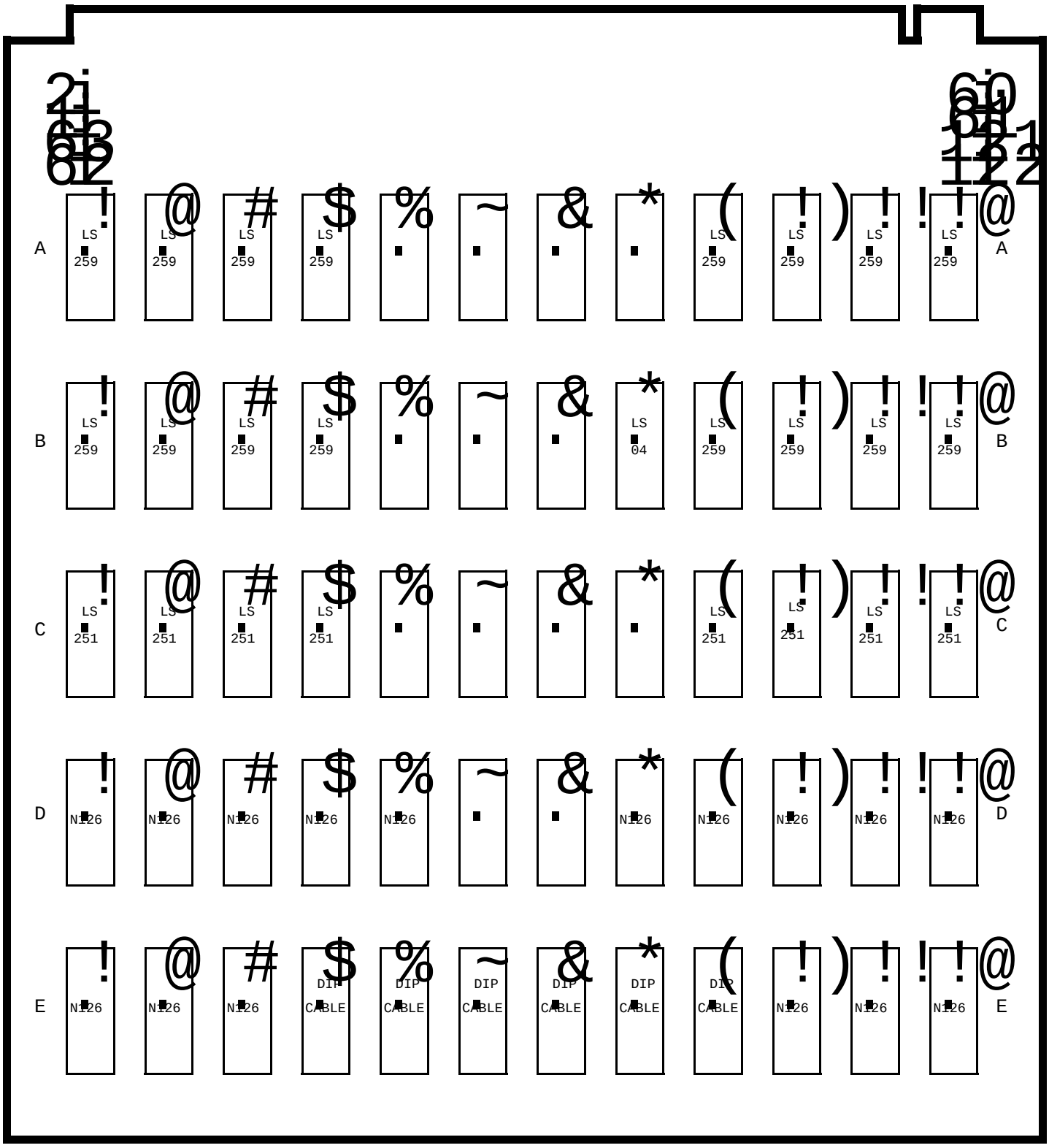


Tester Module Arrangement in Card Cage



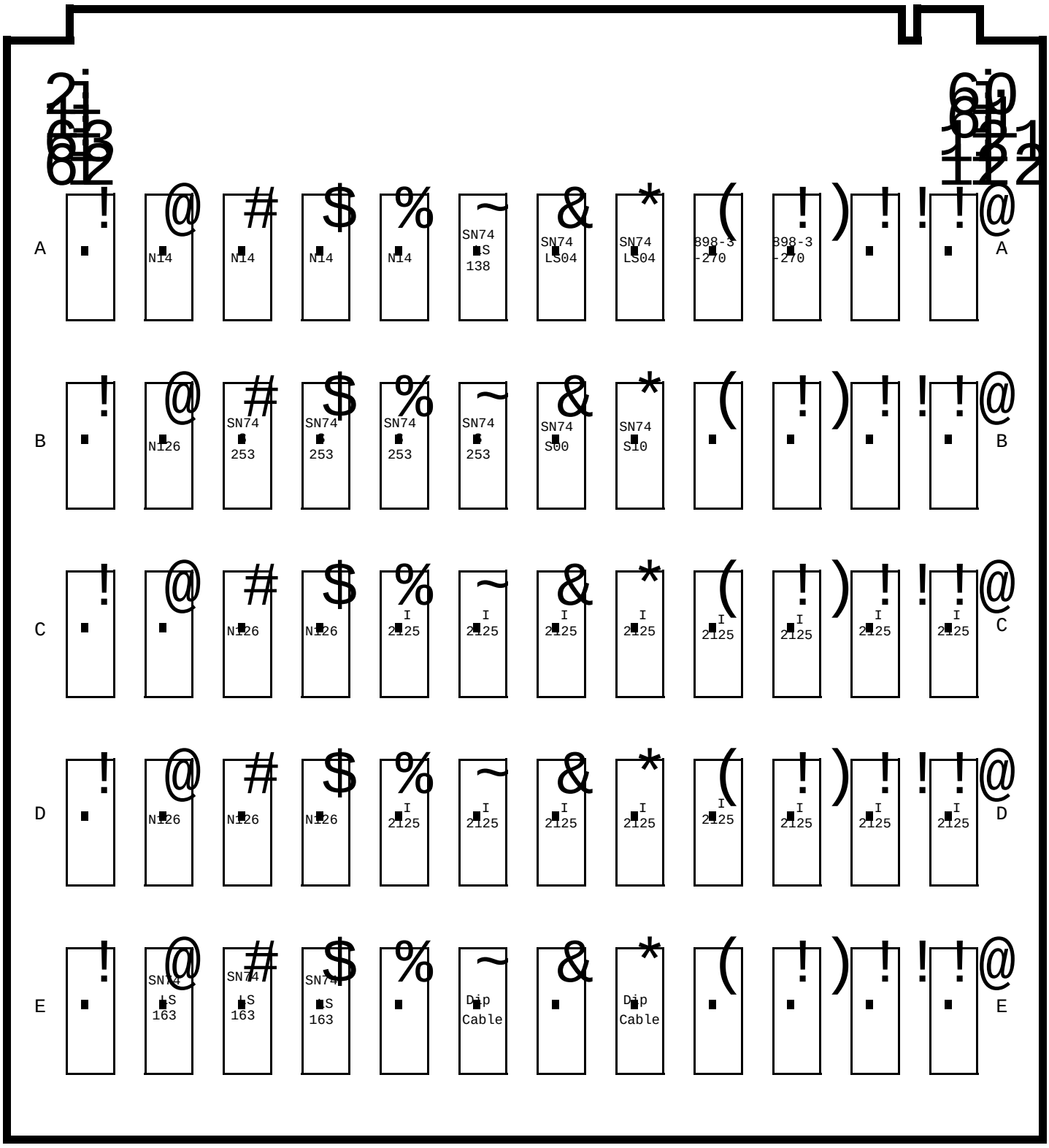
Eprom Simulator Cabling

XEROX EOD	Project D0	D0Tester Layout and Cables	File D0TesterLayout.sil	Designer J. F. Cameron	Rev B	Date 10/07/77	Page 01



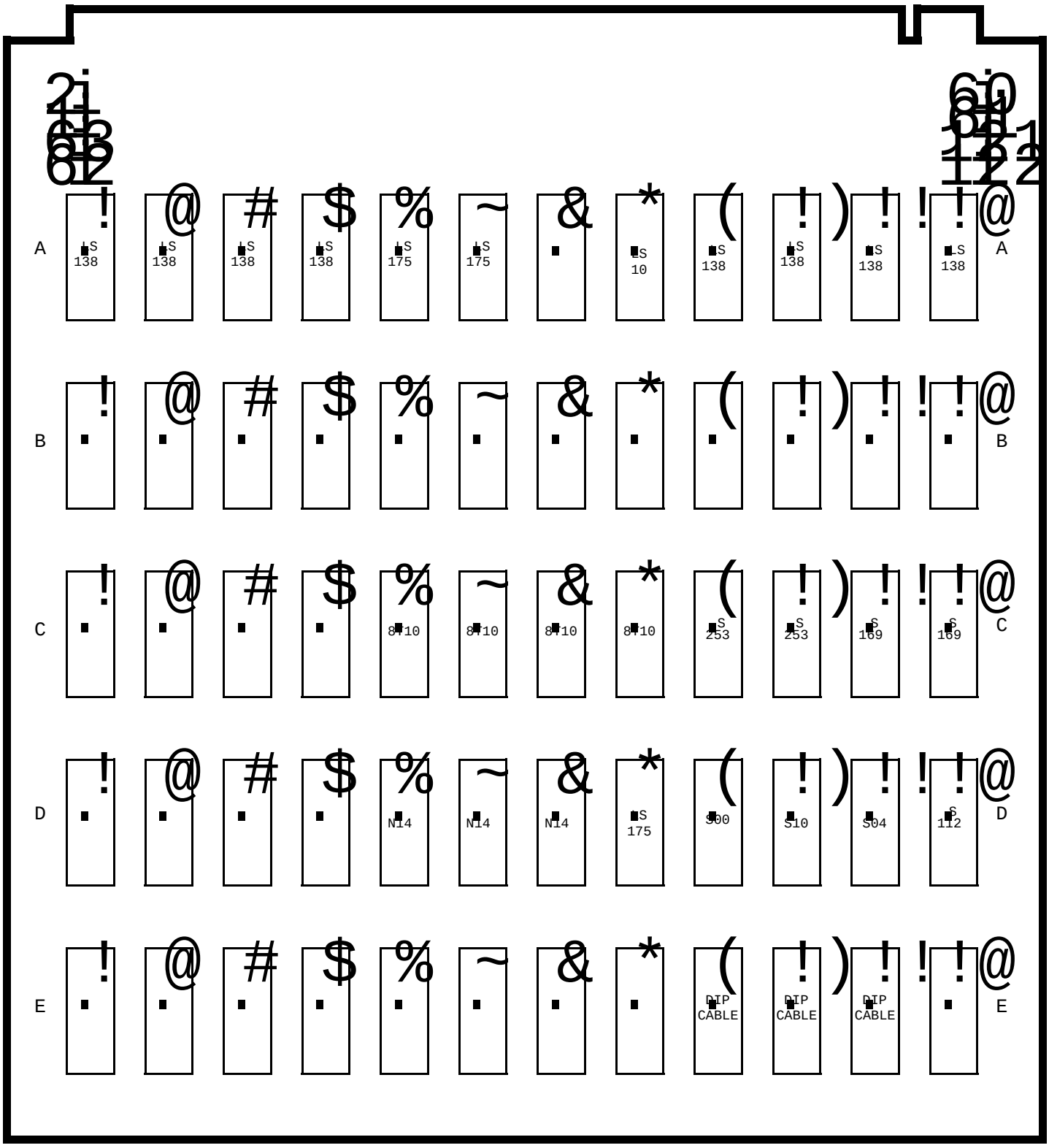
D0 TESTER CARD B,C,D,E

COMPONENT SIDE



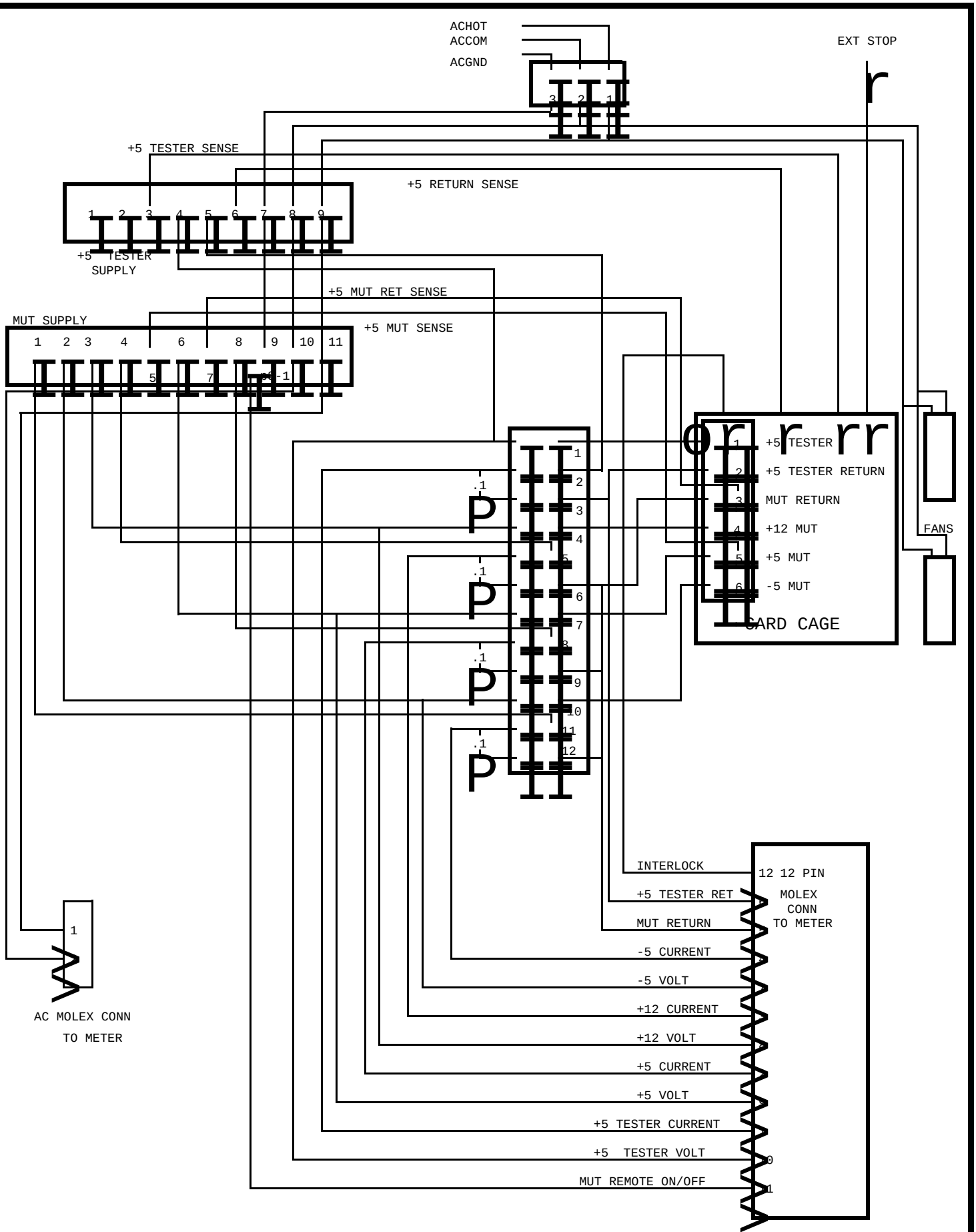
D0 TESTER CARD F

COMPONENT SIDE

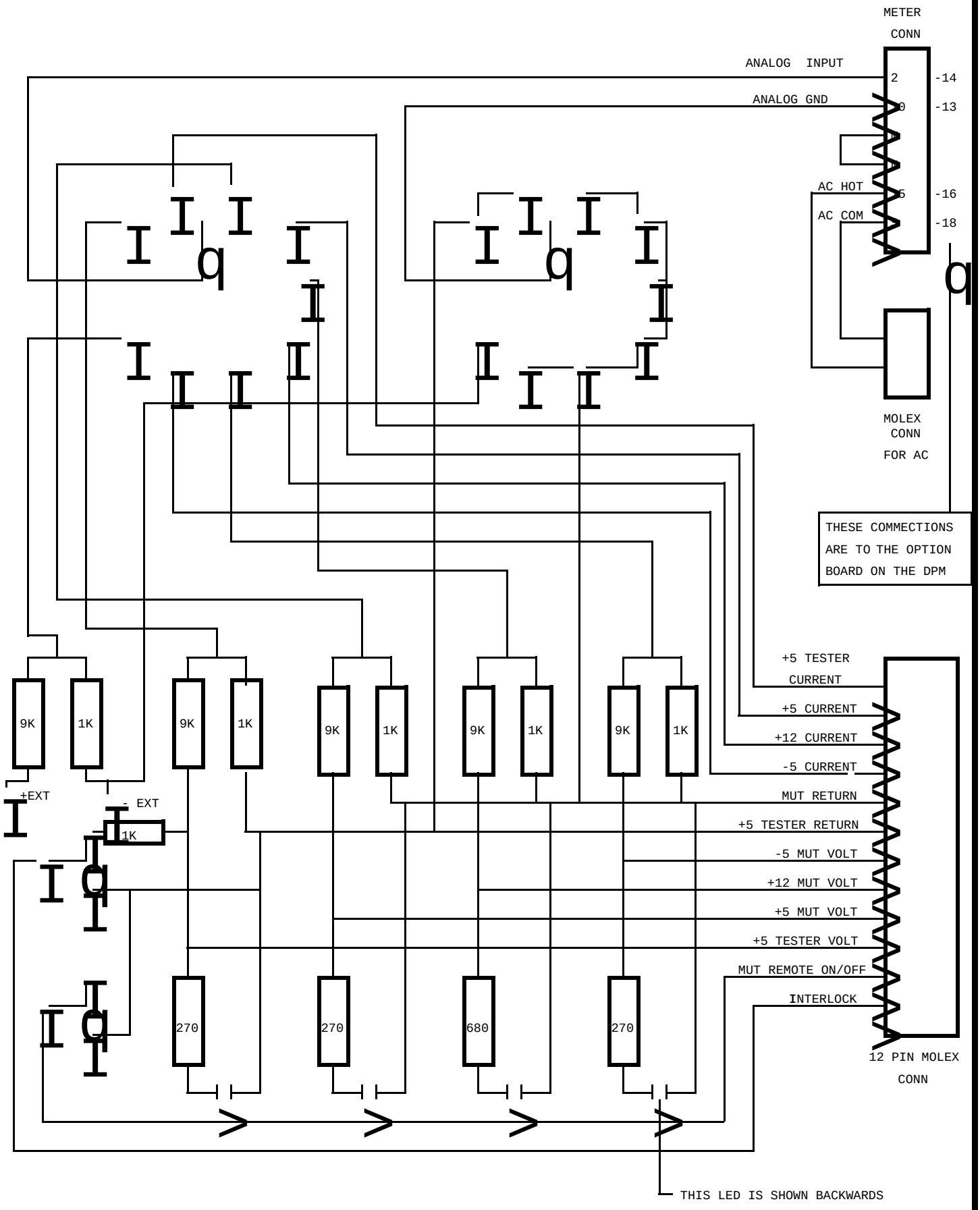


D0 TESTER G BOARD

COMPONENT SIDE



XEROX	PROJECT:	DRAWING:	DESIGNED by:	REV.	DATE:	PAGE:
CSL	D0TESTER	D0TesterWirng1.sil	VEST	A	3/22/79	1



METER CIRCUITRY

XEROX	PROJECT:	DRAWING:	DESIGNED by:	REV.	DATE:	PAGE:
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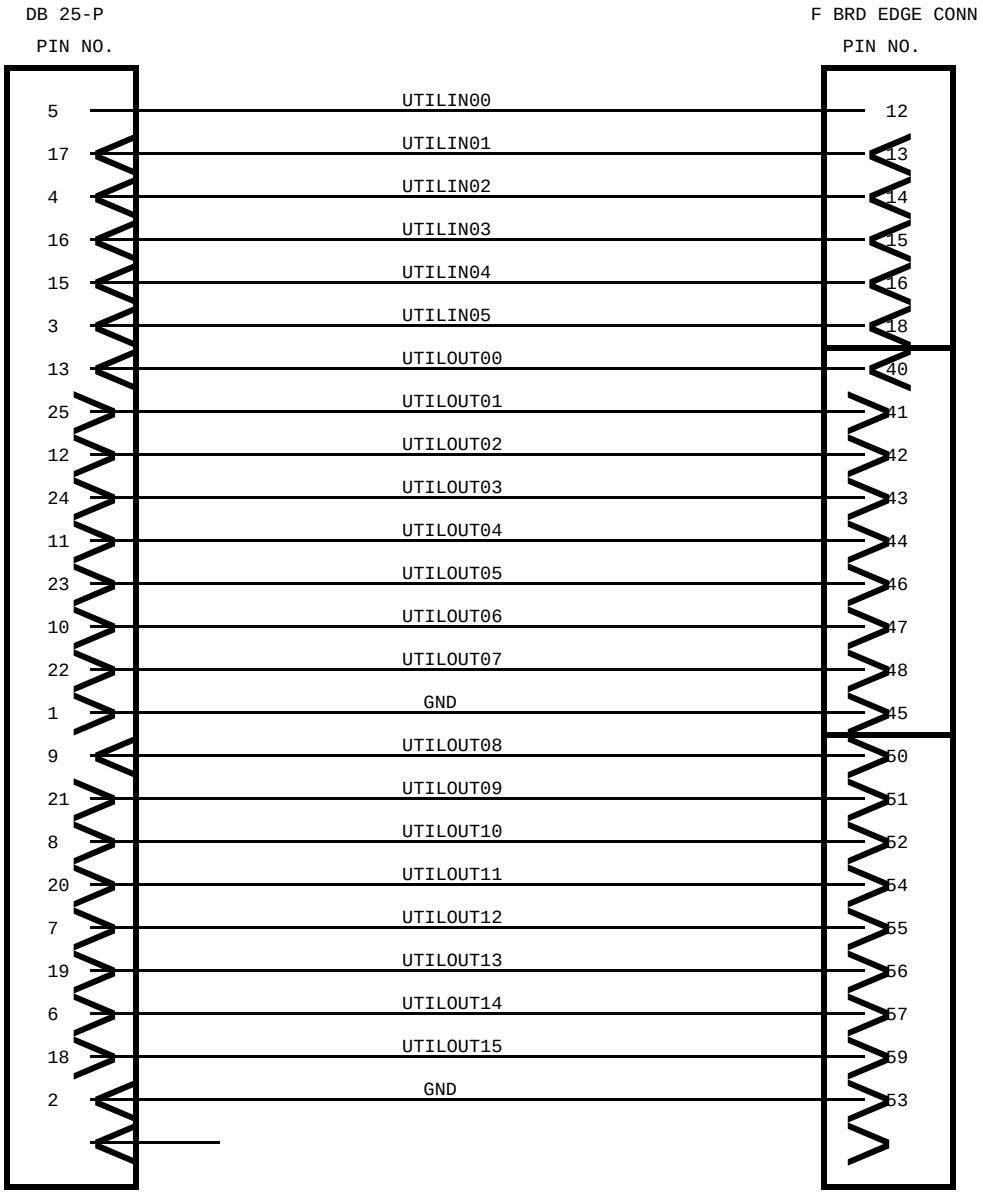

THE ABOVE IS A DIAGRAM OF THE INTERNAL CABLING OF THE UTILIN AND UTILOUT BITS FROM THE F BRD EDGE CONN VIA BERG CONNS TO THE DB25-P FOR THE ALTO THAT IS LOCATED ON THE D0TESTER INTERFACE PLATE.