

Figure 1: Dorado block diagram

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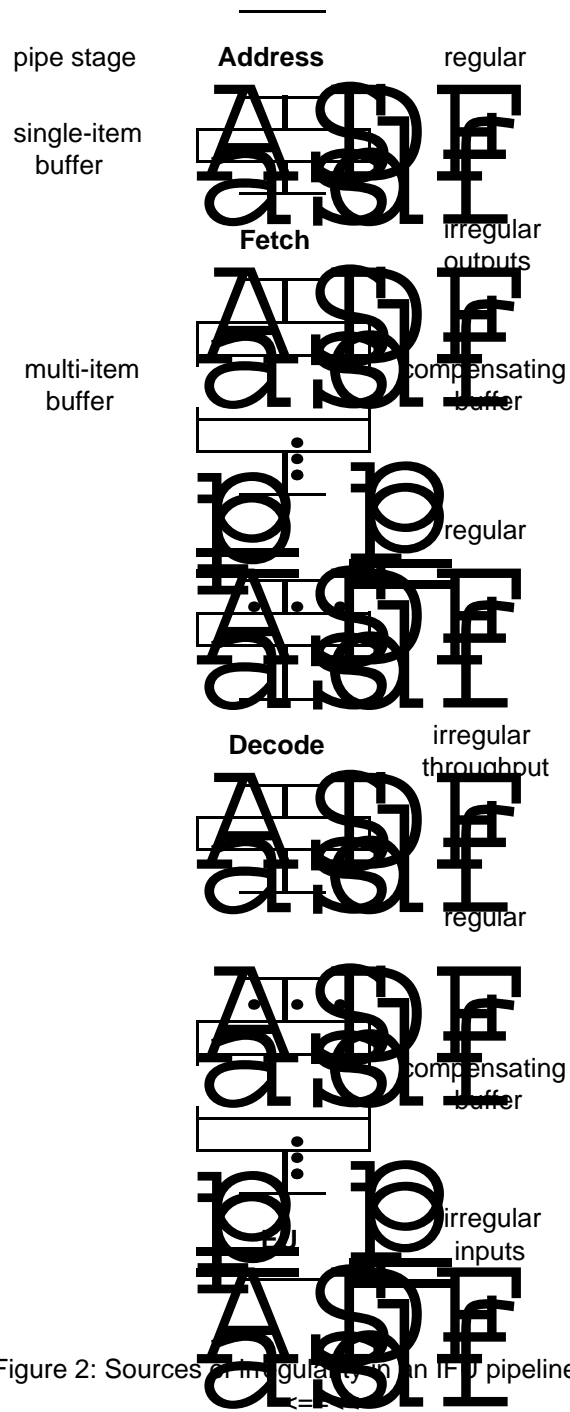


Figure 2: Sources of irregularity in an IFU pipeline

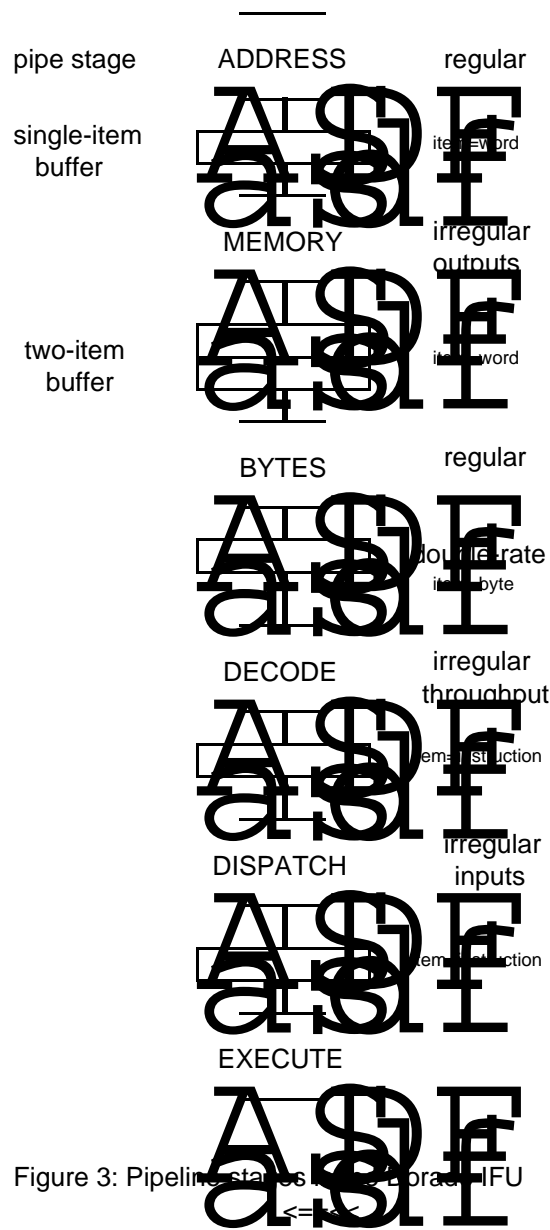


Figure 3: Pipeline stages in the processor IFU

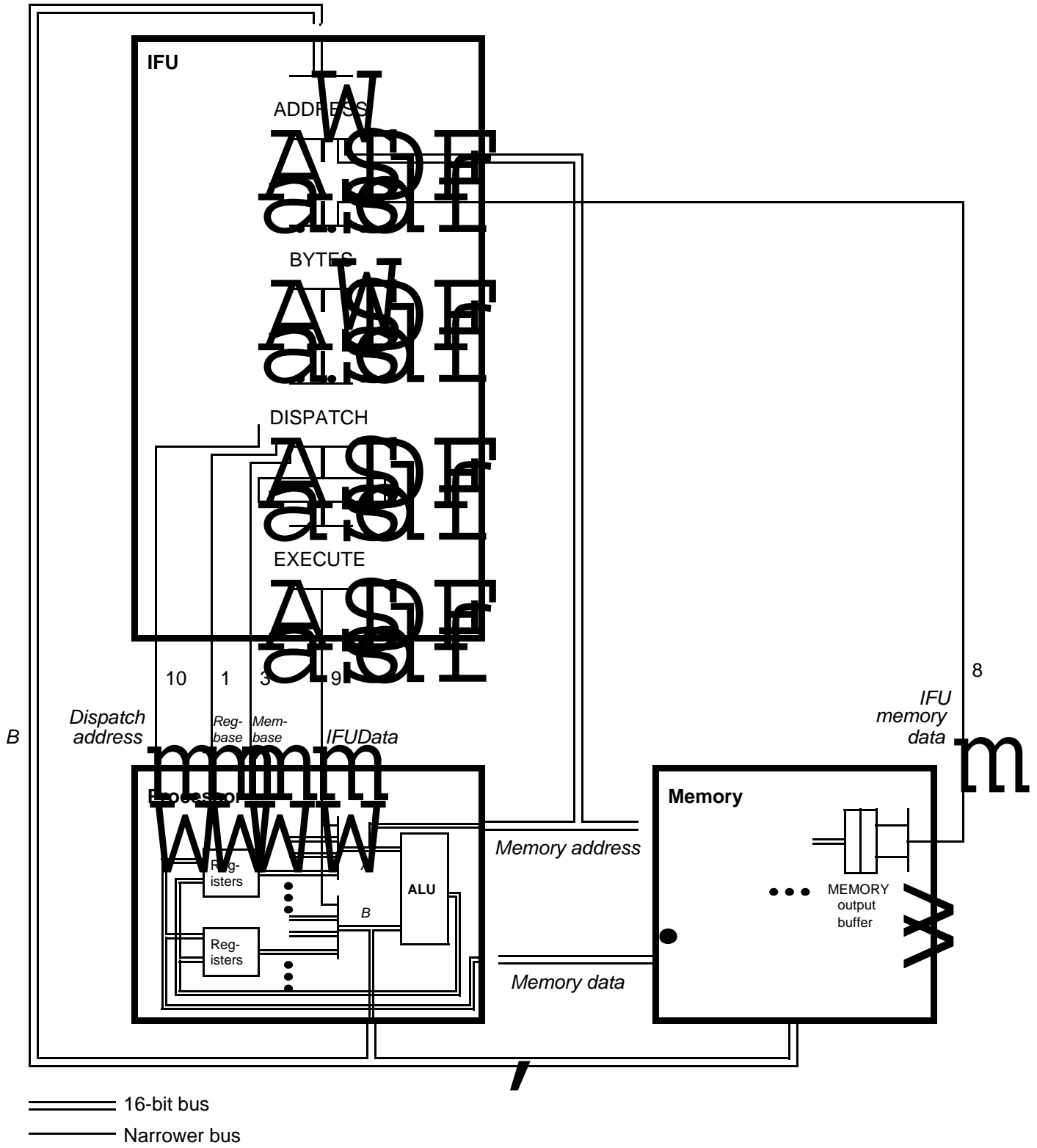


Figure 4: Busses between the IFU and the processor/memory

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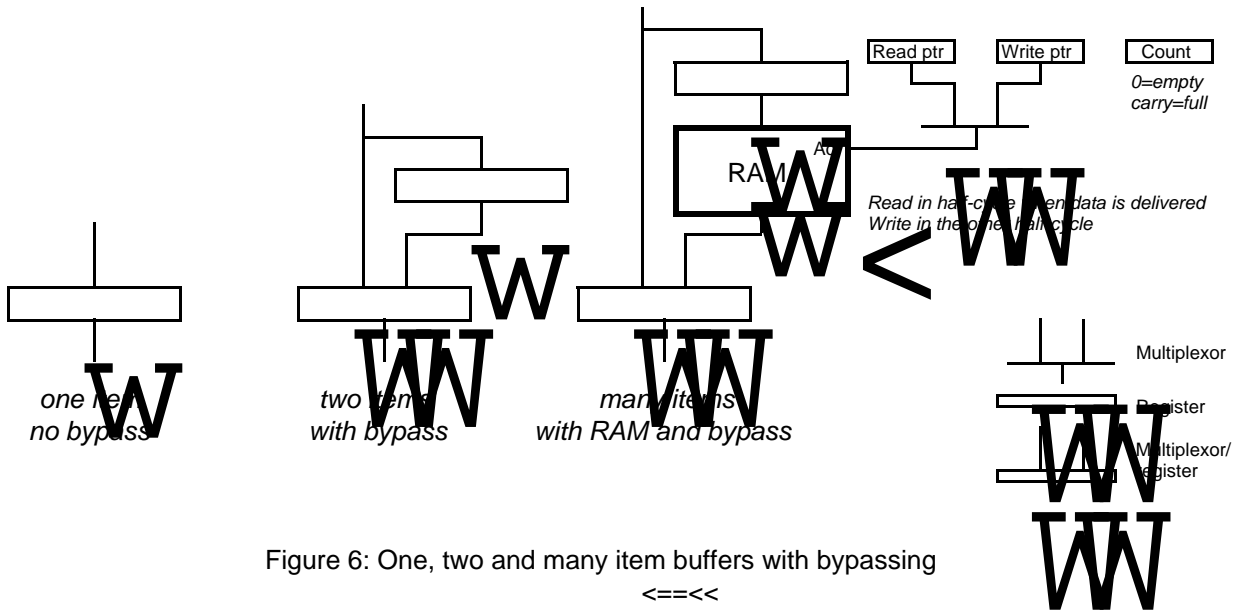
ADDRESS buffer	4	4	4	4	—	5	—	6
MEMORY buffer	3	3	3	—	4	—	5	—
BYTES buffer	2	2	—	3	—	4	—	5
DECODE buffer	1	—	2	—	3	—	4	—
processor has	—	1	—	2	—	3	—	4

Figure 5a: Cogging with local control and one item buffering

ADDRESS buffer	7,8	7,8	7,8	7,8	-,8	-,9	-,10	-,11
MEMORY buffer	5,6	5,6	5,6	-,6	-,7	-,8	-,9	-,10
BYTES buffer	3,4	3,4	-,4	-,5	-,6	-,7	-,8	-,9
DECODE buffer	1,2	-,2	-,3	-,4	-,5	-,6	-,7	-,8
processor has	—	1	2	3	4	5	6	7

Figure 5b: Smooth operation with local control and two item buffering

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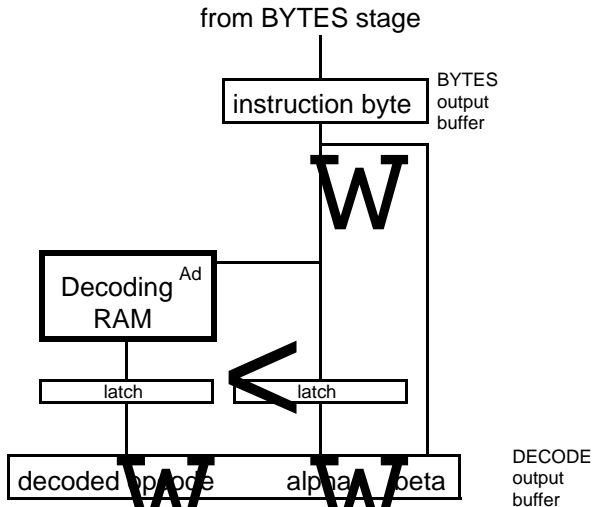


Figure 7a: Simple implementation of DECODE

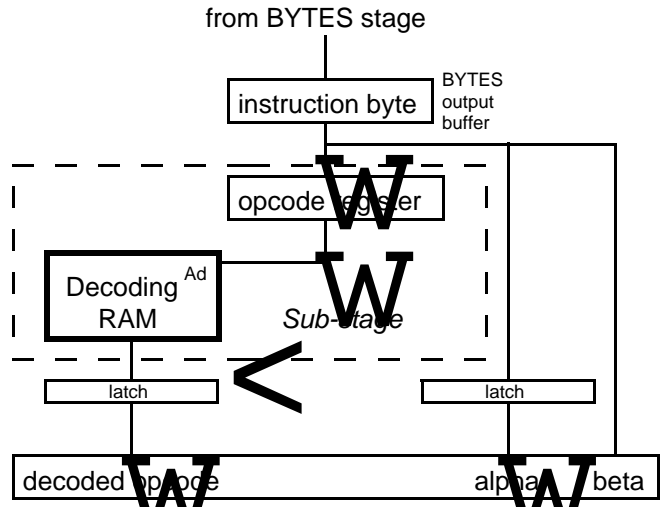


Figure 7b: Sub-stage implementation of DECODE

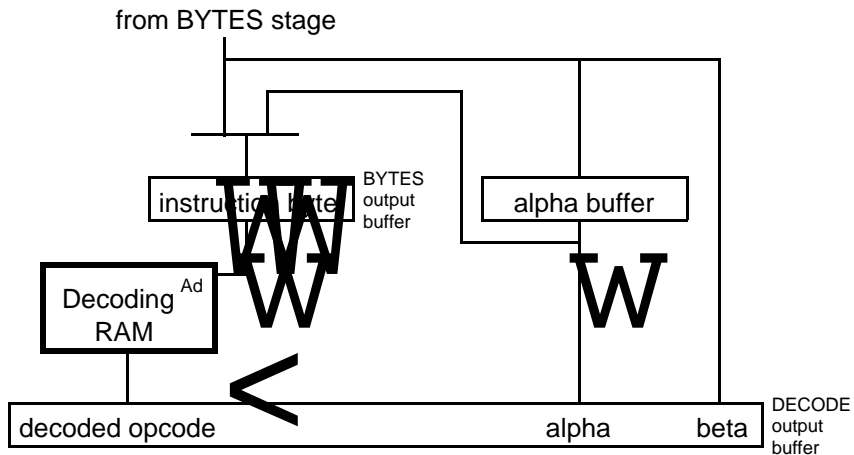
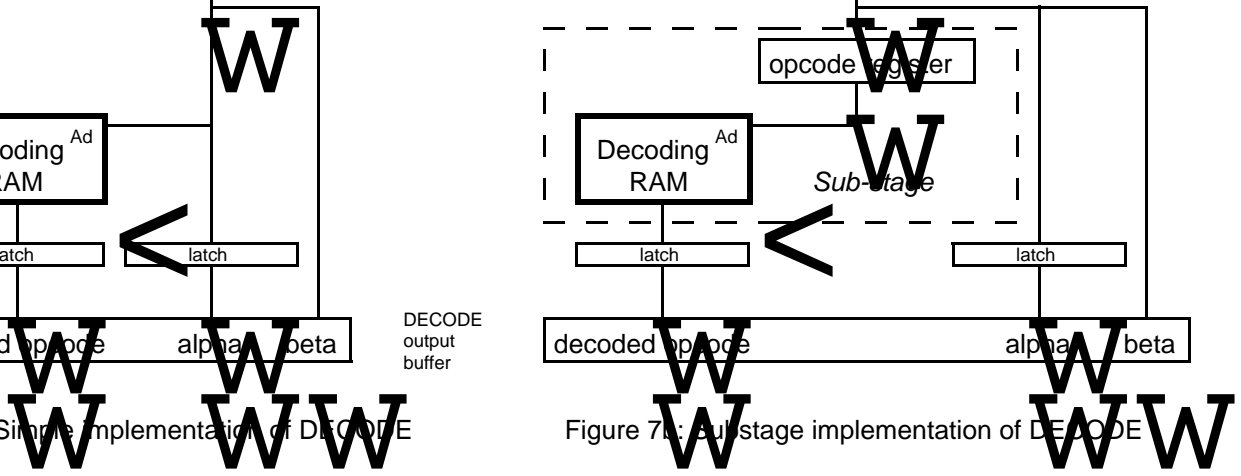


Figure 7c: Recycling implementation of DECODE



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