Dorado PC Board Spec of November 2, 1982 12:34 PM

1.0 Scope

This specification covers end product requirements for multilayer printed boards for the CSL Dorado computer system. These boards consist of six layers; four of which are used for signal interconnection, with the remaining two layers for power and ground distribution.

2.0 Applicable Documents

The following documents of the issue currently in effect form a part of this specification to the extent specified herein. In the event of conflict between these documents and this specification, the requirements of this specification shall govern. In the event of conflict between this specification and the fabrication drawing, the requirements of the fabrication drawing shall govern.

2.1 Institute of Printed Circuits

IPC-T-50 - Terms and Definitions

IPC-ML-910A - Design and End Production Specification for Rigid Multilayer Printed Boards

IPC-L-108 - Thin Laminates, Metal Clad, Primarily for High Temperature Multilayer Printed Boards

IPC-L-l09 - Glass Cloth, Resin Preimpregnated (B-Stage) for High Temperature   Multilayer Printed Boards

IPC-L-110 - Preimpregnated, B-Stage Epoxy Glass Cloth for Multilayer Printed Circuit Boards

IPC-L-30 - Thin Laminate, Metal Clad, Primarily for General-Purpose Multilayer Printed Boards

IPC-CF-150 - Copper Foil for Printed Circuit Applications

IPC-AM-372 - Electroless Copper Film

IPC-A-600 - Acceptability of Printed Circuit Boards

IPC-TM-650 - Test Methods Manual
- 2.1.1 Microsectioning
- 2.4.10 Plating Adhesion

IPC-ML-950 - Performance Multilayer Printed Circuit Boards

IPC-ML-975 - Multilayer Printed Wiring Documentation

2.2 Department of Defense

MIL-C-14550 - Copper Plating, Electrolytically Deposited

MIL-G-45204 - Gold Plating (Electrodeposited)

MIL-I-46058 - Insulating Compound, Electrical

2.3 Federal

QQ-N-290 - Nickel Plating (Electrolytically Deposited)

2.4 American Society for Testing and Materials

ASTM-E-53 - Methods for Chemical Analysis of Copper

2.5 American National Standards Institute

USASI Y 14.5-1973 - Dimensioning and Tolerancing for Engineering Drawings

2.6 Underwritters Laboratory

UL746 - Printed Wiring Boards

3.0 Requirements

Note: The use of letters [A,B,C, etc.] in this specification are for clarification purposes; they are used in equations, tables, text, etc., and are represented in Figure 1 of IPC-ML-910A.

3.0.1 Definitions. The definition of terms used in this specification shall be in accordance with IPC-T-50 and the following:

a. *Functional Land*. A land required for circuit interconnection or termination.

b. *True position*. [reference USASI Y 14.5-1973] The theoretically exact location of a feature established by basic dimensions.

3.1 Dimensions and Tolerances. All dimensions and tolerances specified herein are applicable to the finished product only. All artwork and design considerations must include proper compensation for the particular processes being used in order that these end product requirements can be met. A visual description of the items specified is deliniated in Figure 1.

Note: Unless otherwise noted, all dimensions and tolerances in this specification are in inches. Reference information is in brackets [ ].

3.1.2 Conductors

3.1.2.1 Conductor Thickness [A] and Tolerance [Atol] The initial copper prior to etch shall be 0.5 oz/sq ft. on all signal layers. The initial copper prior to etch shall be 2 oz/sq ft. on the power and ground layers. The nominal conductor thickness and its tolerance shall be specified in accordance with IPC-CF-150, for 2 oz and 1/2 oz material.

3.1.2.2 Conductor Width [B]. Nominal conductor width [B], shall be 0.006 for inner signal layers. Nominal conductor width shall be 0.008 for outer signal layers.

3.1.2.3 Conductor Width Tolerance [Btol]. The conductor width tolerance, due to fabrication processes but not including master pattern tolerances [see 3.1.6.1], shall not exceed +/- 0.001 for inner signal layers and shall not exceed +/- 0.002 for outer signal layers.

3.1.3 Spacing

3.1.3.1 Conductor Spacing, Coplanar [C]. The minimum conductor spacing [Cmin] between conductors on the same layer of the board shall be not less than 0.007 inch minimum.

3.1.3.2 Conductor to Hole Spacing [D]. The minimum spacing [Dmin] between an internal conductor and the wall of a plated through hole shall be not less than 0.007 inch minimum.

3.1.3.3 Layer to Layer Spacing [E]. The minimum spacing between conductors on adjacent conductive layers of the board [Emin] measured perpendicular to the layers shall be 0.003 inch.

3.1.3.4 Conductor to Edge of Board [U]. The minimum spacing between a conductor and the edge of the board [Umin] shall be 0.040 inch on the external layers. This spacing on the internal layers shall be 0.040 inch minimum.

3.1.4 Lands. At every point where a conductor is to be connected to a through hole there shall be a land with a diameter that is larger than the drilled hole.

3.1.4.1 Annular Rings [F&G]. The minimum annular ring is the minimum distance between the edge of a functional land and the edge of the drilled or etched hole. Minimum annular ring on internal layers [Fmin] shall be 0.001 and external layers [Gmin] shall be 0.002.

3.1.5 Holes

3.1.5.1 Hole Location Tolerance [K]. The location of holes shall be within 0.006 true position radius of the .025 grid location.

3.1.5.2 Unplated Hole Diameter Tolerance [Ltol]. The unilateral tolerance for unplated holes [Ltol], i.e., the difference between the maximum and minimum hole diameters, shall be 0.006, or as specified by the fabrication drawing.

3.1.5.3 Plated Hole Diameter Tolerance [Mtol]. The unilateral tolerance for plated holes, i.e., the difference between the maximum and minimum plated hole diameters shall be 0.006, or as specified by the fabrication drawing.

3.1.6 Feature Location Tolerance [N]. The tolerance allowance for the location of lands and conductors [including tolerances for master pattern accuracy, material movement, layer registration and fixturing] shall be 0.016.

3.1.6.1 Production Master Accuracy [W]. The location and size tolerances of all features on the production copies of the master artwork shall be +/- .003.

3.1.7 Composite Board Thickness [P]. The composite board thickness shall be measured across the board cross section extremities including metallic deposition, and shall be as specified by the fabrication drawing.

3.1.7.1 Board Thickness Tolerance [Ptol]. The bilateral board thickness tolerance shall be as specified on the fabrication drawing.

3.1.8 Smear removal. Holes made by the "plated-thru-hole" process are to have smear removal prior to plating.

3.2 Materials

3.2.1 Base Material The base material for individual layers of a general purpose multilayer board shall be in accordance with the requirements of IPC-L-130.

3.2.2 Bonding Agent The bonding agent used for the construction of a general purpose multilayer board shall be in accordance with requirements of IPC-L-110.

3.2.3 Plating [S]. Plating shall be one or a combination of several of the following and shall be specified on the fabrication drawing including applicable types and classes. Unless otherwise specified, plating thicknesses shall be as defined per the following paragraphs and shall be measured on the surface of the board or in the plated-thru-hole, as applicable.

3.2.3.1 Copper Plating. The minimum thickness of copper on the wall of a plated hole, except in areas of acceptable voids, shall be 0.001 inch [see 5.3.1]. All electrolytically deposited copper plating shall be in accordance with the requirements of ML-C-14550. Minimum purity shall be 99.5% as determined by ASTM-E-53. Electroless deposition of copper adherent to plastic and copper shall be used as a preliminary process for providing the conductive layer over nonconductive materials.

3.2.3.2 Nickel Plating. Where required low stress nickel plating shall be a minimum thickness of 0.0002 inch on the connector fingers. All electrolytically low stress nickel plating shall be in accordance with Federal Specification QQ-N-290.

3.2.3.3 Gold Plating. Where required gold plating shall be a minimum thickness of 0.000050 [50 millionths] inch over plated nickel on the connector area of the board. All electrolytically deposited gold shall be in accordance with the requirements of ML-G-45204.

3.2.3.4 Tin-Lead Plating [Fused]. When required tin-lead plating shall be 50-70 percent tin content. Fusing [reflowing] shall be required on all tin-lead plated surfaces. The fused tin-lead shall be 0.0003 inch thick minimum, when measured at the crest, and shall be homogeneous and completely cover the conductors [not intended for conductor edges] without pitting, pinholes, etc.

4.0 Performance Requirements

4.1 The multilayer boards shall be manufactured and processed so that they are in accordance with those requirements of IPC-ML-950 specified on the fabrication drawing.

5.0 Acceptability Requirements

5.1 The multilayer boards shall be manufactured and processed to meet the applicable requirements of IPC-A-600.

5.2 Conductors

5.2.1 Defects. Conductor defects such as pin holes, pits, nicks or ragged edges shall be acceptable if they do not reduce the conductor width more than 20 percent below the minimum specified on the master drawing in a localized area. Surface defects, such as scratches, shall not reduce the conductor below its minimum allowable cross section, Amin x Bmin.

5.2.2 Undercut. The plated conductor undercut on the surface layers shall not reduce the conductor width below the minimum specified by 3.1.2, and shall not exceed 0.001 inch per 0.001 of copper thickness, on a side.

5.2.3 Separation. When tested, in accordance with Test Method 2.4.10 of IPC-TM-650 [Plating Adhesion], conductors shall not show any evidence of separation from the base laminate nor shall any plating show evidence of separation from a conductor.

5.3 Holes

5.3.1 Plating. The metallic interlayer connection in the hole shall be continuous. When examined under 10x magnification in accordance with Test Method 2.1.1 of IPC-TM-650 [Microsectioning], the hole may have one pin hole or void not to exceed 10 percent of the wall area. This defect shall not appear on more than 90 degrees of the hole's circumference or at the interface between a land and a plated hole. This condition shall not be present in more than 5% of all of the holes on the board.

5.4 Electrical Continuity. There shall be 100 percent continuity on all conductors of the board as specified by the master artwork.

5.5 Solderability. The board shall be solderable under the following conditions. When exposed to 500 degree solder wave for 10 seconds there shall be no evidence of delamination, blistering or craking of plated through holes. When soldered usiong normal wave soldering techneques the board shall provide good wicking action onto component leads.

6.0 Packaging

Finished boards before shipment shall be baked at 120 degrees C - 150 degrees C for one hour before packing into a plastic bag. After prolonged storage prior to shipment, the boards should be subjected to the same drying cycle again prior to shipment.

7.0 Vendor Responsibility

7.1 Vendor Supplied Data and Samples

7.1.1 Cross Sections. The vendor shall supply to Xerox Corp. at least two mounted cross-sections from at least one board per manufacturing lot. If the lot size exceeds 20 pieces the vendor shall provide sections from two boards. These cross sections should be taken from the center of the board under evaluation, however the vendor may present cross sections taken of the test coupon area with the written permission of Xerox Corp.

7.1.2 Acceptability Statement. The vendor shall supply to Xerox Corp. a statement of acceptability to section 5 of this specification. This statement shall contain a list of tests performed on the boards or samples, the date of test and the signature of the Quality Assurance personal responsible for the test results.

7.2 Source Inspection Privlage. The vendor shall allow Xerox Corp., with reasonable notice, source inspection rights during any part of the manufacturing process, whether performed by the vendor or his subcontractors. This visitation right shall be without additional cost to Xerox Corp.