Inter-Office Memorandum

To	Dorado Group	Date	19 September 1979
From	Roger Bates	Location	Palo Alto
Subject	Build Standards	Organization	CSL

XEROX

Filed on: [Ivy]<DoradoDocs>BuildStandards.press
Sources on: [Ivy]<DoradoSource>BuildStandards.dm

This memo describes how to convert an existing set of drawings into the "standard" Dorado build system. References made to *rev* in the following description should be replaced by the current rev level of your board.

The essential changes implemented in this process are:

Use font 1 italic for small italics and free up font 2
Use font 2 for Template64 font for arcs and diagonal lines in comments
Change the default from bold font 0 and 1 to normal face font 0 and 1
Make minor changes to the title block for esthetic reasons
Pick a file naming convention where the "rev" is in all generated files

Disk Initialization

The procedure is best performed by starting from scratch with a new disk. If you don't do this, you stand the risk of running out of disk space due to the presence of unnecessary files on your disk. You should go through the following incantation:

Load a fresh disk and boot the Ether Executive;
Run NewOs.boot;
Install with long dialogue and ERASE the disk;
When the dust settles, retrieve [IVY]<DoradoLogic>DoradoDisk.cm;
Execute the "DoradoDisk.cm" command file;
When the dust settles again, load [IVY]<DoradoLogic>DoradoFiles.dm
Initialize Sil with Sil/I
Load from your last board dump file the current ".wl" file and all sil drawings--nothing else

The files contained in [IVY]<DoradoLogic>DoradoFiles.dm are ordered in INVERSE order of importance, so that you should run FTP in interactive mode, look at the files as they are presented and skip (DEL key) the files you don't need. Once you get the file Sil.run you should continue and accept all files.

The files contained are:

User.cm	"standard" Dorado-User.cm file
SendBuild.chatcm	Template for chat command to archive .dm file
RouteSB.br RouteMWSB.br	Board characterization for the MSA board
TtlDict.analyze Sil.lb5 Sil.lb6	TTL stuff - only get if necessary
Routemlb.br RouteMwlb.br	Board characterization for the Logic board
Sil.run Analyze.run Route.run Build.run	All required run programs
Sil.lb7 Sil.lb8 Dorado.lb9	ECL component library files
EclDict.analyze DoradoDict.analyze	Required dictionary files
NewSwRev SwBuild.cm SwReBuild.cm	Command files for stitchweld boards
NewMwRev MwBuild.cm MwReBuild.cm	Command files for multiwire boards
BuildBackupTemplate.cm	command file for actions after running Route

(These files are enumerated in [Ivy]<DoradoLogic>DoradoFiles.cm.) I recommend that you skip unnecessary files to avoid problems with full disks. When in doubt, retrieve the file, then delete later if you haven't used it. TtlDict.analyze, Sil.lb5, and Sil.lb6 will be required on some boards that do not use any TTL components because some terminators are defined in these files.

User.cm

The User.cm file supplied defines the Sil fonts and Libraries etc. It defines a Bravo init macro used in BuildBackupTemplate.cm and also defines the Bravo fonts such that a minimum of font files are required on the disk. The DoradoDisk.cm command file also does "copy SysFont.al _ Helvetica10.al" so that Type.run will print wirelist files semi-reasonably.

Wire List file

Change the name of your current ".wl" file to *Board*-Rev-*rev*.wl

Board Specific files

You will have to create four files as follows:

File Name	*Contents*
"Board"	Board name such as "ProcL"
"Slot"	Slot number such as "s04"
"Rev"	Current existing rev such as "Cf"
"Addendum"	Space, optional switches, or added sil files for Build

The files (except "Addendum") must contain *exactly* the text specified, with no leading spaces or trailing spaces or carriage returns.

The catch-all file "Addendum" is called from all of the Build-invoking command files. It allows you to include commands to build which are not in the standard command files, or to include sil files which will not be caught by the standard expansion of "Board##.sil" entry.

In addition to these files which you must create, other files "OldRev" and "OldOldRev" will be created by sucessive reworks to a board as they are needed.

Creating a Standard Title Page

Retrieve the file [IVY]<DoradoLogic>Title-Rev-Ab.sil and edit the file as appropriate. when you are done, you should rename it to *Board*-Rev-*rev*.sil and delete you old title page and Title-Rev-Ab.sil. Note: the title page does not have Title block entry for "page" number, rather it has a place for you to manually enter the page number of the last page. Note that Analyze will flag a level 1 error (warning) that it could not find the page number, but this is OK.

Standardizing Your Sil Drawings

You will need to go through each drawing and perform the following manipulation.

Change all font 2 strings to font 1 italic using the followings commands:

^V 2	select all strings in font 2
^J 1	Jam selected strings to font 1
^J i	Jam selected strings to italic

Select "XEROX" and "*PARC*" in the title block and Jam bold

Move the right end of the title block to match the end of the build marks. i.e. move the right most line left 2 grid 4 units (location x=564)

Set the "boldness" of all font 0 strings within your drawing as desired.

If you have a temperature sensor on the board, you should change the name of the platform from PLAT to TEMP. This will cause Route to put "LM3911+20K" in the loading chart.

In preparation for multiwire, you must declare any unused sockets that you want available for future fixes so that route will have the pins drilled in the multiwire board. The macro "L" in Dorado.lb9 is a macro named SPARE with pins 1,16 and 8 declared so that you can connect them to the signal "Whatever".

I would like to see all muffler input drawings changed to make use of Dorado.lb9 macros "@" and "#". These make it easier to locate signal bits within the midas muffler words.

Command Files for the Build Process

After completing the preliminary procedures above, you are ready to embark on a rework of the existing stitchweld board. To do this, you first execute the "NewSwRev.cm" command file *once only*; then you execute "SwReBuild.cm" as many times as necessary to get through without errors. The "SwBuild.cm" file is also provided to generate a brand new stitchweld board (i.e., a new design or major rev).

"NewMwRev.cm," "MwReBuild.cm," and "MwBuild.cm" are the equivalent command files for multiwire boards.

Below are listings and brief descriptions of these command files. To allow for human interaction

with command files, *there are occasional calls on non-existent files, which will cause the operating system to interrogate the user for the contents of the non-existent file*. There are two general situations when this occurs:

> In the command files that invoke Build, a call of the file "Switches" is made. At this point it is appropriate to type "*CR*" for all things standard, "A*CR*" to force Analyze to run on all files, "4*CR*" to restart at Route, or "6*CR*" to restart after Route.
>
> Within BuildBackupTemplate.cm, each operation is preceded by a call on some disk file such as "@DoNewPrescan@". If you want to perform the operation, then type "*CR*"; if you dont, type "//*CR*" to turn the operation into a comment. If you always want to execute some action, you may define the appropriate file as containing nothing.

@NewSwRev.cm@ is executed to cause appropriate name changes and deletion of old files in preparation for generating a NEW stitchweld REV for your board. You should execute this command file *once and only once* before a new rev. Before running, be sure that "Rev" contains the current rev for your board, and that "OldRev" (if is exists) contains the last stitchweld rev for your board. (The first time you carry out the build process there will be some confusion about files "OldRev" and OldOldRev" that don't exist--plunge on fearlessly). Its contents are:

```
Delete *.press *.wlOld
Delete *.ad *.bp *.comments *.er *.re *.pe *.lc *.ps *-E.nl *-C.nl *.inl *.mh *.mhi *.mw
copy OldOldRev _ OldRev
copy OldRev _ Rev
Bravo/n Rev
Rename @Board@-Rev-@Rev@.sil _ *Rev-##.sil  //rename the sil title page
Delete *Rev-##.nl  //Delete title page .nl file - Buildd will re-Analyze
Delete @Board@-Rev-@OldOldRev@.wl  //delete any very old wirelist file
Delete *-mwRev-##.wl  //delete any multiwire wirelist file

//Finally, clean up the system directory for speed and disk pages
Ftp MAXC retrieve/c <Alto>CleanDir.run
CleanDir SysDir 2000
Delete CleanDir.run
```

@SwReBuild.cm@ is executed to rework a stitchweld board. It will invoke Route in rework mode, using the ".wl" file from the existing board (*OldRev*) as the basis for the rework. This will cause the build process to be invoked, and should generate a new "null" rev of your board; all files generated by Analyze and Route will have the "Rev" level in their names. The need for "tentative" mode has gone away, since ".wl" is no longer copied into ".wlold", and therefore no file information is lost during the normal build process. You may now invoke SwRebuild.cm as many times as necessary to get through without errors. Its contents are:

```
// SwReBuild.cm -- last modified September 10, 1979  5:24 PM by Taft

Build/RC@switches@ @Rev@/R E/GM @Slot@/GL RouteMLb.br/GB /GR ^
@Board@-Rev-@OldRev@.wl/GC ^
0/p @Board@-Rev-@Rev@.sil @Board@##.sil @Addendum@
```

@SwBuild.cm@ is executed to create a stitchweld board from scratch (i.e., a new design or a major revision). Its contents are:

```
// SwBuild.cm -- last modified September 10, 1979  5:24 PM by Taft

Build/R@switches@ @Rev@/R E/GM @Slot@/GL RouteMLb.br/GB /GR ^
0/p @Board@-Rev-@Rev@.sil @Board@##.sil @Addendum@
```

@NewMwRev.cm@ is similar to NewSwRev.cm; it is executed *once and only once*, when you have a working stitchweld board and you want to build the equivalent multiwire board. It deletes all unnecessary files, and renames the Title page name to Board-mw ___Rev-*rev*.sil as the convention to indicate a set of multiwire files. Its contents are:

```
Delete *.press *.wlOld
Delete *.ad *.bp *.comments *.er *.re *.pe *.lc *.ps *-E.nl *-C.nl *.inl *.mh *.mhi *.mw
Rename @Board@-mwRev-@Rev@.sil _ *Rev-##.sil  //rename the sil title page
Delete *Rev-##.nl  //Delete title page .nl file - Buildd will re-Analyze
Delete @Board@-Rev-@OldRev@.wl  //delete any old wirelist file
Delete *-mwRev-##.wl  //delete any multiwire wirelist file

//Finally, clean up the system directory for speed and disk pages
Ftp MAXC retrieve/c <Alto>CleanDir.run
CleanDir SysDir 2000
Delete CleanDir.run
```

@MwBuild.cm@ is executed to create a multiwire board from scratch. No new errors should occur except possibly those associated with power pin connections. The multiwire board has numerous restrictions about non-standard ECL power on pins 1,8, and 16.

```
// MwBuild.cm -- last modified September 10, 1979  5:24 PM by Taft

Build/RM@switches@ @Rev@/R E/GM @Slot@/GL RouteMwLb.br/GB /GR ^
0/p @Board@-mwRev-@Rev@.sil @Board@##.sil @Addendum@
```

Note: if errors do occur during this operation, you should repair them and re-run @MwBuild.cm@ as many times as is required. Then, assuming that no corresponding stitchweld boards have actually been fabricated, you should retract the current stitchweld rev and redo it. That is, reload files *Board*-Rev-*OldRev*.wl, Rev, OldRev, and OldOldRev from *Board*-Rev-*OldRev* _____.dm, execute @NewSwRev.cm@, and then execute @SwReBuild.cm@. On the other hand, if stitchweld boards for *rev* have already been fabricated, you should of course make a new rev (both stitchweld and multiwire).

@MwReBuild.cm@ - This command file is used to generate a multiwire "rework". Of course, it is not actually possible to rework a multiwire board, but this is useful to formalize changes implemented by means of cuts and patches, or to perform null revs for documentation purposes.

```
// MwReBuild.cm -- last modified September 10, 1979  5:24 PM by Taft

Build/RCM@switches@ @Rev@/R E/GM @Slot@/GL RouteMwLb.br/GB /GR ^
@Board@-mwRev-@OldRev@.wl/GC ^
0/p @Board@-mwRev-@Rev@.sil @Board@##.sil @Addendum@
```

Due to disk space limitations, this command file is not quite as automatic as the others; it requires a few manual steps to delete and reload .wl files. To begin a multiwire rework, first make sure you are completely backed up. Execute @NewMwRev.cm@ (as usual), delete *.wl, load *Board*-mw ___Rev-*OldRev*.wl from *Board*-mw ___Rev-*OldRev*.dm, and then execute @MwReBuild.cm@ to invoke the Build process. When you are done multiwiring, delete *.wl and reload *Board*-Rev-*rev*.wl from *Board*-Rev-*rev*.dm in preparation for any future stitchweld rework.

In executing any of the above build command files, "BuildBackupTemplate.cm" will be processed by Build when finishing processing of a board. Build replaces the "$Z" entries per the build manual, and passes the results to the executive in Com.Cm. Its contents are:

```
// BuildBackupTemplate.cm -- last modified September 12, 1979  6:07 PM by Taft
```

```
//Check things out  ** Shift-SWAT ** to abort
type $ZN.e# $ZN.re $ZCN.ad

@DoNewPrescan@Analyze/p $ZAN.sil

//Make a dump file for IVY
@DumpToIVY@ftp ivy connect/c DoradoLogic dump/c $ZN.dm $ZCN.ad $ZN.wl $ZN.lc $ZN.resist $ZMN.mw
$ZMN.mh $ZMN.mhi $ZN.bp $ZRN-E.nl $ZRN-C.nl $ZAN.sil *Rev Board Slot Addendum $ZLF

//Make a dump file for MAXC archiving
@DumpToMAXC@ftp maxc/c connect/c d1logic dump/c $ZN.dm $ZCN.ad $ZN.wl $ZN.lc $ZN.resist $ZMN.mw
$ZMN.mh $ZMN.mhi $ZN.bp $ZRN-E.nl $ZRN-C.nl $ZAN.sil *Rev Board Slot Addendum $ZLF

//Delete the multiwire files just dumped to make room for the Drawing file!!!
@DeleteMultiwireFiles@Delete $ZMN.mw $ZMN.mh $ZMN.mhi $ZMN.resist

@DoNewDrawings@sil/p 6/x $ZAN.sil
@SendDrawings@ftp ivy connect/c DoradoDrawings store/s sil.press $ZN.press store/c $ZN.ps

//Now make up a message and send to Rosemary
@DoReworkMessage@Bravo/n sendBuild.chatCm
@SendReworkMessage@chat sendbuild.chatCm/D

@MakeListings@empress Sil.press  //drawings - need more double sided copies
@MakeListings@Bravo/h $ZN.ps  //prescan - need more double sided copies
@MakeListings@empress $ZN.lc $ZCN.ad  //loading chart (for Mike) & Add/delete list
@MakeListings@empress 6/p $ZN.wl //wire list - Mike needs copies of the first fiew pages
```

Documentation Distribution

The last operations in BuildBackupTemplate.cm file print copies of the drawings, prescan, wirelist, and prescan files. They should be distributed as follows:

Drawings, prescan, and wirelist to the Board Specific Binder

2-sided copies of drawings and prescan to each of the two Schematics Binders

Loading chart, first few pages of the wire list (which contains a location sorted list for checking), and a copy of the sil layout drawing to Mike’s Board Stuffing Binder.

Dorado-User.cm

[Dorado-User.cm]
Last modified September 4, 1979 3:43 PM by Taft

[EXECUTIVE]
eventRFC: FTP/K; Quit

[SIL]
0: Helvetica10
1: Helvetica7
2: Template64
3: Gates32
9: Dorado.lb9
Y: 712
A: DoradoDict.Analyze

[BRAVO]

N.INIT:"{6,1,0,0}g'@1{@@G[@1]@@E"

H.INIT:"{6,1,0,0}g'@1{@@G[@1]{6,2,0,0}h
{6,2,0,0}q
@@E"

FONT:0 Helvetica 10 Helvetica 10
FONT:1 Helvetica 8 Helvetica 7
FONT:2 Logo 24 Helvetica 10
FONT:5 Helvetica 12 Helvetica 10
FONT:6 Helvetica 10 Helvetica 10

TABS: Standard tab width = 1792
MARGINS: paragraph margin = 2998,Left margin = 2998, right margin = 20598
UPDOWN: Delta left = 1792, Delta right = 0, Delta paragraph = 0
LEAD: Line leading = 6, Paragraph leading = 12
SCREEN: Screen top = 25, System window end = 90, Screen bottom = 780
OFFSET: Standard offset = 4

[HARDCOPY]
PREFERREDFORMAT: Press
PRESS: Clover
PRINTEDBY: "$"

[CHAT]
BORDER: BLACK
BELL: FLASH

DoradoDisk.cm

```
// <DoradoLogic>DoradoDisk.cm
// Last modified September 17, 1979  6:28 PM  by Taft

FTP Maxc Directory/c Alto Retrieve/c ^
    Sys.errors CallFtp.run InstallSwat.run Chat.run Type.run ^
    Empress.Run Bravo.run Bravo.error Bravo.messages ^
  Directory/c Fonts Retrieve/c Fonts.Widths ^
  Directory/c AltoFonts Retrieve/c Helvetica10.al Helvetica7.al ^
    Gates32.al Template64.al

Copy Ftp.run _ CallFtp.run  //4 page stripped down version of Ftp.run
InstallSwat
Copy SysFont.al _ Helvetica10.al  //use Helvetica so that .wl files print OK
BootFrom sys.boot  //boot here to fix file pointers and SysFont.al core allocation
delete  installswat.run Dumper.Boot DMT.boot CallFtp.run

delete *Disk.cm

//You should now load files from [IVY]<DoradoLogic>DoradoFiles.dm and then run Sil/i.
```

DoradoDict.Analyze

```
; This is a custom dictionary for the Dorado
; Last edited by R. Bates July 23, 1979
get = ECLDict.Analyze
TEMP=LM3911+20K/16/J;                   Temperature sensor - LM3911 plus 20K in pin 6
SPARE=SpareSocket/16/J;                 Empty chip locations for multiwire
N128=SN74128/14/N;                      Should go away when released in TtlDict.analyze
MC107=MC10107/16/E;                     adds pin 6 for MemC - Lampson
MC124=MC10124/16/ETC;                   standard MC124 with extra sections for drawings
MC125=MC10125/16/ETC;                   standard MC125 with extra sections for drawings
MosRam=MosRam/16/J;                     section for drawing explicit pwr and GND
DS3679=DS3679/16/N;                     memory driver with series resistor and 2 disables
8T98=8T98/16/N;                         Hex Ttl drivers with enables on 4 & 2 groups
MPQ3303=MPQ3303/14/J;                   quad transistors for BaseBoard
MPQ6002=MPQ6002/14/J;                   quad transistors for BaseBoard
CD4051=CD4051/16/T;                     8 input analoge switch for BaseBoard
MC12040=MC12040/14/E;                   Phase Frequence Detector for BaseBoard
COMP=AUGATCG16/16/J;                    Another macro def for descrete components
8RP-27=B898-3-R27/16/J;                 Beckman Resistor pack - 8 27 ohm resistors
MC318=MC10318/16/J;             Something for Ken!

@
TEMP
a,P1,1 > a,P2,2 > a,P3,3 > a,P4,4 > a,P5,5 > a,P6,6 > a,P7,7 > a,P8,8 > a,P9,9
a,P10,10 > a,P11,11 > a,P12,12 > a,P13,13 > a,P14,14 > a,P15,15 > a,P16,16
b,IN,1 > c,IN,2 > d,IN,3 > e,IN,4 > f,IN,5 > g,IN,6 > h,IN,7 > i,IN,8
j,IN,9 > k,IN,10 > l,IN,11 > m,IN,12 > n,IN,13 > o,IN,14 > p,IN,15 > q,IN,16

@
COMP, 8RP-27
a,P1,1 > a,P2,2 > a,P3,3 > a,P4,4 > a,P5,5 > a,P6,6 > a,P7,7 > a,P8,8 > a,P9,9
a,P10,10 > a,P11,11 > a,P12,12 > a,P13,13 > a,P14,14 > a,P15,15 > a,P16,16
b,--,1 > b,-,16  ;the "--" is hidden under the left of 4  & 5 and bottom of 6
c,--,2 > c,-,15  ;the "-" is hidden under the right of 4  & 5 and top of 6
d,--,3 > d,-,14
e,--,4 > e,-,13
f,--,5 > f,-,12
g,--,6 > g,-,11
h,--,7 > h,-,10
i,--,8 > i,-,9
j,--,9 > j,-,8
k,--,10 > k,-,7
l,--,11 > l,-,6
m,--,12 > m,-,5
n,--,13 > n,-,4
o,--,14 > o,-,3
p,--,15 > p,-,2
q,--,16 > q,-,1
```

```
@

SPARE
a,P1,1 > a,P8,8 > a,P16,16

@
N128
a,IN,2,3 >a,OUT,1 >b,IN,5,6 >b,OUT,4 >c,IN,8,9 >c,OUT,10 >d,IN,11,12 >d,OUT,13

@
MC107
a,IN,4,5 > a,OUT,2 > a,o,3
b,IN,7,9 > b,OUT,11 > b,o,10
c,IN,14,15 > c,OUT,12 > c,o,13
d,IN,6

@
MC124
a,IN,5 > a,c,6 > a,OUT,4 > a,o,2 > a,x,9
b,IN,7 > b,OUT,3 > b,o,1
c,IN,10 > c,OUT,12 > c,o,15
d,IN,11 > d,OUT,13 > d,o,14
e,IN,5 > e,OUT,4 > e,o,2
f,IN,6

@
MC125
a,IN,3 > a,c,2 > a,OUT,4 > a,v,1 > a,x,9
b,IN,7 > b,c,6 > b,OUT,5
c,IN,11 > c,c,10 > c,OUT,12
d,IN,15 > d,c,14 > d,OUT,13
e,IN,3 > e,c,2 > e,OUT,4
f,IN,1

@
MosRam
a,A0,1> a,A1,9> a,A2,5> a,A3,7> a,A4,6> a,A5,12> a,A6,11> a,A7,10
a,A8,13> a,RAS',4> a,CAS',15> a,WE',3> a,V+,8> a,GRND,16
b,IN,2 > b,OUT,14
c,A0,1> c,A1,9> c,A2,5> c,A3,7> c,A4,6> c,A5,12> c,A6,11> c,A7,10
c,A8,13> c,RAS',4> c,CAS',15> c,WE',3> c,V+,8> c,GRND,16

@
DS3679
a,IN,2 > a,OUT,3
b,IN,4 > b,OUT,5
c,IN,6 > c,OUT,7
d,IN,10 > d,OUT,9
e,IN,12 > e,OUT,11
f,IN,14 > f,OUT,13
```

g,EN',1,15

@
8T98
a,IN,2 >a,OUT,3 >b,IN,4 >b,OUT,5 >c,IN,6 >c,OUT,7 >d,IN,10 >d,OUT,9
e,IN,12 >e,OUT,11 >f,IN,14 >f,OUT,13 >g,En4',1 >g,En2',15

@
MPQ3303, MPQ6002
a,IN,2 > a,OUT,1 > a,e,3
b,IN,6 > b,OUT,7 > b,e,5
c,IN,9 > c,OUT,8 > c,e,10
d,IN,13 > d,OUT,14 > d,e,12

@
CD4051
a,A,11 > a,B,10 > a,C,9
a,Ch7,4 > a,Ch6,2 > a,Ch5,5 > a,Ch4,1 > a,Ch3,12 > a,Ch2,15 > a,Ch1,14 > a,Ch0,13
a,INH,6 > a,V-,7
a,OUT,3

@
MC12040
a,R,6 > a,V,9
a,U,4 > a,U',3 > a,D,12 > a,D',11

@
MC318
a,D0,8 > a,D1,7 > a,D2,6 > a,D3,5 > a,D4,4 > a,D5,3 > a,D6,2 > a,D7,1 >
a,Comp,11 > a,Ref+,12 > a,Ref-,10
a,Out+,14 > a,Out-,15
a,V-,9 > a,GRND,16