***** Preliminary Draft *****

Dandelion Hardware Manual

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Dandelion Hardware Manual

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1.0 Overview

This manual describes the Dandelion (Series 8000 Processor) hardware. There are no page-by-page descriptions of schematic diagrams nor listings of PROMS and microcode. This manual should help the microcoder understand the hardware and help the trouble-shooter understand the schematics. It may also be used to get a general understanding of the machine.

This introductory chapter looks at the major characteristics of each controller and processor in the system. The logical boundaries of the Dandelion are shown in Figure 1. There are two main processors: the Central Processor (CP) and the Input/Output Processor (IOP). The CP controls the high bandwidth peripheral devices and emulates the target language (e.g., Mesa). It is a high performance, microprogrammable processor which has been optimized for cost. The IOP, on the other hand, supervises the lower-speed devices, such as the mouse and keyboard, and controls the booting process. It is also used as a base to run diagnostics. It employs a traditional microprocessor (8085) in an 8-bit bus architecture. To the CP, the IOP appears as another high bandwidth I/O device.

Central Processor

The CP executes microcode to control device controllers and main memory. Only the CP can access main memory. When devices request CP cycles (they get three per request), they can read or write one memory location. The processor, together with the memory, are time-division multiplexed among the device controllers in a round-robin fashion. The idea is that the (expensive) high-speed processor is shared among the (inexpensive) controllers. The controllers can be made very small because the round-robin nature of the memory access mechanism *guarantees* maximum memory latencies compatible with the controller bandwidths (unlike general bus architectures).

Time is divided up into *rounds*, where a single round consists of five slots, called *clicks*. Each click is preallocated to one (or more) of the device controllers. If a controller desires CP service or wants to transfer a word to or from memory, it raises its wakeup request and the CP will schedule the controller's microcode *task* for the next click in the round allocated to the device. If a controller does not desire any service, the click is allocated to the language Emulator instead. It can be seen that the CP hardware must preserve the microprogram counters for each of the controller's tasks.

Clicks are further divided into three *cycles*: exactly one microinstruction is executed in each cycle. Memory requests must always be started in the first cycle (`c1`) of a click, thereby guaranteeing the memory's latency for the controllers (and eliminating the need for more interclick state). A cycle is 137 nanoseconds in duration, thereby setting the memory access time at 411 nanoseconds (39 Mbits/sec). The simplest and most frequently executed Emulator instructions complete in one click (411 nS).

The CP executes microinstructions from a 4K-by-48-bit, writeable control store. The heart of the ALU is implemented with a high-speed 2901 bit-slice processor. There is an auxiliary register file of 256 words and a device used to rotate words 4, 8, or 12 bits. Every 48-bit microinstruction contains the 12-bit address of the next instruction. Branching and dispatching are accomplished by *or*ing condition bits into the "next address" field.

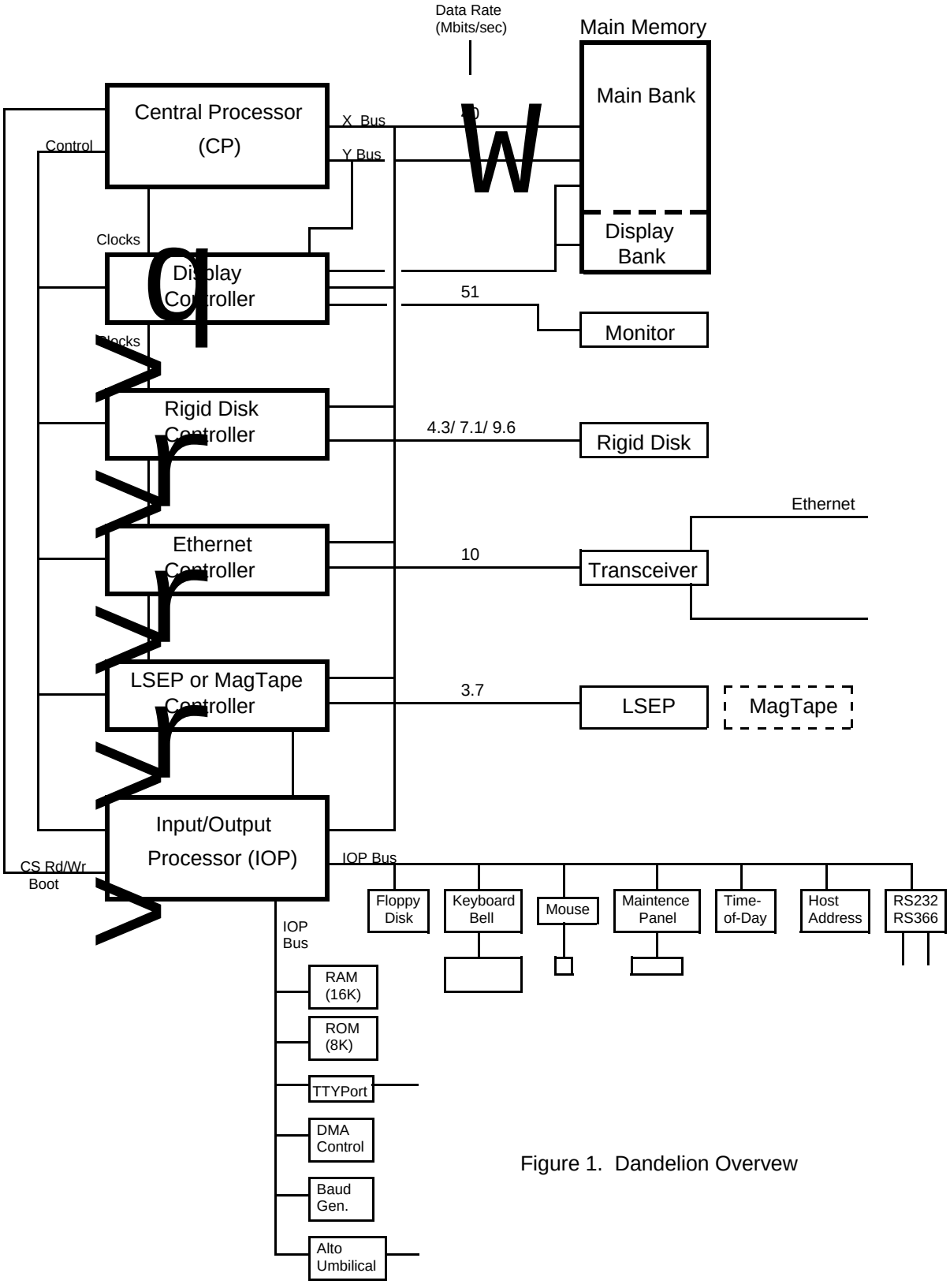


Figure 1. Dandelion Overvew

Main Memory

The Dandelion memory system is composed of two cards: the control card (MCC) and the storage card (MSC). They each come in two versions; one using 16K chips, the other using 64K chips. The versions of the cards using 64K chips are called MCC-X and MSC-X. Thus, the total memory size can vary from 64K to 768K words. The maximum size of real memory is 1024K words (20-bit real address).

The memory system has some hardware support for virtual addresses. The mapping between real and virtual page numbers is stored in a linear array (the Map) located in the real address space. The maximum size of the Map is 16K words for the MCC (22-bit virtual addresses) and 64K words for the MCC-X (24-bit virtual addresses). Smaller virtual addresses spaces can be used, reclaiming real memory space.

The memory system is logically divided into the display bank and the main bank. The display bank is the lowest 64K of memory and has two ports: one for the display controller and one for the CP. When the display is actually on and displaying bits, accesses to the display bank from the CP are reduced by 47%.

The memory is single-bit corrected and double-bit error detected. A double-bit error encountered in the Emulator causes the Emulator microcode to trap. Double-bit errors caused by I/O task microcode are recorded but cause no traps. The display controller runs the display bank at a faster rate than the CP and receives uncorrected data.

Display and Clocks

The display controller reads words from a 51K-word bitmap in the memory display bank and produces video and synch signals for the 17" monitor. The screen has an active image of 808 lines by 1024 bits. A frame (an even followed by an odd field) is repainted 38.7 times a second. The bit rate to the monitor is 51MHz (19.6 nS). The phosphor is P40 white, with a long decay time (used in the Alto).

The controller can divide each scan line into up to seven segments. The bits shown in each segment may come from a different line in memory. Thus, windows can be scrolled vertically without having to move the bits of the window in memory. The cursor is implemented in the microcode as a 16-by-16 window (although it can be any size). In every frame, the microcode *or*s the cursor with the appropriate words in the active region, these words are written into a temporary area (in the display bank), and then this temporary area is used as the cursor window.

A total of 54 lines of top and bottom border are displayed. Each line consists of a repeated pattern generated from the controller border pattern register which can be loaded from software. There are also 32 bits of border on each end of every visible line. The display controller hardware orchestrates the horizontal line events, while the display microcode decides when the line state should change.

The display microcode also has the task of refreshing main memory. Two refresh pulses are required for each 28.8 msec scan line with the normal controller communications. Furthermore, it maintains a 32-bit counter, incremented once per scan line, which can be used by the Emulator to measure short-duration events. The display microcode can also wake up an Emulator process at an arbitrary scan line in every field.

The CP's clocks are derived from the display clock: the display's bit period of 19.59 nS is multiplied by seven to give the CP's cycle time of 137.14 nS. There are exactly 14 rounds per horizontal display scan line.

IOP

The Input/Output Processor (IOP) is an 8085 based processor which services the low speed I/O devices, can boot the CP, and read or write its microstore and task program counters. It is also a convenient place from which to exercise the CP and the high speed devices (e.g., floppy disk diagnostic programs).

The IOP supports the following low speed devices: (1) IBM-compatible floppy disk with both single and double density and double sided diskettes; (2) Star Level 4 Keyboard interface, mouse interface, and simple tone generator to drive the speaker in the keyboard; (3) TTY port interface (RS232C DCE) to connect a Lear Siegler terminal or Diablo 630 character printer; (4) the maintenance panel (4-digit 7-segment display plus 2 boot buttons); (5) the time-of-day clock; (6) the CP control store and task program counters; (7) the CP-IOP communication port; (8) the Alto umbilical debugging connection; and (9) the Ethernet host address PROM. In addition, located on the Option card, the IOP supports (10) the LSEP UART and baud-rate generator and (11) a Z80-SIO with RS232C and RS366 interfaces. The 48-bit Ethernet host address is located in a prom on the IOP.

The IOP has 16K bytes of RAM and four, socketed EPROMS for 8K bytes of read-only memory. The EPROM contains some simple 8085 diagnostics, the basic IOP boot supervisor, and some initial CP boot microcode for the various sources of boot files (rigid or floppy disk or Ethernet).

The IOP communicates with the CP via the CP-IOP port. This is a normal set of input/output registers in the CP's I/O system. IOP task microcode can read or write main memory with arguments supplied by the IOP through the port. The IOP can supply or accept data in a polled fashion or with DMA (one byte per 4 microseconds).

The 32-bit time-of-day clock counts seconds based on the 60 Hz power line. The clock continues to run when the Dandelion is turned off but is still plugged into the wall. This feature is disabled on current hardware.

Rigid Disks

The HSIO board can operate either a Shugart SA1000 or a SA4000 drive, but not both and not multiple drives. The two controllers share some common circuitry; a wire in the interface cable distinguishes between the two types of drives. The SA1000 requires and expects phase encoded data, whereas the SA4000 does not. Another version of the HSIO card, the HSIO-L, can support up to 4 Trident T-300 or T-80 drives.

The following table summarizes the formatted capacity, average access time, and bit rates of the three types of drives:

drive	capacity (Mbytes)	avg access (msec)	bit rate (MHz)
SA1004	8.38	80	4.27
SA4008	23.17	75	7.14
T-300	237.8	30	9.6

The SA1000 clock rate (234 nS/bit) is derived by dividing the display rate (51 MHz) by 12.

Ethernet

The Ethernet controller contains: a phase encoder (based on a 20MHz crystal), a phase decoder (Phase Lock Loop), serial-to-parallel and parallel-to-serial converters, a 16-word FIFO buffer, a 9.6-msec counter, a 51.2-msec interval counter, and a state machine to manage the buffer among incoming and outgoing packets. The Ethernet task requires two clicks per round because of the high data rate: 1.6 msecs per word. Moreover, the FIFO is required because of the software queue overhead and the microcode overhead required to check the destination-address field of incoming packets.

There is a single FIFO and CRC generator/checker shared between input and output. The controller hardware and microcode, to the extent possible, operate this half-duplex buffer so as not to lose packets an incoming packet has priority over a packet being staged for transmission. The FIFO can hold more than one received packet. There is a "end-of-packet" marker maintained in the buffer.

The microcode appends packets to an input queue maintained by the Emulator in main memory. Similarly, it reads from an output queue set up by software. The microcode generates the retransmission interval when there is a collision (it uses the 51.2-msec controller wakeup when deferring).

The controller has a special mode (which also requires special microcode) which will loopback a 15-word packet. The packet can be sent either through the transceiver or only through the phase encoder and decoder, thereby bypassing the transceiver and drop cable. In loopback mode, the CRC checker is also verified with a microcode-supplied checksum.

LSEP

The Low-Speed Electronic Printer (laser ROS or thermal) controller has two parts on the Options card: a one-word "video" buffer, which is an I/O device controlled by the CP, and an IOP-controlled UART which is used to send and receive commands and status.

The buffer is a simple two-word, ping-pong arrangement: one shift register is loaded while the other is supplying data to the printer. The Raven microcode reads words from the display bank and then zeros them (all in one click) in order to prepare for the next page. The "video" clock is supplied by the printer. The speed of the command/status UART is set by an IOP controlled baud-rate generator.

The one click per round used by the LSEP is also shared with the special Refresh task needed when the display is off.

MagTape

(to be added)

Configuration

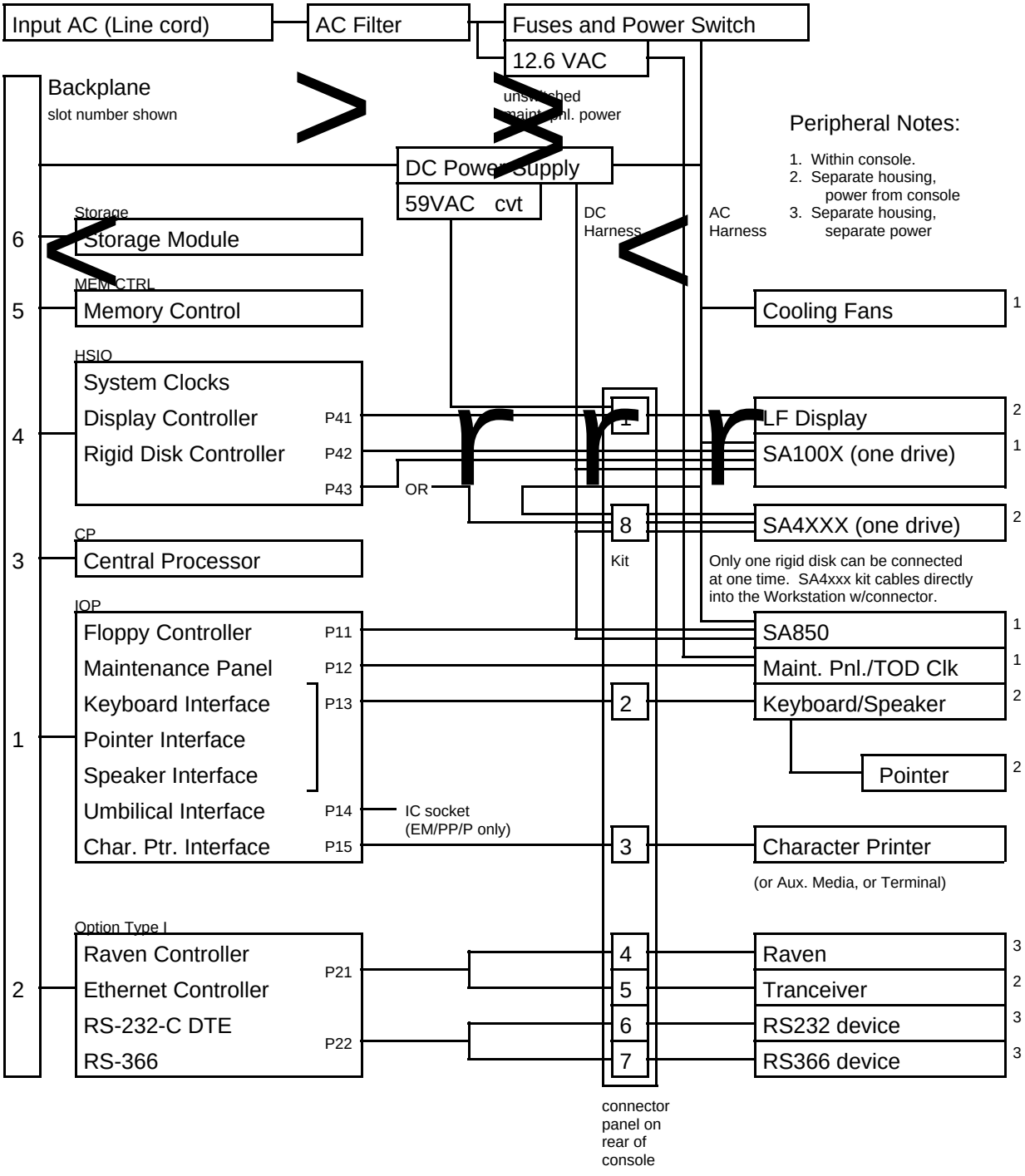
The figure on the next page shows the baseline configuration of the Dandelion using Shugart drives. The cards measure 11x14 inches. No remote power up or down is included. There is a mechanical, rocker-type, power switch on the front of the console under a cover.

Two momentary contact pushbuttons are included with a 4 digit maintenance panel under the cover with the power switch at the front of the machine. One of the buttons (boot) is hardwired to the 8085's reset line. If you push boot, the 8085 will boot the machine in the default way. If the second button (alternate boot) is held down while boot is pushed, the 8085 will slowly display a sequence of numbers in the maintenance panel which refer to alternate booting strategies. When the user releases the AltBoot button the selected strategy will take place. The strategies include booting from rigid disk, booting from floppy disk, from the Ethernet, and diagnostic boots. Note that when the power is turned on, the standard boot takes place without the need to push any buttons.

Whereas the SA1000 drive fits inside of the main cabinet, the SA4000 requires a separate housing. If power is lost in the middle of writing a disk page, the page will be lost.

Workstation Configuration

Base Line Workstation



Connector Panel Notes:

1 D Series 25 Pin Socket
2 D Series 50 Pin Socket
3 D Series 25 Pin Socket
4 D Series 25 Pin Plug
5 D Series 25 Pin Socket
6 D Series 25 Pin Socket
7 D Series 25 Pin Socket
8 Kit