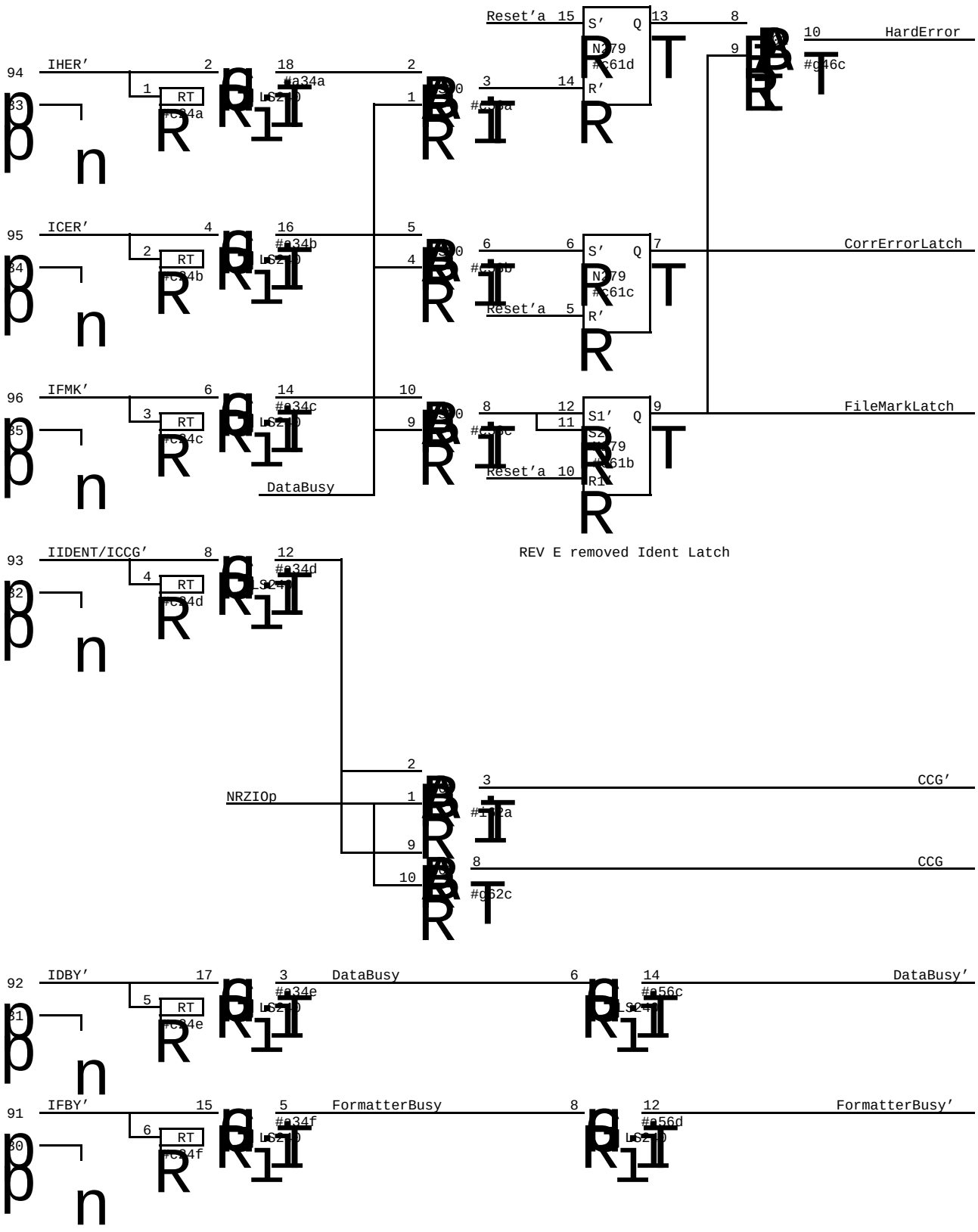
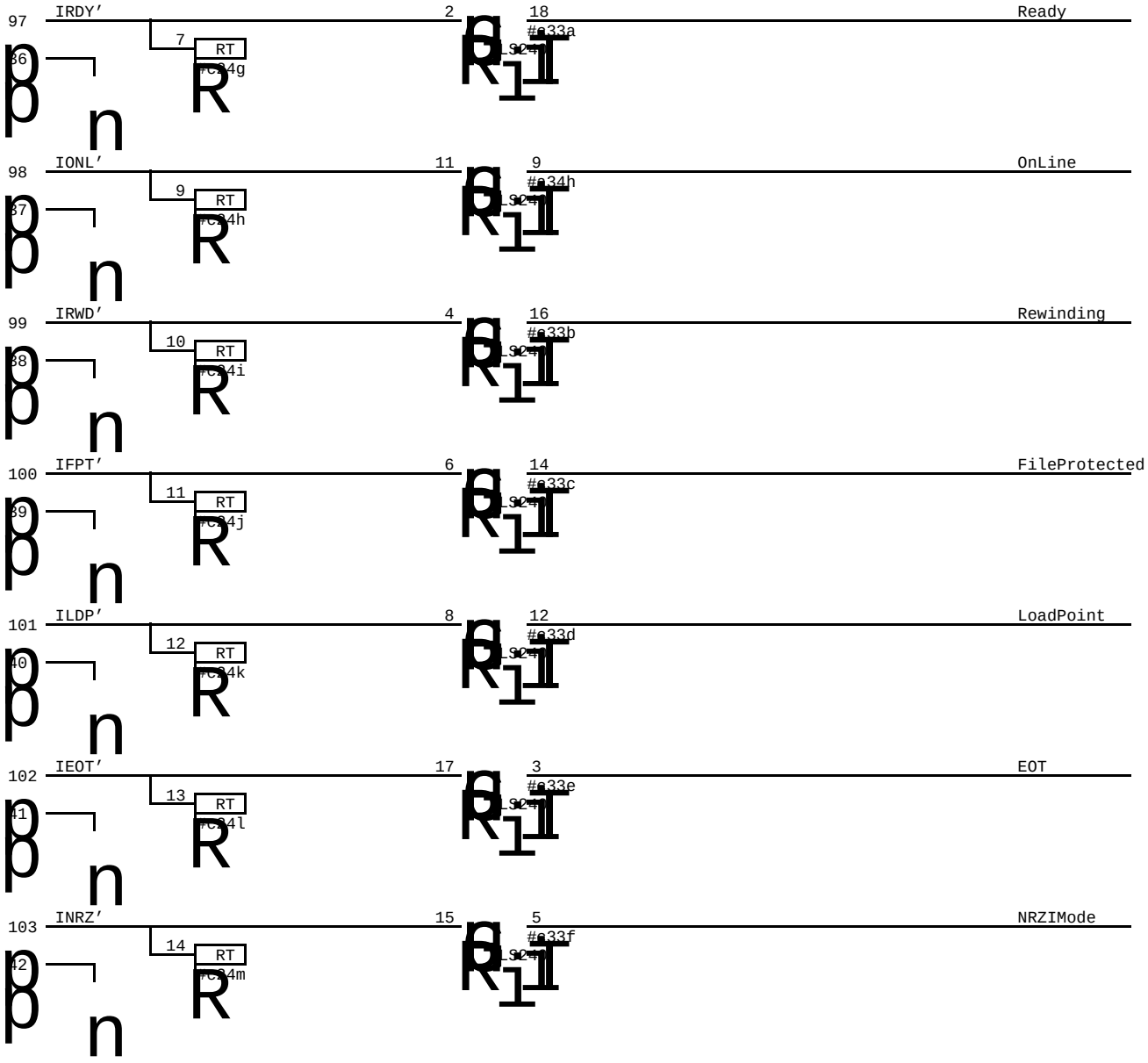
ALTO DUAL DENSITY TAPE CONTROLLER

DDTape

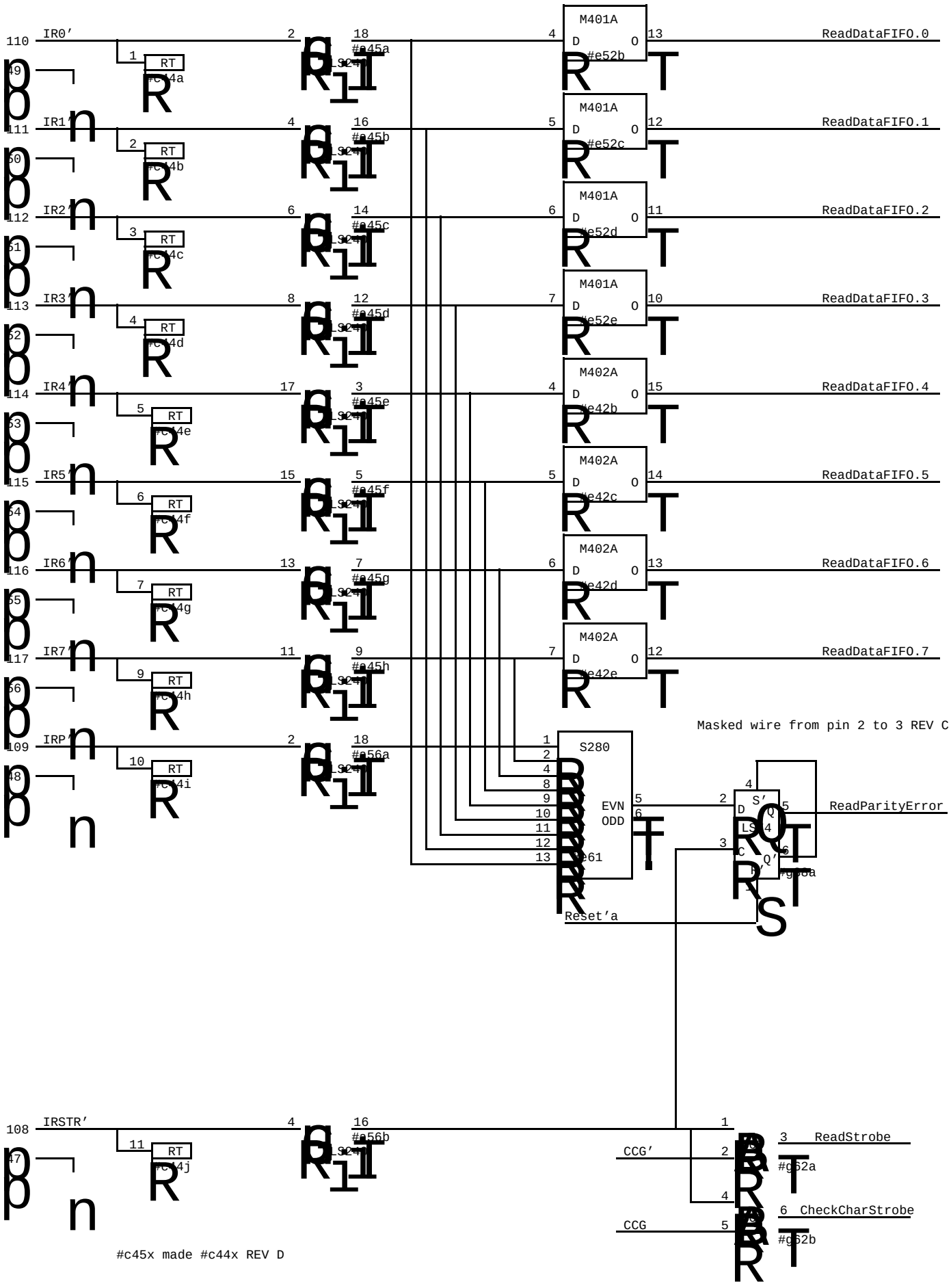
Table of contents



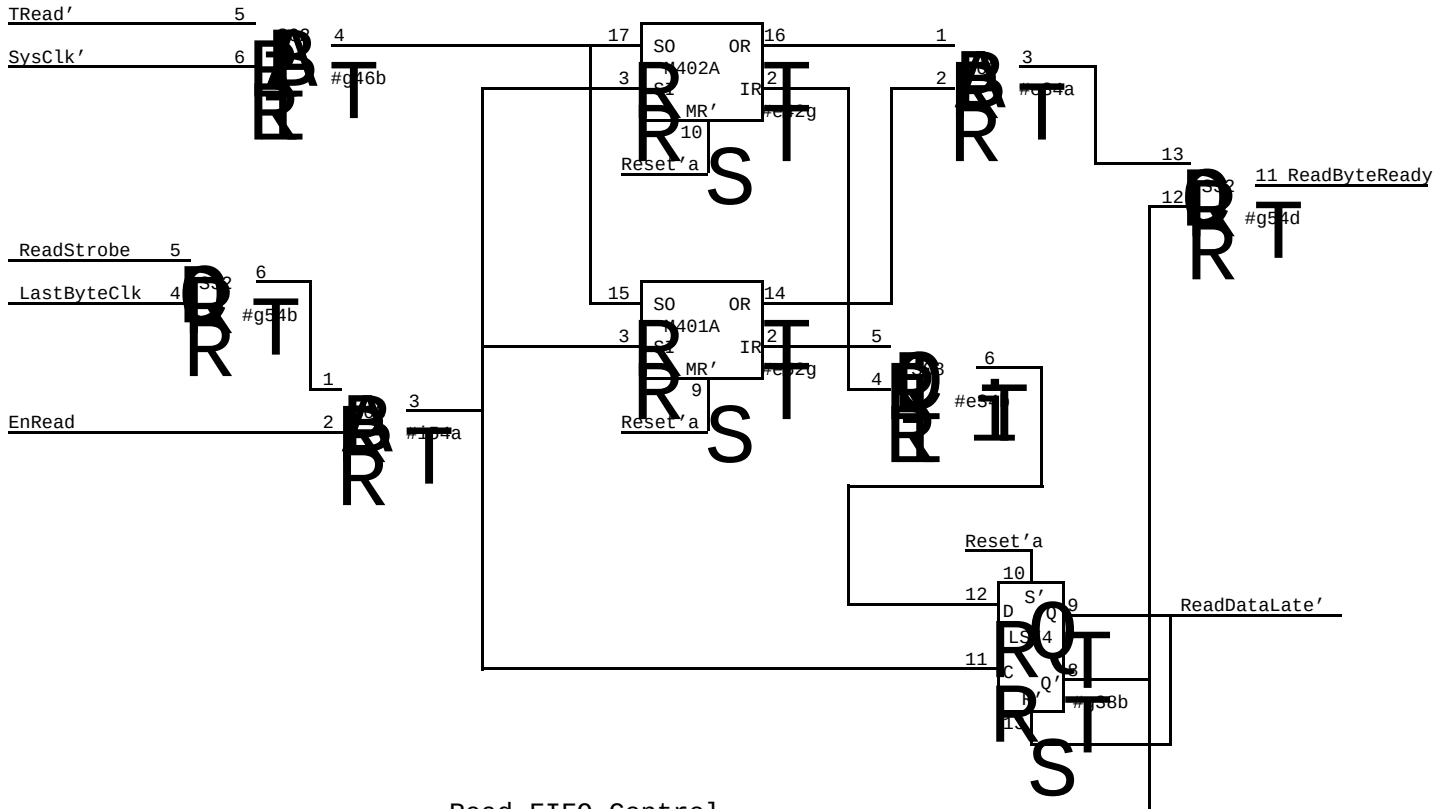
XEROX PARC/CSL	Project		File	Designer	Rev	Date	Page
	DDTape	Tape Formatter Status Interface	DDTape01.sil	Tim Diebert	E	3/17/81	02



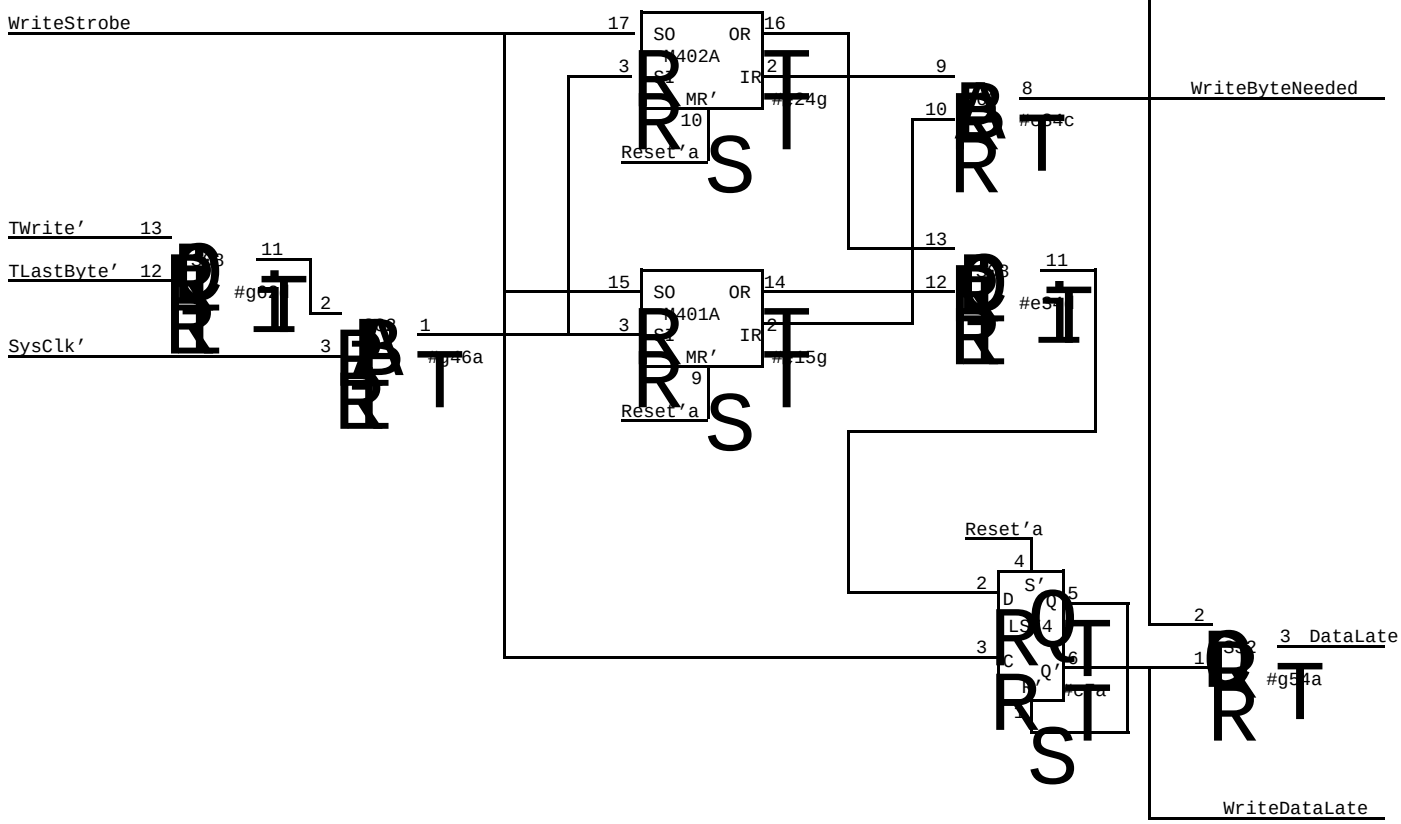
XEROX PARC/CSL	Project DD Tape	Tape Unit Status Interface	File DDTape02.sil	Designer Tim Diebert	Rev E	Date 12/18/80	Page 03



XEROX PARC/CSL	Project DD Tape	Read Data Recievers and Read FIFO	File DDTape03.sil	Designer Tim Diebert	Rev E	Date 2/12/81	Page 04

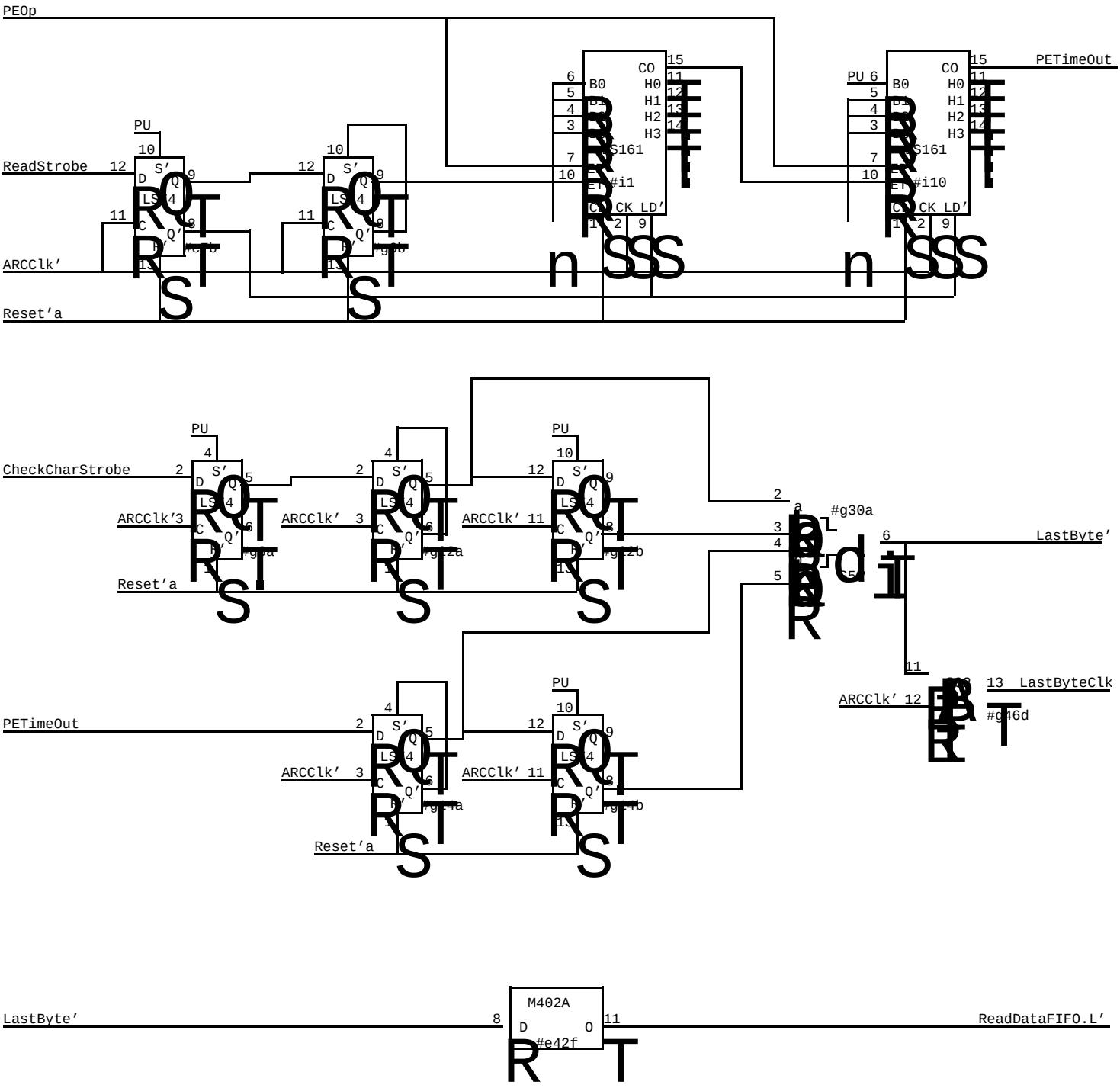


Read FIFO Control

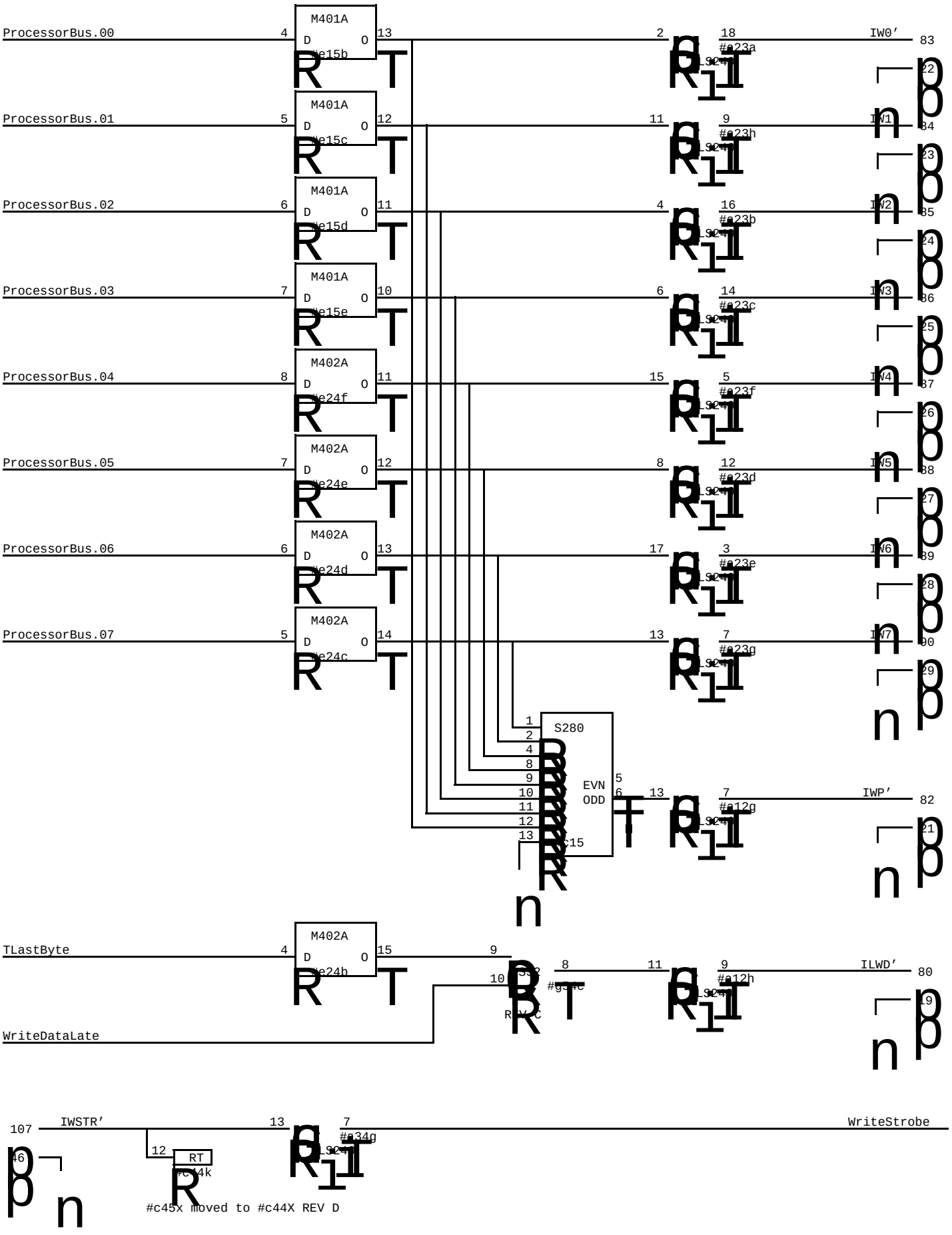


Write FIFO Control

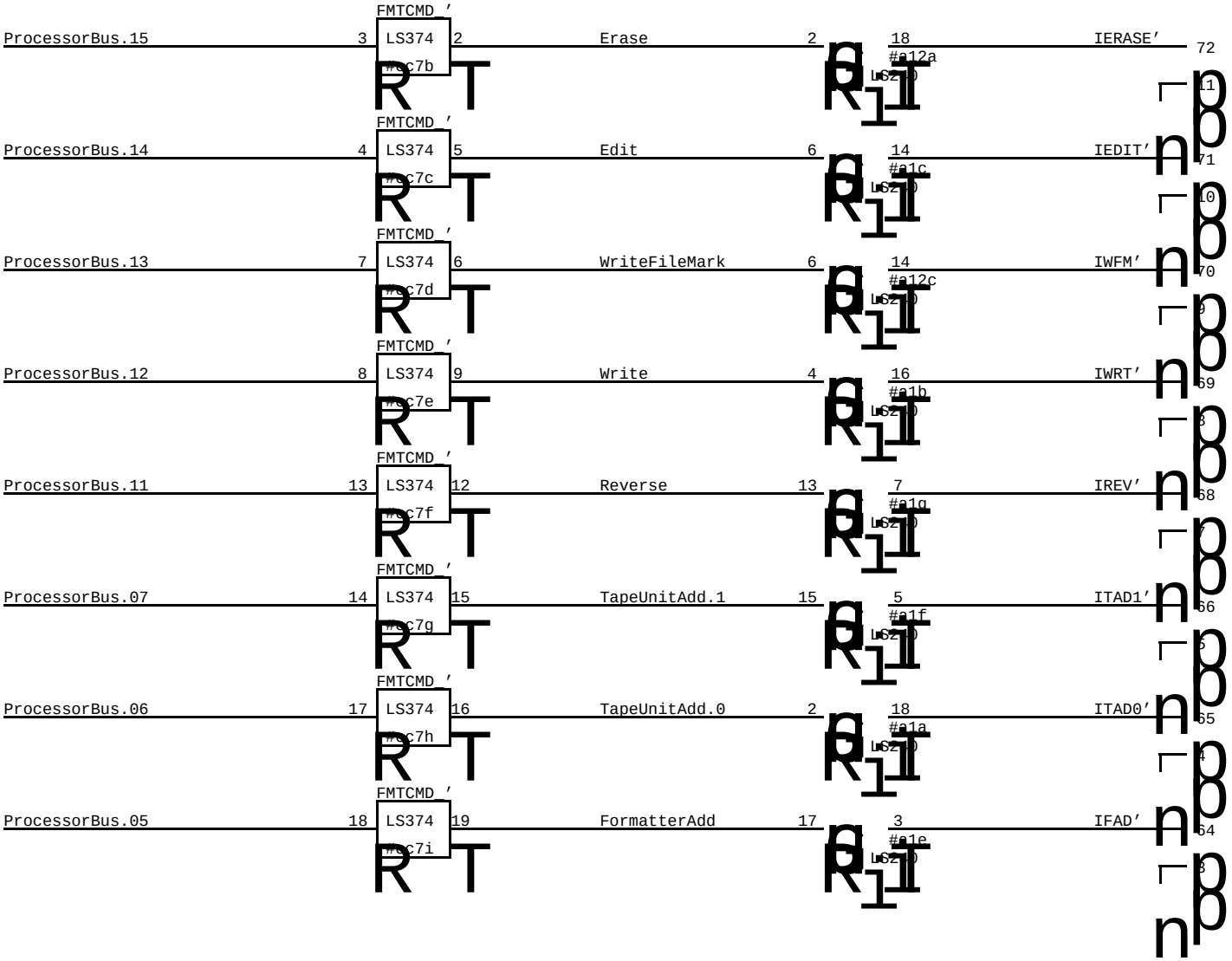
XEROX PARC/CSL	Project DD Tape	FIFO Control	File DDTape04.sil	Designer Tim Diebert	Rev E	Date 3/17/81	Page 05

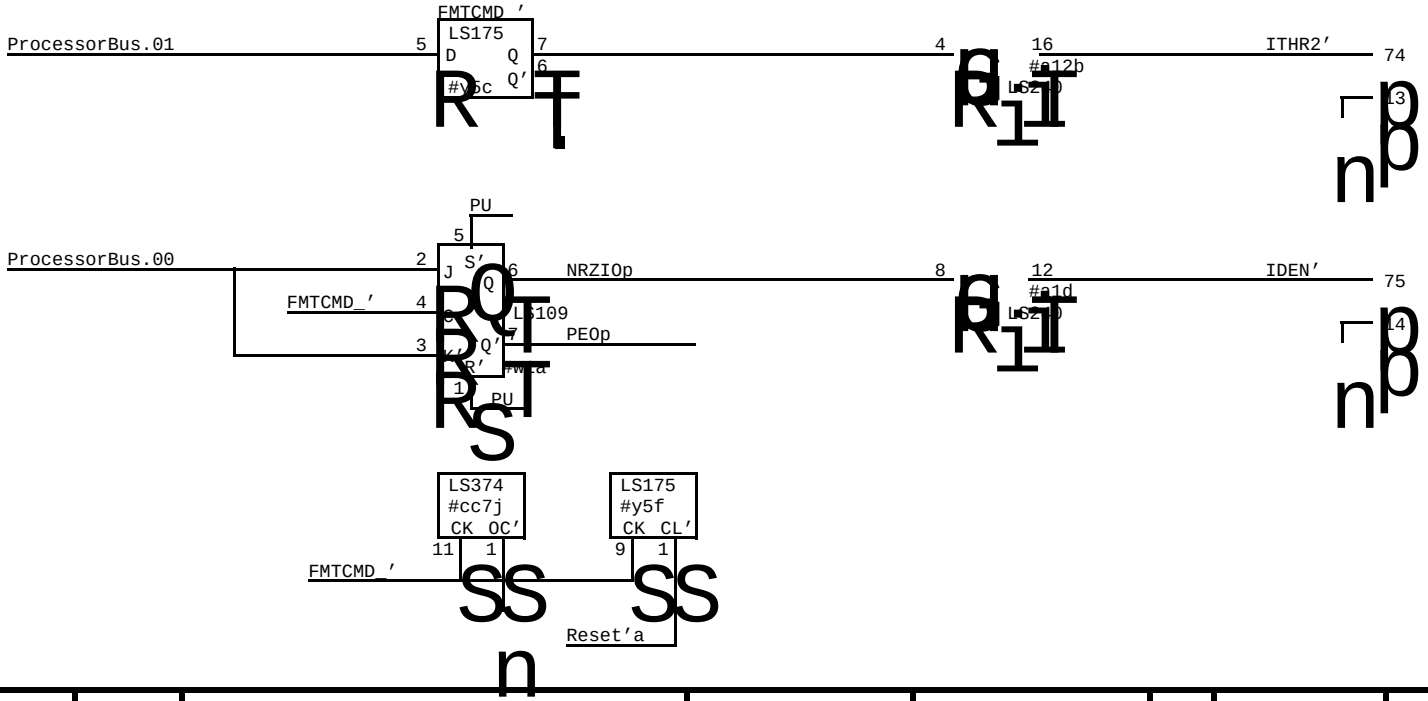


XEROX PARC/CSL	Project DD Tape	Last Byte Detect	File DDTape05.sil	Designer Tim Diebert	Rev E	Date 12/09/80	Page 06

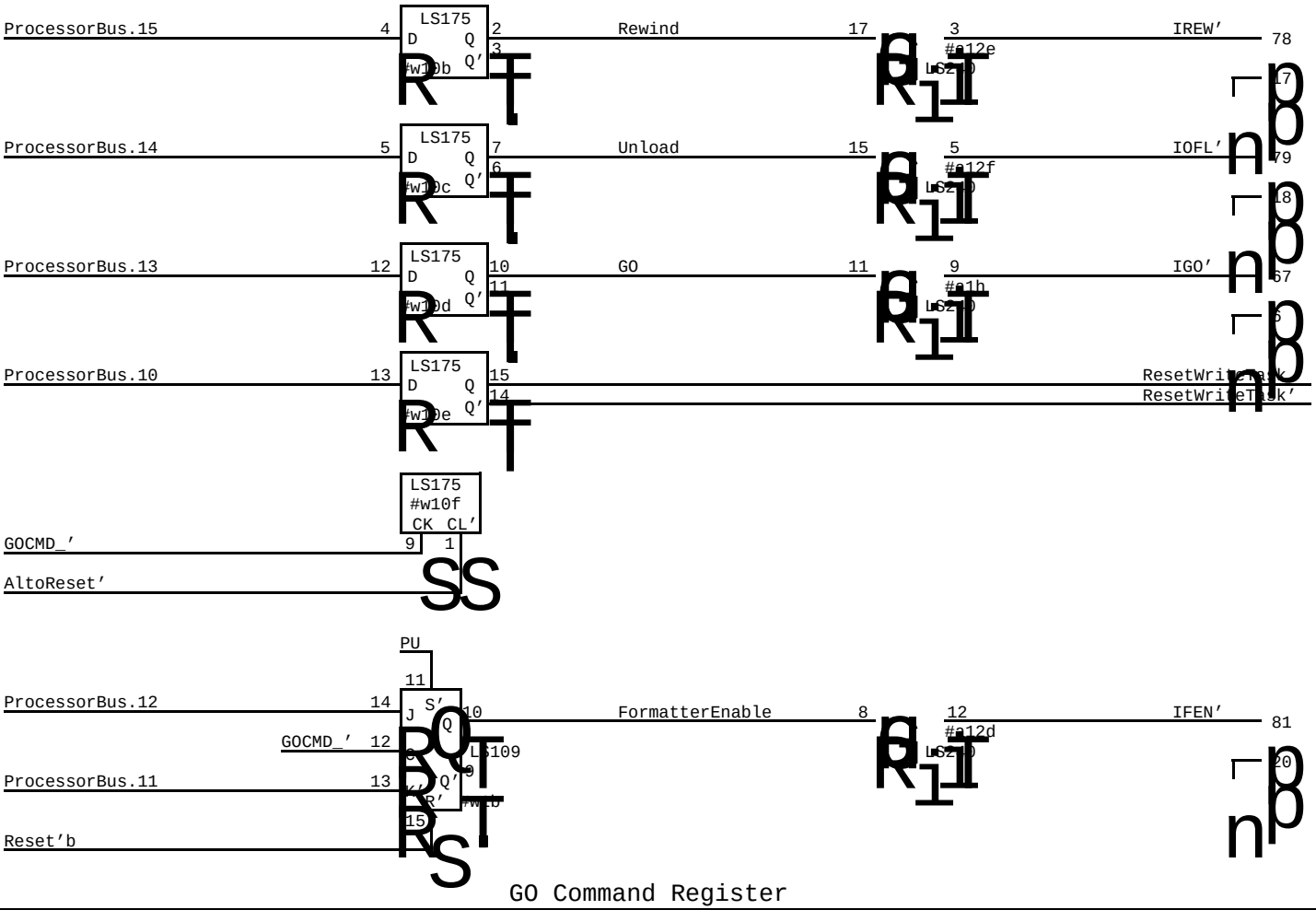


XEROX PARC/CSL	Project DD Tape	Write FIFO and Output Drivers	File DDTape06.sil	Designer Tim Diebert	Rev E	Date 2/12/81	Page 07

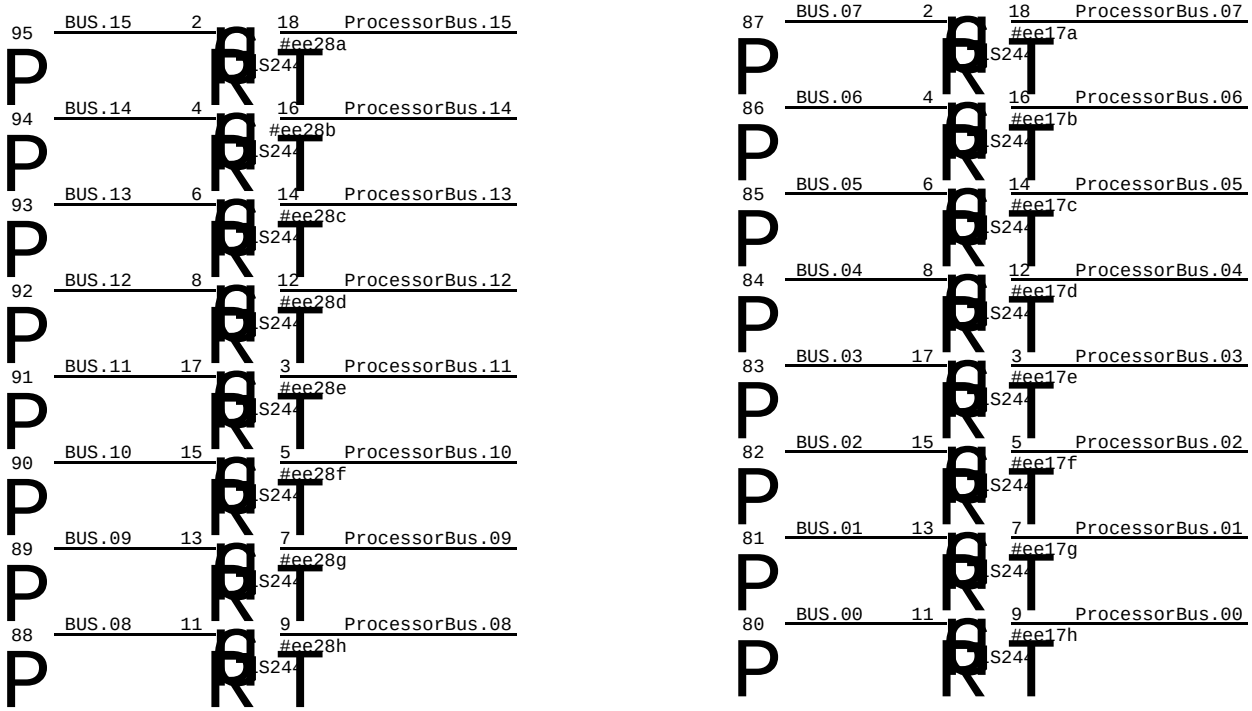




XEROX PARC/CSL	Project DDTape	Formatter Command Register	File DDTape07.sil	Designer Tim Diebert	Rev E	Date 3/17/81	Page 08

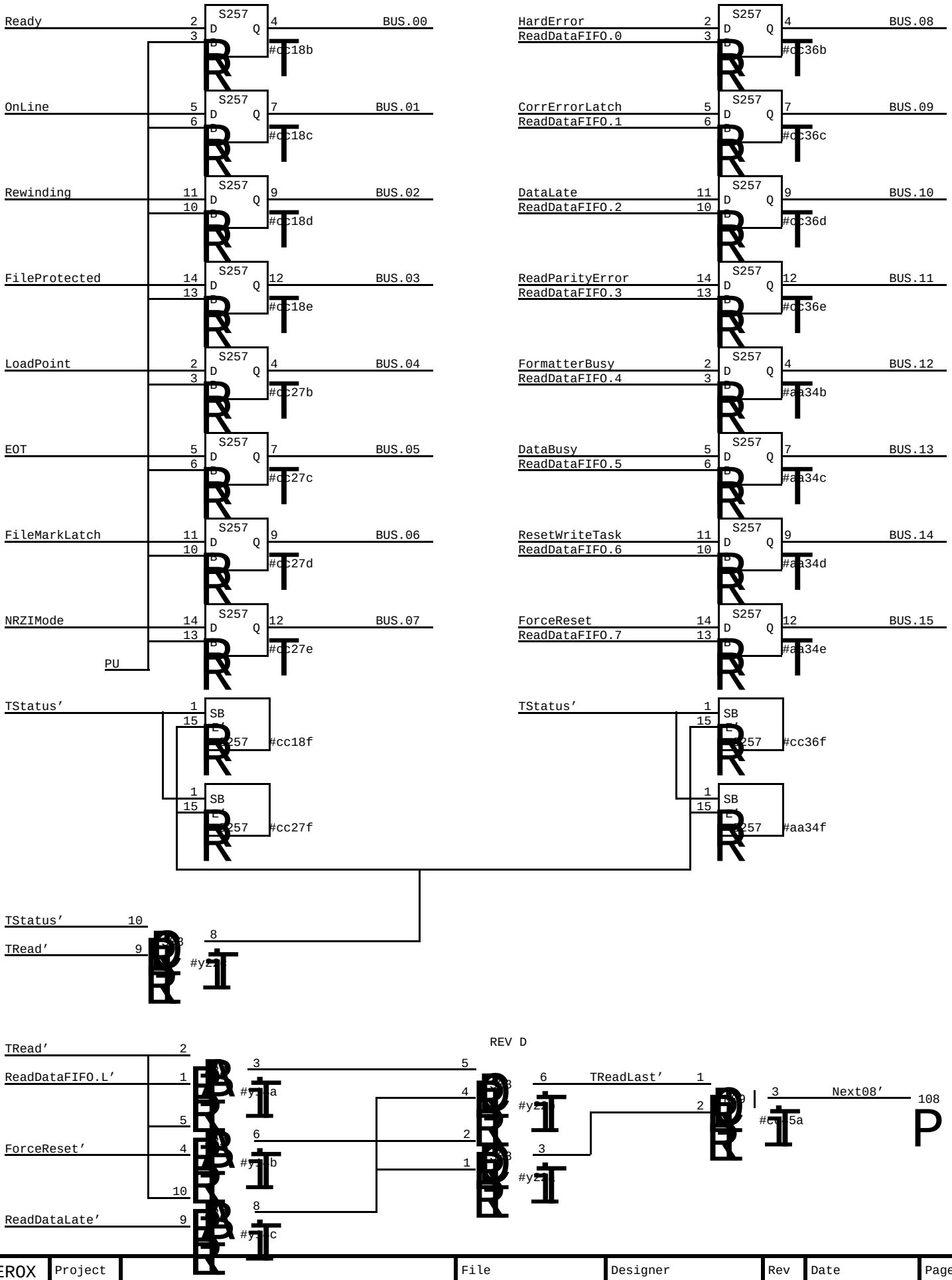


GO Command Register

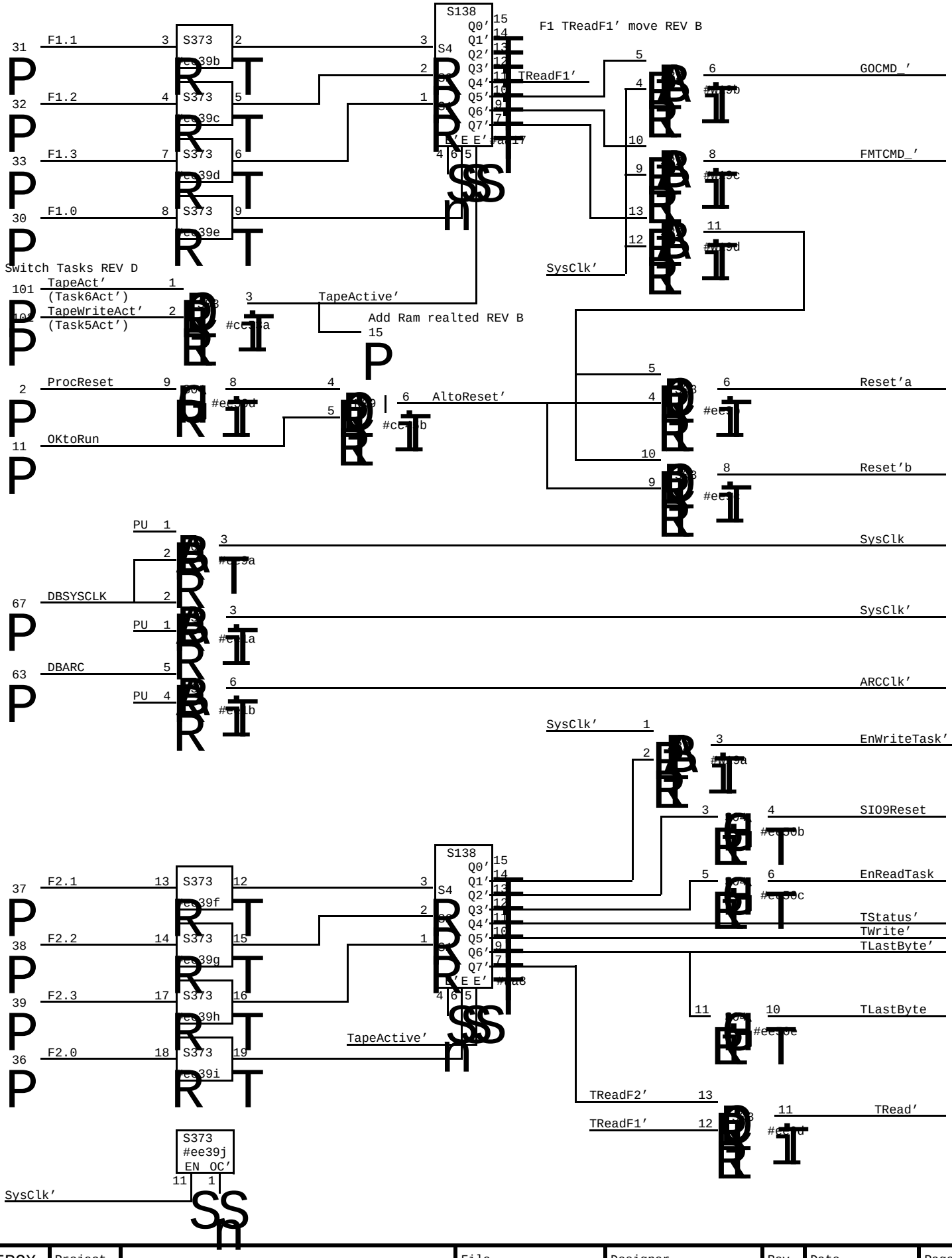


Alto Bus Interface

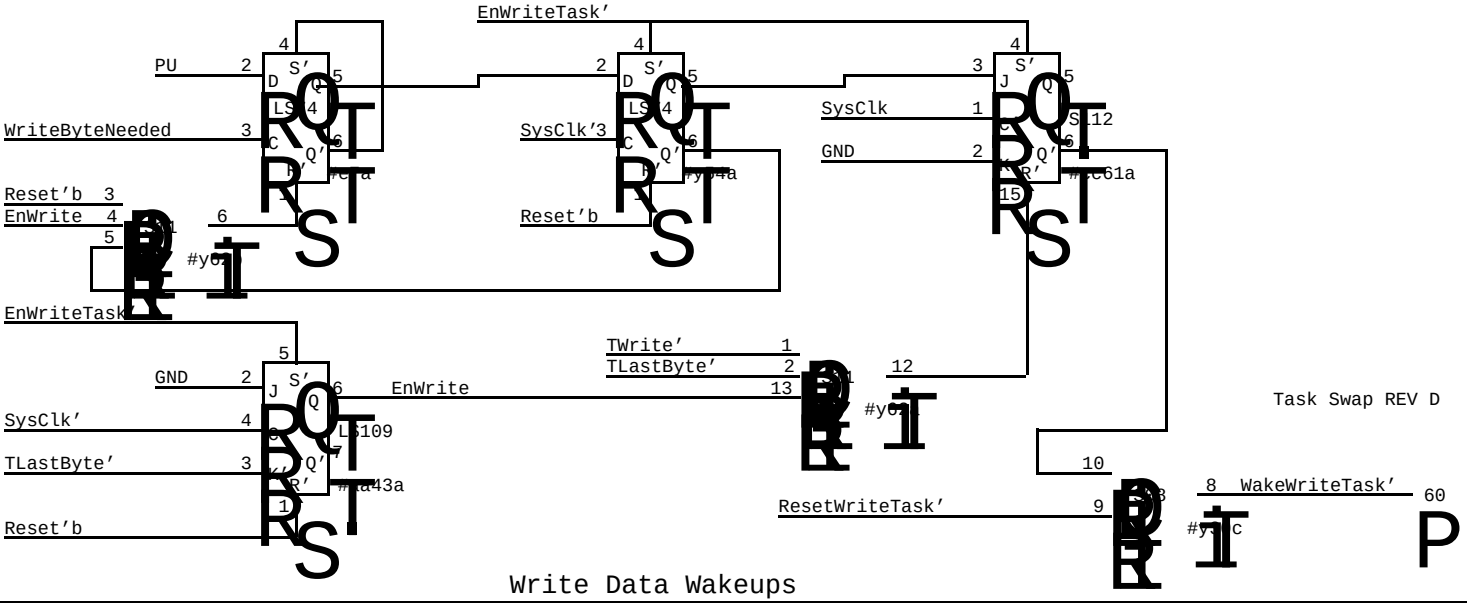
XEROX PARC/CSL	Project DDTape	GO Command Register Alto Bus Interface	File DDTape08.sil	Designer Tim Diebert	Rev E	Date 3/17/81	Page 09



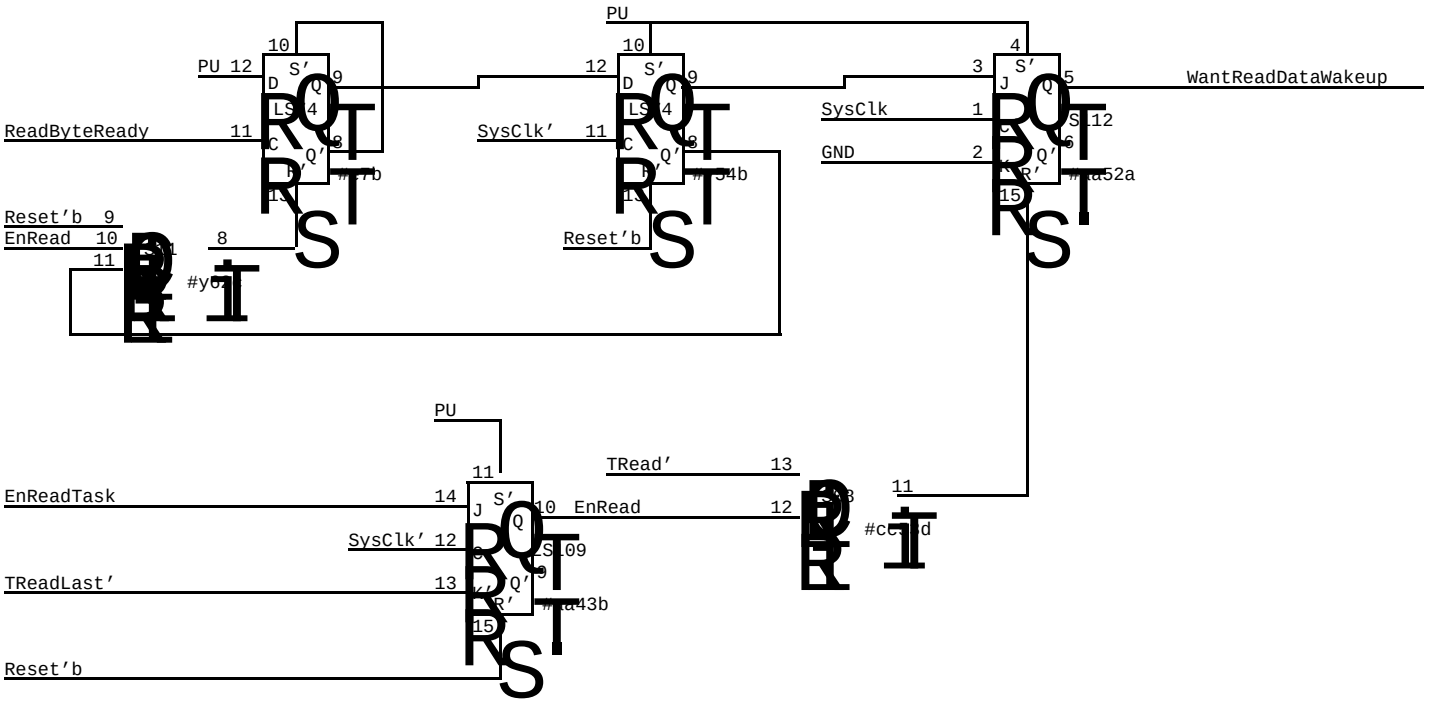
XEROX PARC/CSL	Project		File	Designer	Rev	Date	Page
	DDTape	Alto Input Bus Multiplexors	DDTape09.sil	Tim Diebert	E	3/17/81	10



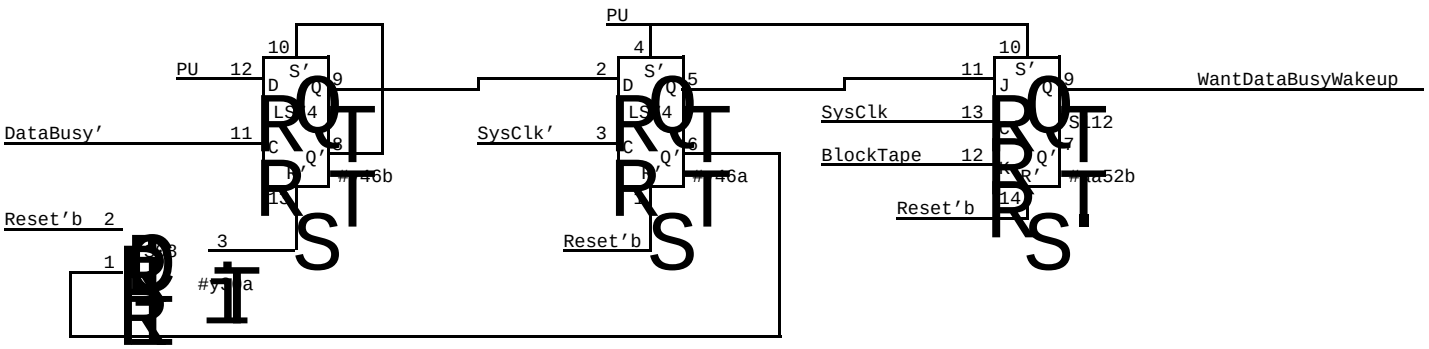
XEROX PARC/CSL	Project		File	Designer	Rev	Date	Page
	DDTape	Alto Processor Interface	DDTape10.sil	Tim Diebert	E	2/12/81	11



Write Data Wakeups

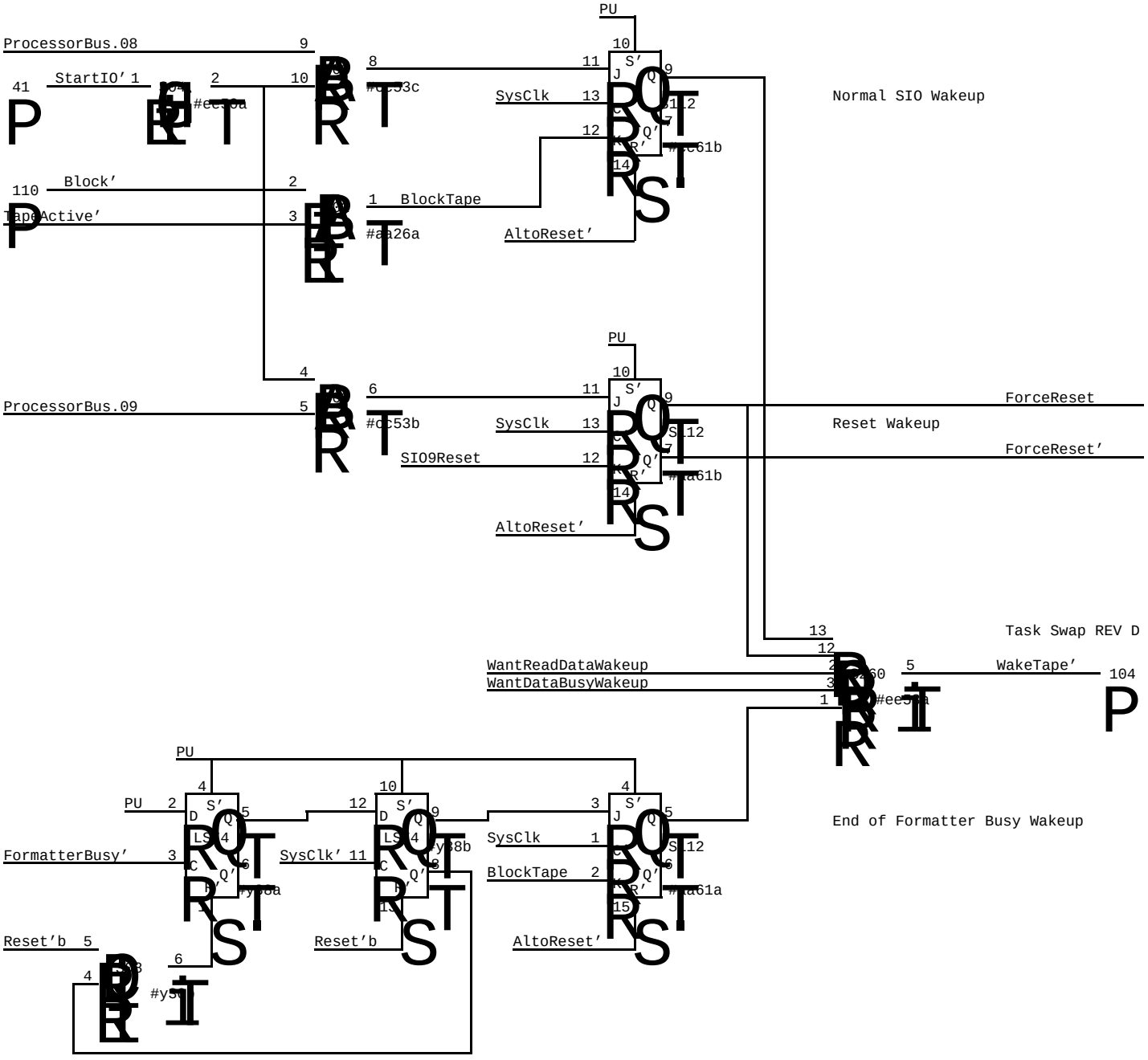


ReadDataWakeups

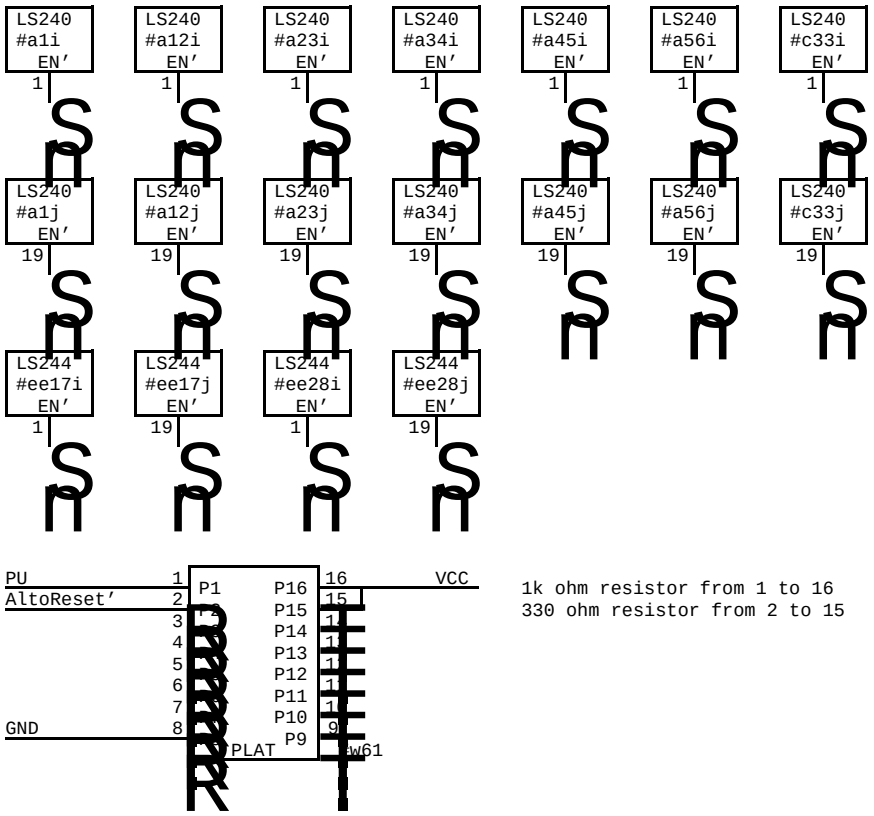


End of Data Busy Wakeup

XEROX PARC/CSL	Project DDTape	Data Wakeups	File DDTape11.sil	Designer Tim Diebert	Rev E	Date 3/17/81	Page 12



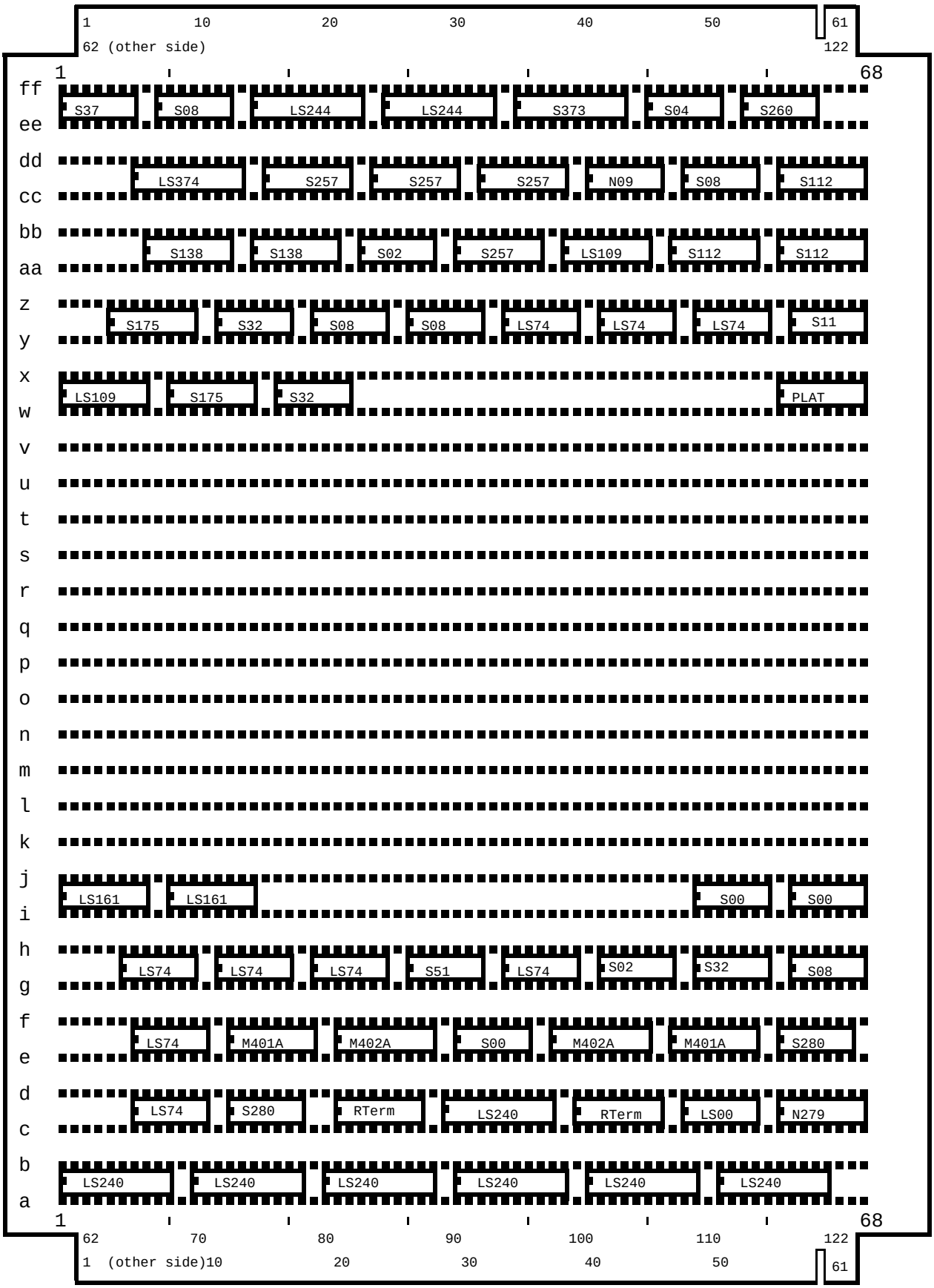
XEROX PARC/CSL	Project DDTape	Other Wakeups	File DDTape12.sil	Designer Tim Diebert	Rev E	Date 2/12/81	Page 13



1k ohm resistor from 1 to 16
330 ohm resistor from 2 to 15

XEROX PARC/CSL	Project DDTape	Stuff to Keep Route Happy	File DDTape13.sil	Designer Tim Diebert	Rev E	Date 12/09/80	Page 14

E D G E C O N N E C T O R



C A B L E C O N N E C T O R

Misc Clean up REV D

As viewed from the component side

Load .01uf caps all available locations near chips
Install heavy ground connections from edge to power p

XEROX PARC/CSL	Project	Reference	File	Designer	Rev	Date	Page
	DDTape	Layout	DDTape14.sil	Tim Diebert	E	3/17/81	15